The TTL Data Book

Volume 2

1985

Advanced Low-Power Schottky
Advanced Schottky

TEXAS INSTRUMENTS

The TTL Data Book
Volume 2

Advanced Low-Power Schottky and Advanced Schottky Logic Circuits

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

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Information contained herein supersedes data published in the *ALS/AS Logic Circuits Data Book 1983*, SDAD001.

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INTRODUCTION

In this volume, Texas Instruments presents technical information on the most advanced families of TTL integrated circuits, Advanced Low-Power Schottky† (ALS), and Advanced Schottky† (AS). The choice provided by selecting from either ALS or AS functions provides this systems design engineer with a management tools to achieve performance budgeting. Efficient design parameters can be met easily by taking advantage of this low power of ALS in noncritical paths and using high performance AS in speed critical paths. The efficiencies realized by ALS and AS are being offered to system designers in the following forms:

1. Pin-to-pin compatible, plug-in versions of most popular LSTTL and STTL functions.
2. Higher density MSI and LSI functions.

The ease of use of pin-to-pin compatible functions enables designers to upgrade existing TTL based systems with the following benefits:

- Reduce system power requirements
- Enhance critical system performance
- Improved overall system reliability

New system designs can can capitalize on both the improved efficiency of the pin-compatible devices and the higher densities of the MSI/LSI series of devices, such as the 'ALS632 32-bit parallel error detection and connection circuitry, with the following system benefits:

- Reduced system component count
- Expanded functional capabilities
- Improved levels of cost effectiveness
- DC and AC specifications across the full rated supply voltage and temperature ranges with AC specifications at 50 pF loading.

ALS and AS devices utilize an advanced wafer fabrication process that includes ion-implanted transistors, oxide isolations, and composed mask sets. This process is coupled with circuit design techniques to implement the following:

- Improve input threshold and noise margins
- Improve line driving and receiving
- Maintain or increase drive capability
- Increase density of LSI functions
- Implement universal logic solutions
- Take advantage of new packaging
  - — 24-pin 300-ml DIP
  - — Ceramic and plastic chip carriers
  - — Small Outline (SO) Package

The ALS/AS family will grow to well over 300 devices through the end of 1985. Included among the new functions are:

- 16-bit by 16-bit universal multiplier
- 20-MHz 8-bit-slice universal processor element with on-board register file
- 20-MHz 14-bit controller with 9-word stack
- 20-MHz 16-bit barrel shifter
- Many additional pin-compatible ALS and AS devices

Logic symbols prepared in accordance with IEEE activity and pin assignments for all bipolar devices are shown in the Product Guide section of Volume 1 with typical performance data and chip carrier information. Package dimensions given in the Mechanical Data section of this book are in metric measurement (and parenthetically in inches), which should simplify board layout for designers involved in metric conversion and new designs.

While this volume offers design and specification data for bipolar Advanced Low-Power Schottky (ALS) and Advanced Schottky (AS) components, complete technical data for any TI semiconductor product is available from your nearest TI field sales office or local authorized TI distributor.

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

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NUMERICAL INDEX

Please note: Details of all other Texas Instruments SN54/74 Families are contained in TTL Data Book Vol. 1

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GLOSSARY
ALS/AS TTL SYMBOLS, TERMS, AND DEFINITIONS

INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

PART I — OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)

f_{max} **Maximum clock frequency**
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

I_{CC} **Supply current**
The current into* the V_{CC} supply terminal of an integrated circuit.

I_{CCH} **Supply current, outputs high**
The current into* the V_{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the high level.

I_{CCL} **Supply current, outputs low**
The current into* the V_{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the low level.

I_{IH} **High-level input current**
The current into* an input when a high-level voltage is applied to that input.

I_{IL} **Low-level input current**
The current into* an input when a low-level voltage is applied to that input.

I_{OH} **High-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.

I_{OL} **Low-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.

I_{OS} **Short-circuit output current**
The current into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

I_{OZH} **Off-state (high-impedance-state) output current (of a three-state output) with high-level voltage applied**
The current flowing into* an output having three-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output and with a high-level voltage applied to the output.
NOTE: This parameter is measured with other input conditions established that would cause the output to be at a low level if it were enabled.

*Current out of a terminal is given as a negative value.

I_{OZL} **Off-state (high-impedance-state) output current (of a three-state output) with low-level voltage applied**
The current flowing into* an output having three-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output and with a low-level voltage applied to the output.
NOTE: This parameter is measured with other input conditions established that would cause the output to be at a high level if it were enabled.

V_{IH} **High-level input voltage**
An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.
NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IK} **Input clamp voltage**
An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.

V_{IL} **Low-level input voltage**
An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.
NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{OH} **High-level output voltage**
The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a high level at the output.

V_{OL} **Low-level output voltage**
The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a low level at the output.

t_a **Access time**
The time interval between the application of a specific input pulse and the availability of valid signals at an output.

t_{dis} **Disable time (of a three-state output)**
The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state. (t_{dis} = t_{PHZ} or t_{PLZ}).

t_{en} **Enable time (of a three-state output)**
The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low). (t_{en} = t_{PZH} or t_{PZL}).

*Current out of a terminal is given as a negative value.

t_h **Hold time**
The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.
NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

t_{pd} **Propagation delay time**
The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. (t_{pd} = t_{PHL} or t_{PLH}).

t_{PHL} **Propagation delay time, high-to-low-level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{PHZ} **Disable time (of a three-state output) from high level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

t_{PLH} **Propagation delay time, low-to-high-level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

t_{PLZ} **Disable time (of a three-state output) from low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

t_{PZH} **Enable time (of a three-state output) to high level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.

t_{PZL} **Enable time (of a three-state output) to low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.

t_{sr} **Sense recovery time**
The time interval needed to switch a memory from a write mode to a read mode and to obtain valid data signals at the output.

t_{su} **Setup time**
The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.
NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

t_w **Pulse duration (width)**
The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

PART II – CLASSIFICATION OF CIRCUIT COMPLEXITY

Gate Equivalent Circuit

A basic unit-of-measure of relative digital-circuit complexity. The number of gate equivalent circuits is that number of individual logic gates that would have to be interconnected to perform the same function.

Large-Scale Integration, LSI

A concept whereby a complete major subsystem or system function is fabricated as a single microcircuit. In this context a major subsystem or system, whether digital or linear, is considered to be one that contains 100 or more equivalent gates or circuitry of similar complexity.

Medium-Scale Integration, MSI

A concept whereby a complete subsystem or system function is fabricated as a single microcircuit. The subsystem or system is smaller than for LSI, but whether digital or linear, is considered to be one that contains 12 or more equivalent gates or circuitry of similar complexity.

Small-Scale Integration, SSI

Integrated circuits of less complexity than medium-scale integration (MSI).

Very-Large-Scale Integration, VLSI

The description of any IC technology that is much more complex than large-scale integration (LSI), and involves a much higher equivalent gate count. At this time an exact definition including a minimum gate count has not been standardized by JEDEC or the IEEE.

EXPLANATION OF FUNCTION TABLES

The following symbols are used in function tables on TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
→	=	value/level or resulting value/level is routed to indicated destination
↶	=	value/level is re-entered
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state-output
a . . h	=	the level of steady-state inputs at inputs A through H respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
$\bar{Q}_0$	=	complement of Q_0 or level of $\bar{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↓ or ↑
⎍	=	one high-level pulse
⎎	=	one low-level pulse
TOGGLE	=	each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑.

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\bar{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, ⎍ or ⎎, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

Among the most complex function tables in this book are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74194.

FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

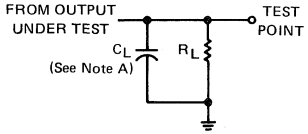
The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output Q_A, data entered at B will be at Q_B, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

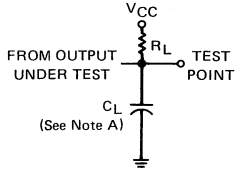
The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A, the previous levels of Q_C and Q_D are now at Q_B and Q_C, respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both mode inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

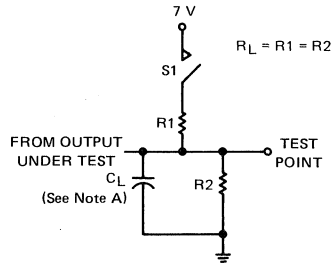
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

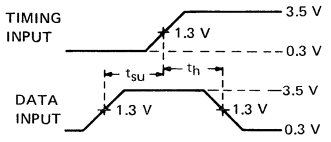


LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

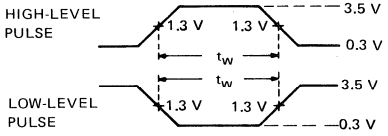


LOAD CIRCUIT FOR THREE-STATE OUTPUTS

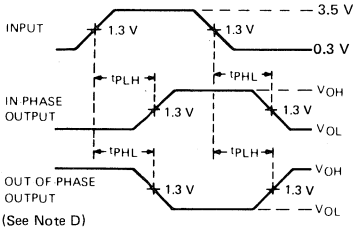
NOTE A. C_L includes probe and jig capacitance.



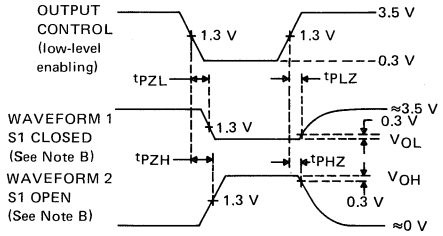
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cyle = 50%.

D. When measuring propagation delay times of 3-state outputs, switch S1 is open.

TYPICAL CHARACTERISTICS†

'ALS00A
PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

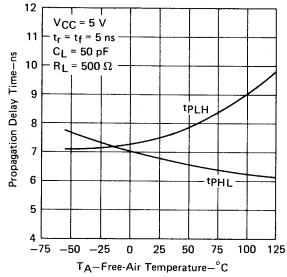


FIGURE 1

'ALS00A
PROPAGATION DELAY TIMES
vs
INPUT RISE & FALL TIMES

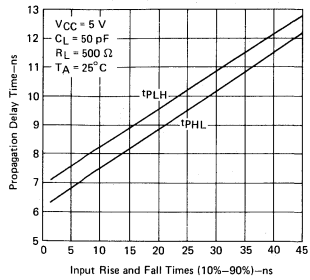


FIGURE 2

'ALS00A
PROPAGATION DELAY TIMES
vs
LOAD CAPACITANCE

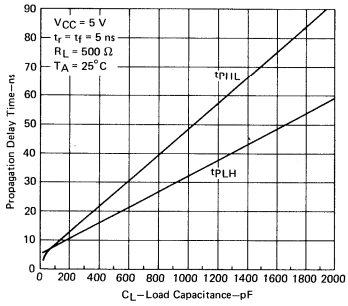


FIGURE 3

'ALS244A
PROPAGATION DELAY TIMES
vs
LOAD CAPACITANCE

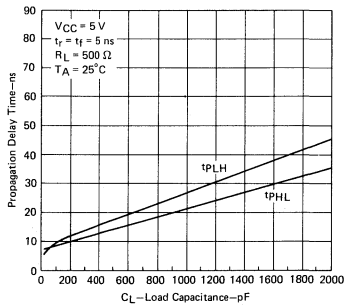


FIGURE 4

'ALS00A
POWER DISSIPATION PER GATE
vs
FREQUENCY

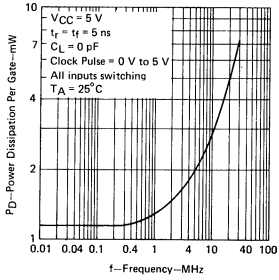


FIGURE 5

†Data for temperatures below 0°C and above 70°C are applicable for Series 54ALS circuits only.

TYPICAL CHARACTERISTICS†

'AS804A
PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

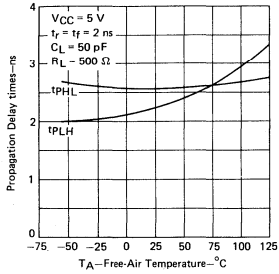


FIGURE 1

'AS804A
PROPAGATION DELAY TIMES
vs
INPUT RISE AND FALL TIMES

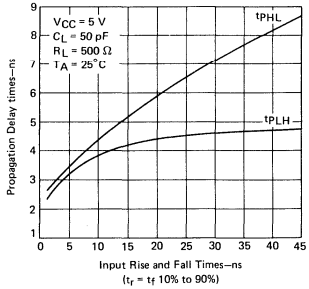


FIGURE 2

'AS804A
PROPAGATION DELAY TIMES
vs
LOAD CAPACITANCE

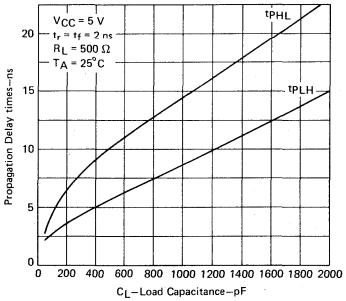


FIGURE 3

†Data for temperatures below 0°C and above 70°C are applicable for Series 54AS Circuits only.

GATES AND INVERTERS

POSITIVE-NAND GATES AND INVERTERS

DESCRIPTION	TYPE	TECHNOLOGY	
		ALS	AS
Hex 2-Input Gates	'804	●	B
Hex Inverters	'04	A	●
	'1004	A	●
Quadruple 2-Input Gates	'00	A	●
	'1000	A	A
Triple 3-Input Gates	'10	A	●
	'1010	A	
Dual 4-Input Gates	'20	A	●
	'1020	A	
8-Input Gates	'30	A	●
13-Input Gates	'133	●	
Dual 2-Input Gates	'8003	●	

POSITIVE-NAND GATES AND INVERTERS WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY	
		ALS	AS
Hex Inverters	'05	A	
	'1005	●	
Quadruple 2-Input Gates	'01	●	
	'03	B	
	'1003	A	
Triple 3-Input Gates	'12	A	
Dual 4-Input Gates	'22	B	

POSITIVE-AND GATES

DESCRIPTION	TYPE	TECHNOLOGY	
		ALS	AS
Hex 2-Input Gates	'808	●	B
Quadruple 2-Input Gates	'08	●	●
	'1008	A	●
Triple 3-Input Gates	'11	A	●
	'1011	A	
Dual 4-Input Gates	'21	●	●

POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY	
		ALS	AS
Quadruple 2-Input Gates	'09	●	
Triple 3-Input Gates	'15	A	

POSITIVE-OR GATES

DESCRIPTION	TYPE	TECHNOLOGY	
		ALS	AS
Hex 2-Input Gates	'832	●	B
Quadruple 2-Input Gates	'32	●	●
	'1032	A	●

POSITIVE-NOR GATES

DESCRIPTION	TYPE	TECHNOLOGY	
		ALS	AS
Hex 2-Input Gates	'805	●	B
Quadruple 2-Input Gates	'02	●	●
	'1002	A	
Triple 3-Input Gates	'27	●	●

● Denotes available technology.
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GATES, EXPANDERS, BUFFERS, DRIVERS, AND TRANSCEIVERS

BUFFER AND INTERFACE GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY	
		ALS	AS
Hex	'35	A	
	'1035	●	
Hex Inverter	'1005	●	
Quad 2-Input Positive NAND	'38	A	
	'1003	A	
Quad 2-Input Positive-NOR	'33	A	

BUFFERS, DRIVERS, AND BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY	
		ALS	AS
Noninverting Octal Buffers/Drivers	'743	▲	
	'757	●	●
	'760		●
Inverting Octal Buffers/Drivers	'742	▲	
	'756	●	●
	'763	▲	●
Inverting and Noninverting Octal Buffers/Drivers	'762	▲	●
Noninverting Quad Transceivers	'759	▲	●
Inverting Quad Transceivers	'758	▲	●

GATES, BUFFERS, DRIVERS, AND BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY	
		ALS	AS
Noninverting Octal Buffers/Drivers	'241	A	●
	'244	A	●
	'465	A	
	'467	A	
	'541	●	
	'1241△	▲	
	'1244△	A	
Inverting Octal Buffers/Drivers	'231		●
	'240	A	●
	'466	A	
	'468	A	
	'540	●	
	'1240△	●	
Inverting and Noninverting Octal Buffers/Drivers	'230		●
Octal Transceivers	'245	A	●
	'1245	A	
Noninverting Hex Buffers/Drivers	'365	▲	
	'367	▲	
Inverting Hex Buffers/Drivers	'366	▲	
	'368	▲	
Noninverting Quad Transceivers	'243	A	●
	'1243△	▲	
Inverting Quad Transceivers	'242	A	●
	'1242△	▲	

50-OHM/75-OHM LINE DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY	
		ALS	AS
Hex 2-Input Positive-NAND	'804	●	B
Hex 2-Input Positive-NOR	'805	●	B
Hex 2-Input Positive-AND	'808	●	B
Hex 2-Input Positive-OR	'832	●	B
'804 with Center Pinning	'1804	△	●
'805 with Center Pinning	'1805	△	●
'808 with Center Pinning	'1808	△	●
'832 with Center Pinning	'1832	△	●

CF Denotes Contact Factory.
● Denotes available technology.
▲ Denotes planned new products.
△ Denotes very low power.
A Denotes "A" suffix version available in the technology indicated.
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BUFFERS, DRIVERS, TRANSCEIVERS, AND CLOCK GENERATORS

BUFFERS, CLOCK/MEMORY DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY	
		ALS	AS
Hex 2-Input Positive-NAND	'804	●	B
Hex 2-Input Positive NOR	'805	●	B
Hex 2-Input Positive-AND	'808	●	B
Hex 2-Input Positive-OR	'832	●	B
Hex Inverter	'1004	●	●
Hex Buffer	'34	●	●
	'1034	●	A
Quad 2-Input Positive-NAND	'37	A	
	'1000	A	A
Quad 2-Input Positive-NOR	'28	A	
	'1002	A	
	'1036		A
Quad 2-Input Positive-AND	'1008	A	●
Quad 2-Input Positive-OR	'1032	A	●
Triple 3-Input Positive-NAND	'1010	A	
Triple 3-Input Positive-AND	'1011	A	
Dual 4-Input Positive-NAND	'40	A	
	'1020	A	

OCTAL BUS TRANSCEIVERS/MOS DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY	
		ALS	AS
Inverting Outputs, 3-State	'2620		●
	'2640		●
True Outputs, 3-State	'2623		●
	'2645		●

OCTAL BUFFERS AND LINE DRIVERS WITH INPUT/ OUTPUT RESISTORS

DESCRIPTION		TYPE	TECHNOLOGY	
			ALS	AS
Input Resistors	Inverting Outputs	'746	●	
	Noninv. Outputs	'747	●	
Output Resistors	Inverting Outputs	'2540	●	
	Noninv. Outputs	'2541	●	

OCTAL BI-/TRI-DIRECTIONAL BUS TRANSCEIVERS

DESCRIPTION		TYPE OF OUTPUT	TYPE	TECHNOLOGY	
				ALS	AS
12 mA/24 mA/ 48 mA/64 mA Sink, True Outputs	Low Power	3-State	'245	A	●
		OC	'621	A	●
		3-State	'623	A	●
		OC, 3-State	'639	A	●
		3-State	'652	▲	●
		OC, 3-State	'654	▲	
	Very Low Power	OC	'1621	▲	
		3-State	'1623	▲	
		OC, 3-State	'1639	▲	
12 mA/24 mA/ 48 mA/64 mA Sink, Inverting Outputs	Low Power	3-State	'620	A	●
		OC	'622	A	●
		OC, 3-State	'638	A	●
		3-State	'651	▲	●
		OC, 3-State	'653	▲	
	Very Low Power	3-State	'1620	▲	
		OC	'1622	▲	
		OC, 3-State	'1638	▲	
12 mA/24 mA/ 48 mA/64 mA Sink, True Outputs	Low Power	OC	'641	A	●
		3-State	'645	A	●
	Very Low Power	OC	'1641	A	
		3-State	'1645	A	
12 mA/24 mA/ 48 mA/64 mA Sink, Inverting Outputs	Low Power	3-State	'640	A	●
		OC	'642	A	●
	Very Low Power	3-State	'1640	A	
		OC	'1642	▲	
12 mA/24 mA/ 48 mA/64 mA Sink, True and Invert. Outputs	Low Power	3-State	'643	A	●
		OC	'644	A	●
	Very Low Power	3-State	'1643	▲	
		OC	'1644	▲	
Registered with Multiplex 12 mA/24 mA/48 mA/ 64 mA True Outputs		3-State	'646	▲	●
		OC	'647	▲	
Registered with Multiplexed 12 mA/24 mA/48 mA/ 64 mA Inverting Outputs		3-State	'648	▲	●
		OC	'649	▲	
Universal Transceiver/ Port Controllers		3-State	'877		●
			'852		●
			'856		●

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FLIP-FLOPS

DUAL AND SINGLE FLIP-FLOPS

DESCRIPTION	TYPE	TECHNOLOGY	
		ALS	AS
Dual J-K Edge-Triggered	'109	A	●
	'112	A	▲
	'113	A	▲
	'114	A	▲
Dual D-Type	'74	A	●

QUAD AND HEX FLIP-FLOPS

DESCRIPTION	NO. OF FFs	OUTPUTS	TYPE	TECHNOLOGY	
				ALS	AS
D-Type	6	Q	'174	●	●
	4	Q, $\overline{Q}$	'175	●	●

OCTAL, 9-BIT, AND 10-BIT D-TYPE FLIP-FLOPS

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY	
				ALS	AS
True Data	Octal	3-State	'374	●	●
		3-State	'574	A	●
True Data with Clear	Octal	2-State	'273	●	
		3-State	'575	●	●
		3-State	'874	●	●
		3-State	'878	A	●
Inverting	Octal	3-State	'534	●	●
		3-State	'564	●	
		3-State	'576	A	●
Invert. with Clear	Octal	3-State	'577	A	●
		3-State	'879	A	●
Invert. with Preset	Octal	3-State	'876	A	●
True	Octal	3-State	'825		●
Inverting	Octal	3-State	'826		●
True	9-Bit	3-State	'823		●
Inverting	9-Bit	3-State	'824		●
True	10-Bit	3-State	'821		●
Inverting	10-Bit	3-State	'822		●

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LATCHES AND MULTIVIBRATORS

D-TYPE OCTAL, 9-BIT, AND 10-BIT READ BACK LATCHES

DESCRIPTION	NO. OF BITS	TYPE	TECHNOLOGY	
			ALS	AS
Edge-Triggered Inverting and Noninverting	Octal	'996	▲	
Transparent True	Octal 9-Bit 10-Bit	'990 '992 '994	▲ ▲ ▲	
Transparent Inverting	Octal 9-Bit 10-Bit	'991 '993 '995	▲ ▲ ▲	
Transparent with Clear True Outputs	Octal	'666	▲	
Transparent with Clear Inverting Outputs	Octal	'667	▲	

OCTAL, 9-BIT, AND 10-BIT LATCHES

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY	
				ALS	AS
Transparent	Octal	3-State	'373	●	●
		3-State	'573	A	●
Dual 4-Bit Transparent	Octal	3-State	'873	●	●
Inverting Transparent	Octal	3-State	'533	●	●
		3-State	'563	●	
		3-State	'580	●	●
Dual 4-Bit Invert. Transpar.	Octal	3-State	'880	●	●
Addressable	Octal	2-State	'259	▲	
True	Octal	3-State	'845	▲	●
Inverting	Octal	3-State	'846	▲	●
True	9-Bit	3-State	'843	▲	●
Inverting	9-Bit	3-State	'844	▲	●
True	10-Bit	3-State	'841	▲	●
Inverting	10-Bit	3-State	'842	▲	●

CF Denotes contact factory.
● Denotes available technology.
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REGISTERS

SHIFT REGISTERS

DESCRIPTION	NO. OF BITS	MODES				TYPE	TECHNOLOGY	
		S-R	S-L	LOAD	HOLD		ALS	AS
Parallel-In, Parallel-Out, Bidirectional	8	X	X	X	X	'299	●	▲
		X	X	X	X	'323	●	▲
	4	X	X	X	X	'194		●
Parallel-In, Parallel-Out	4	X		X		'95		●
		X		X		'195		▲
		X		X		'395		▲
Serial-In, Parallel-Out	8	X				'164	▲	
Parallel-In, Serial-Out	8	X		X	X	'165	▲	
		X		X	X	'166	▲	

REGISTER FILES

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY	
			ALS	AS
Dual 16 Words × 4 Bits	3-State	'870		●
	3-State	'871		●

OTHER REGISTERS

DESCRIPTION	TYPE	TECHNOLOGY	
		ALS	AS
Quadruple Multiplexers with Storage	'298		●
8-Bit Universal Shift Registers	'299	●	▲
10-Bit Register Noninverting	'821	▲	●
10-Bit Register Inverting	'822	▲	●
9-Bit Register Noninverting	'823	▲	●
9-Bit Register Inverting	'824	▲	●
8-Bit Register Noninverting	'825	▲	●
8-Bit Register Inverting	'826	▲	●

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COUNTERS

SYNCHRONOUS COUNTERS – POSITIVE EDGE TRIGGERED

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY	
			ALS	AS
Decade	Sync	'160	B	●
	Sync	'162	B	●
	Sync	'560	A	
Decade Up/Down	Sync	'168	B	●
	Async	'190	●	
	Async	'192	●	
	Sync	'568	A	
4-Bit Binary	Sync	'161	B	●
	Sync	'163	B	●
	Sync	'561	A	
4-Bit Binary Up/Down	Sync	'169	B	●
	Async	'191	●	
	Async	'193	●	
	Sync	'569	A	
8-Bit Up/Down	Async CLR	'867		●
	Sync CLR	'869		●

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DECODERS, ENCODERS, DATA SELECTORS/MULTIPLEXERS AND SHIFTERS

DATA SELECTORS/MULTIPLEXERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY	
			ALS	AS
16-To-1	3-State	'250		●
	3-State	'850		●
	3-State	'851		●
8-To-1	2-State	'151	●	●
	3-State	'251	●	▲
Dual 4-To-1	2-State	'153	●	●
	3-State	'253	●	●
	2-State	'352	●	●
	3-State	'353	●	●
Quad 2-To-1 with Storage	2-State	'298		●
Quad 2-To-1	2-State	'157	●	●
	2-State	'158	●	●
	3-State	'257	A	●
	3-State	'258	A	●
6-To-1 Universal Multiplexer	3-State	'857	●	●

DECODERS/DEMULTIPLEXERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY	
			ALS	AS
3-To-8 with Address Latches	2-State	'131	●	●
		'137	●	●
3-To-8	2-State	'138	●	●
	3-State	'538	▲	
Dual 2-To-4	2-State	'139	▲	
Dual 1-To-4 Decoders	3-State	'539	▲	

SHIFTERS

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY	
			ALS	AS
Parallel 16-Bit Multi-Mode Barrel Shifter	3-State	'897		▲

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MEMORY/MICROPROCESSOR CONTROLLERS

MEMORY/MICROPROCESSOR CONTROLLERS

DESCRIPTION	TYPE	TECHNOLOGY	
		ALS	AS
System Controllers, Universal (or For 888)	'890		▲

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COMPARATORS AND ERROR DETECTION CIRCUITS

8-BIT COMPARATORS

DESCRIPTION								TECHNOL.	
INPUTS	P=Q	P=Q	P>Q	P>Q	OUTPUT	OUTPUT ENABLE	TYPE	ALS	AS
20-kΩ Pull-Up	Yes	No	No	No	OC	Yes	'518	●	
	No	Yes	No	No	2-State	Yes	'520	●	
	No	Yes	No	No	OC	Yes	'522	●	
Standard	Yes	No	No	No	OC	Yes	'519	●	
	No	Yes	No	No	2-State	Yes	'521	●	
	No	Yes	No	Yes	2-State	Yes	'688	●	
	No	Yes	No	No	OC	Yes	'689	●	
Latched P	No	No	Yes	Yes	2-State	Yes	'885		●
Latched P and Q	Yes	No	Yes	Yes	Latched	Yes	'866		●

ADDRESS COMPARATORS

DESCRIPTION	OUTPUT ENABLE	LATCHED OUTPUT	TYPE	TECHNOLOGY	
				ALS	AS
16-Bit to 4-Bit	Yes		'677	●	
		Yes	'678	●	
12-Bit to 4-Bit	Yes		'679	●	
		Yes	'680	●	

PARITY GENERATORS/CHECKERS, ERROR DETECTION AND CORRECTION CIRCUITS

DESCRIPTION		NO. OF BITS	TYPE	TECHNOLOGY	
				ALS	AS
Odd/Even Parity Generators/Checkers		9	'280		●
		9	'286		●
Parallel Error Detection/Correction Circuits	3-State	16	'616	●	
	OC	16	'617	▲	
	3-State	32	'632	A	
	OC	32	'633	▲	
	3-State	32	'634	▲	
	OC	32	'635	▲	

FUSE-PROGRAMMABLE COMPARATOR

DESCRIPTION	TYPE	TECHNOLOGY	
		ALS	AS
16-Bit Identity Comparator	'526	▲	
12-Bit Identity Comparator	'528	▲	
8-Bit Identity Comparator and 4-Bit Comparator	'527	▲	

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ARITHMETIC CIRCUITS AND PROCESSOR ELEMENTS

ACCUMULATORS, ARITHMETIC LOGIC UNITS, LOOK-AHEAD CARRY GENERATORS

DESCRIPTION		TYPE	TECHNOLOGY	
			ALS	AS
4-Bit Arithmetic Logic Units/ Function Generators		'181		A
		'881		A
Look-Ahead Carry Generators	16-Bit	'182		▲
		'282		▲
	32-Bit	'882		●
Counter Look Ahead		'264		●

OTHER ARITHMETIC OPERATORS

DESCRIPTION	TYPE	TECHNOLOGY	
		ALS	AS
Quad 2-Input Exclusive-OR Gates with Totem-Pole Outputs	'86	●	
Quad 2-Input Exclusive-OR Gates with Open-Coll. Outputs	'136	●	
Quad 2-Input Exclusive-NOR Gates	'810	●	▲
Quad 2-Input Exclusive-NOR Gates with Open-Coll. Outputs	'811	●	▲

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The TTL Data Book
Volume 2

D2661, APRIL 1982—REVISED DECEMBER 1983

- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

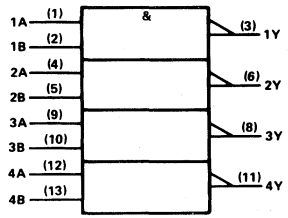
These devices contain four independent 2-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54ALS00A and SN54AS00 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS00A and SN74AS00 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (each gate)

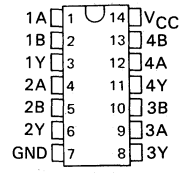
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol

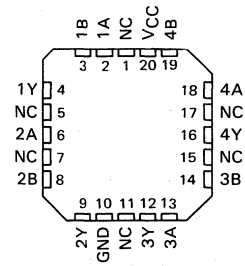


Pin numbers shown are for J and N packages.

SN54ALS00A, SN54AS00 . . . J PACKAGE
SN74ALS00A, SN74AS00 . . . N PACKAGE
SN74ALS00A, SN74AS00 . . . D PACKAGE
(TOP VIEW)



SN54ALS00A, SN54AS00 . . . FH OR FK PACKAGE
SN74ALS00A, SN74AS00 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS00A . . . . . −55 °C to 125 °C
SN74ALS00A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS00A			SN74ALS00A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS00A			SN74ALS00A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.5	0.85		0.5	0.85	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.5	3		1.5	3	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS00A		SN74ALS00A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	3	14	3	11	ns
t_{PHL}	A or B	Y	2	10	2	8	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS00 . . . . . −55 °C to 125 °C
SN74AS00 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS00			SN74AS00			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS00			SN74AS00			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		2	3.2		2	3.2	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		10.8	17.4		10.8	17.4	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS00		SN74AS00		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	5	1	4.5	ns
t_{PHL}	A or B	Y	1	5	1	4	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

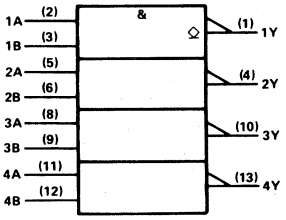
These devices contain four independent 2-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS01 is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS01 is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (each gate)

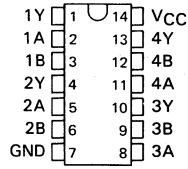
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol

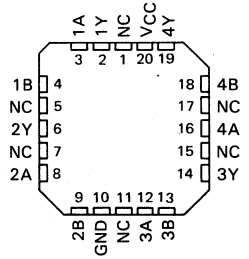


Pin numbers shown are for J and N packages.

SN54ALS01 . . . J PACKAGE
SN74ALS01 . . . N PACKAGE
SN74ALS01 . . . D PACKAGE
(TOP VIEW)



SN54ALS01 . . . FH OR FK PACKAGE
SN74ALS01 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS01 . . . . . −55 °C to 125 °C
SN74ALS01 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS01			SN74ALS01			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS01			SN74ALS01			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.43	0.85		0.43	0.85	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.62	3		1.62	3	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = MIN to MAX				UNIT
			SN54ALS01		SN74ALS01		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	23	59	23	54	ns
t_{PHL}	A or B	Y	8	29	8	28	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D2661, APRIL 1982—REVISED DECEMBER 1983

- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

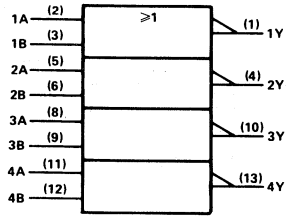
These devices contain four independent 2-input NOR gates. They perform the Boolean functions $Y = \overline{A+B}$ or $Y = \overline{A}\cdot\overline{B}$ in positive logic.

The SN54ALS02 and SN54AS02 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS02 and SN74AS02 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

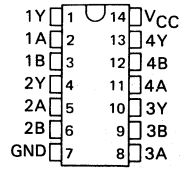
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol

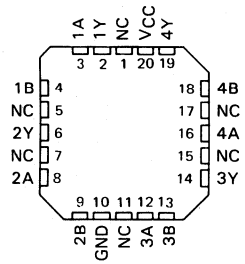


Pin numbers shown are for J and N packages.

SN54ALS02, SN54AS02 . . . J PACKAGE
SN74ALS02, SN74AS02 . . . N PACKAGE
SN74ALS02, SN74AS02 . . . D PACKAGE
(TOP VIEW)



SN54ALS02, SN54AS02 . . . FH OR FK PACKAGE
SN74ALS02, SN74AS02 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS02 . . . . . −55 °C to 125 °C
SN74ALS02 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS02			SN74ALS02			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS02			SN74ALS02			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.86	2.2		0.86	2.2	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		2.16	4		2.16	4	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS02		SN74ALS02		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	3	14	3	12	ns
t_{PHL}	A or B	Y	3	11	3	10	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS02 . . . . . −55 °C to 125 °C
SN74AS02 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS02			SN74AS02			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS02			SN74AS02			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,.	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		3.7	5.9		3.7	5.9	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		12.5	20.1		12.5	20.1	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS02		SN74AS02		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	5	1	4.5	ns
t_{PHL}	A or B	Y	1	5	1	4.5	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

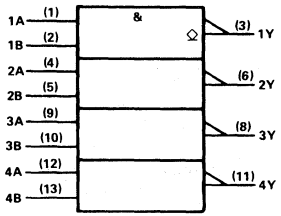
These devices contain four independent 2-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS03A is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS03A is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (each gate)

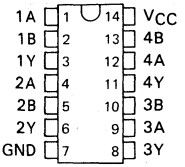
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol

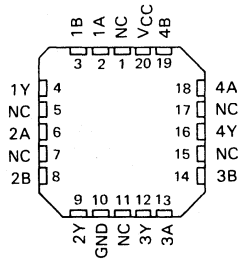


Pin numbers shown are for J and N packages.

SN54ALS03A . . . J PACKAGE
SN74ALS03A . . . N PACKAGE
SN74ALS03A . . . D PACKAGE
(TOP VIEW)



SN54ALS03A . . . FH OR FK PACKAGE
SN74ALS03A . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS03A . . . . . −55 °C to 125 °C
SN74ALS03A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS03A			SN74ALS03A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS03A			SN74ALS03A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.43	0.85		0.43	0.85	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.62	3		1.62	3	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = MIN to MAX				UNIT
			SN54ALS03A		SN74ALS03A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	23	59	23	54	ns
t_{PHL}	A or B	Y	5	26	5	22	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D2661, APRIL 1982—REVISED DECEMBER 1983

- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

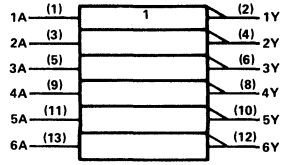
These devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$.

The SN54ALS04A and SN54AS04 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS04A and SN74AS04 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE
(each inverter)

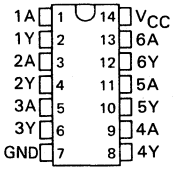
INPUT A	OUTPUT Y
H	L
L	H

logic symbol

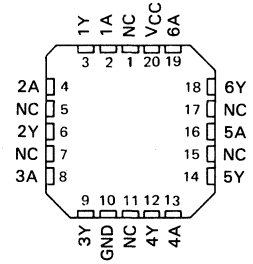


Pin numbers shown are for J and N packages.

SN54ALS04A, SN54AS04 . . . J PACKAGE
SN74ALS04A, SN74AS04 . . . N PACKAGE
SN74ALS04A, SN74AS04 . . . D PACKAGE
(TOP VIEW)



SN54ALS04A, SN54AS04 . . . FH OR FK PACKAGE
SN74ALS04A, SN74AS04 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS04A . . . . . −55°C to 125°C
SN74ALS04A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS04A			SN74ALS04A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS04A			SN74ALS04A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.65	1.1		0.65	1.1	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		2.9	4.2		2.9	4.2	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS04A		SN74ALS04A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	14	3	11	ns
t_{PHL}	A	Y	2	12	2	8	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS04 . . . . . −55 °C to 125 °C
SN74AS04 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS04			SN74AS04			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS04			SN74AS04			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		3	4.8		3	4.8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		14	26.3		14	26.3	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS04		SN74AS04		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	6	1	5	ns
t_{PHL}	A	Y	1	4.5	1	4	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D2661, APRIL 1982—REVISED DECEMBER 1983

- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

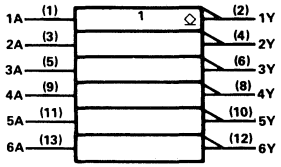
These devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS05A is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS05A is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (each inverter)

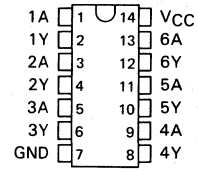
INPUT A	OUTPUT Y
H	L
L	H

logic symbol

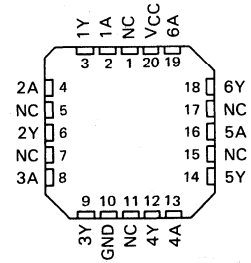


Pin numbers shown are for J and N packages.

SN54ALS05A . . . J PACKAGE
SN74ALS05A . . . N PACKAGE
SN74ALS05A . . . D PACKAGE
(TOP VIEW)



SN54ALS05A . . . FH OR FK PACKAGE
SN74ALS05A . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS05A . . . . . −55°C to 125°C
SN74ALS05A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS05A			SN74ALS05A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS05A			SN74ALS05A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.65	1.1		0.65	1.1	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		2.9	4.2		2.9	4.2	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = MIN to MAX				UNIT
			SN54ALS05A		SN74ALS05A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	23	59	23	54	ns
t_{PHL}	A or B	Y	4	19	4	14	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D2661, APRIL 1982—REVISED DECEMBER 1983

- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

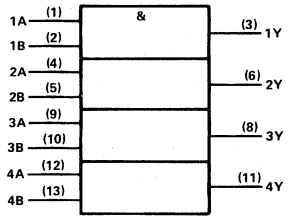
These devices contain four independent 2-input AND gates. They perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

The SN54ALS08 and SN54AS08 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS08 and SN74AS08 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each gate)

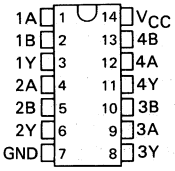
INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol

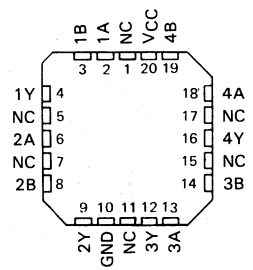


Pin numbers shown are for J and N packages.

SN54ALS08, SN54AS08 . . . J PACKAGE
SN74ALS08, SN74AS08 . . . N PACKAGE
SN74ALS08, SN74AS08 . . . D PACKAGE
(TOP VIEW)



SN54ALS08, SN54AS08 . . . FH OR FK PACKAGE
SN74ALS08, SN74AS08 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS08 . . . . . −55°C to 125°C
SN74ALS08 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS08			SN74ALS08			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS08			SN74ALS08			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2						V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.3	2.4		1.3	2.4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		2.2	4		2.2	4	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS08		SN74ALS08		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	4	16	4	14	ns
t_{PHL}	A or B	Y	3	12	3	10	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS08 . . . . . −55 °C to 125 °C
SN74AS08 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS08			SN74AS08			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS08			SN74AS08			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		5.8	9.3		5.8	9.3	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		14.9	24		14.9	24	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS08		SN74AS08		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	6.5	1	5.5	ns
t_{PHL}	A or B	Y	1	6.5	1	5.5	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

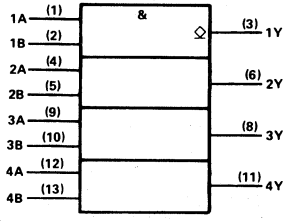
These devices contain four independent 2-input AND gates. They perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{\overline{A}+\overline{B}}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS09 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS09 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

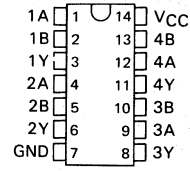
INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol

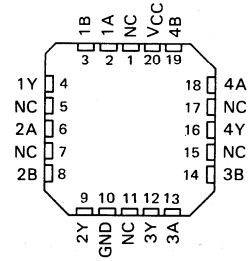


Pin numbers shown are for J and N packages.

SN54ALS09 . . . J PACKAGE
SN74ALS09 . . . N PACKAGE
SN74ALS09 . . . D PACKAGE
(TOP VIEW)



SN54ALS09 . . . FH OR FK PACKAGE
SN74ALS09 . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS09 . . . . . −55 °C to 125 °C
SN74ALS09 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS09			SN74ALS09			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS09			SN74ALS09			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.35	2.4		1.35	2.4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		2.2	4		2.2	4	mA

† All typical values are at V_{CC} = 5 V, T_A = 25 °C

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = MIN to MAX				UNIT
			SN54ALS09		SN74ALS09		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	23	59	23	54	ns
t_{PHL}	A or B	Y	5	17	5	15	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

March 1984

- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

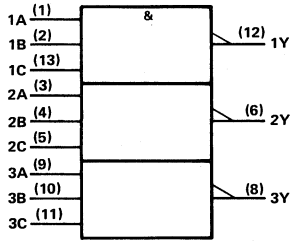
These devices contain three independent 3-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

The SN54ALS10A and SN54AS10 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS10A and SN74AS10 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

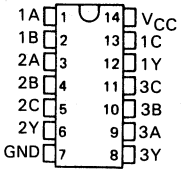
INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

logic symbol

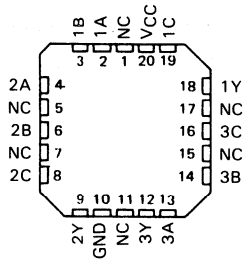


Pin numbers shown are for J and N packages.

SN54ALS10A, SN54AS10 . . . J PACKAGE
SN74ALS10A, SN74AS10 . . . N PACKAGE
SN74ALS10A, SN74AS10 . . . D PACKAGE
(TOP VIEW)



SN54ALS10A, SN54AS10 . . . FH OR FK PACKAGE
SN74ALS10A, SN74AS10 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS10A . . . . . −55 °C to 125 °C
SN74ALS10A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS10A			SN74ALS10A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS10A			SN74ALS10A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.32	0.6		0.32	0.6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.2	2.2		1.2	2.2	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS10A		SN74ALS10A		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	2	13	2	11	ns
t_{PHL}	Any	Y	2	12	2	10	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of The TTL Data Book, Volume 2.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS10 . . . . . −55°C to 125°C
SN74AS10 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS10			SN74AS10			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS10			SN74AS10			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		1.5	2.4		1.5	2.4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		8.1	13		8.1	13	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS10		SN74AS10		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1	5	1	4.5	ns
t_{PHL}	Any	Y	1	5	1	4.5	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of The TTL Data Book, Volume 2.

March 1984

- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

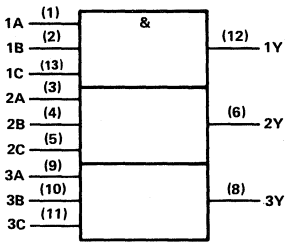
These devices contain three independent 3-input AND gates. They perform the Boolean functions $Y = A \cdot B \cdot C$ or $Y = \overline{\overline{A}+\overline{B}+\overline{C}}$ in positive logic.

The SN54ALS11A and SN54AS11 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS11A and SN74AS11 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

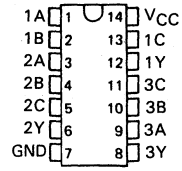
INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

logic symbol

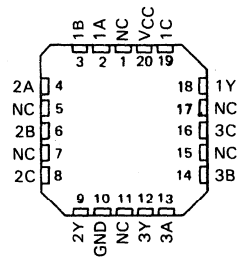


Pin numbers shown are for J and N packages.

SN54ALS11A, SN54AS11 . . . J PACKAGE
SN74ALS11A, SN74AS11 . . . N PACKAGE
SN74ALS11A, SN74AS11 . . . D PACKAGE
(TOP VIEW)



SN54ALS11A, SN54AS11 . . . FH OR FK PACKAGE
SN74ALS11A, SN74AS11 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS11A . . . . . −55 °C to 125 °C
SN74ALS11A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS11A			SN74ALS11A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS11A			SN74ALS11A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		1	1.8		1	1.8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		1.6	3		1.6	3	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS11A		SN74ALS11A		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	2	16	2	13	ns
t_{PHL}	Any	Y	2	12	2	10	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of The TTL Data Book, Volume 2.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS11 . . . . . −55 °C to 125 °C
SN74AS11 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS11			SN74AS11			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS11			SN74AS11			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		4.3	7		4.3	7	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		11.2	18		11.2	18	mA

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS11		SN74AS11		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1	6.5	1	6	ns
t_{PHL}	Any	Y	1	6.5	1	5.5	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12

MARCH 1984

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description

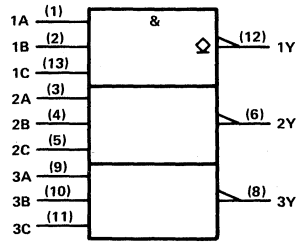
These devices contain three independent 3-input NAND gates with open-collector outputs. These gates perform the Boolean functions $Y = \overline{A \cdot B \cdot C}$ or $Y = \overline{A}+\overline{B}+\overline{C}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS12A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS12A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

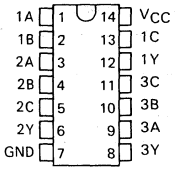
INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

logic symbol

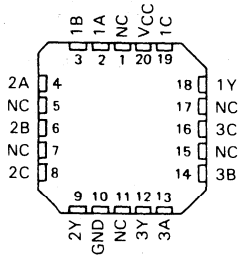


Pin numbers shown are for J and N packages.

SN54ALS12A . . . J PACKAGE
SN74ALS12A . . . N PACKAGE
SN74ALS12A . . . D PACKAGE
(TOP VIEW)



SN54ALS12A . . . FH OR FK PACKAGE
SN74ALS12A . . . FN PACKAGE
(TOP VIEW)



NC No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS12A . . . . . −55°C to 125°C
SN74ALS12A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS12A			SN74ALS12A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS12A			SN74ALS12A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.32	0.6		0.32	0.6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.2	2.2		1.2	2.2	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = MIN to MAX				UNIT
			SN54ALS12A		SN74ALS12A		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	23	59	23	54	ns
t_{PHL}	Any	Y	5	22	5	18	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12

MARCH 1984

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description

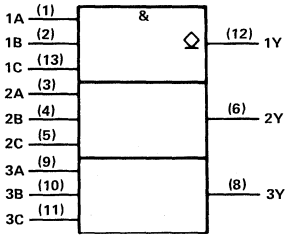
These devices contain three independent 3-input AND gates with open-collector outputs. These gates perform the Boolean functions $Y = A \cdot B \cdot C$ or $Y = \overline{\overline{A}+\overline{B}+\overline{C}}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS15A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS15A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

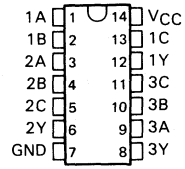
INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

logic symbol

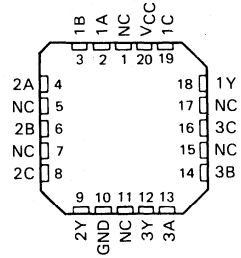


Pin numbers shown are for J and N packages.

SN54ALS15A . . . J PACKAGE
SN74ALS15A . . . N PACKAGE
SN74ALS15A . . . D PACKAGE
(TOP VIEW)



SN54ALS15A . . . FH OR FK PACKAGE
SN74ALS15A . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS15A . . . . . −55°C to 125°C
SN74ALS15A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS15A			SN74ALS15A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS15A			SN74ALS15A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		1	1.8		1	1.8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		1.66	3		1.66	3	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = MIN to MAX				UNIT
			SN54ALS15A		SN74ALS15A		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	20	50	20	45	ns
t_{PHL}	Any	Y	6	23	6	20	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12

D2661, APRIL 1982—REVISED DECEMBER 1983

- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

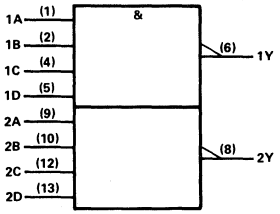
These devices contain two independent 4-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

The SN54ALS20A and SN54AS20 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS20A and SN74AS20 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (each gate)

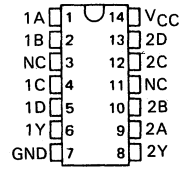
INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

logic symbol

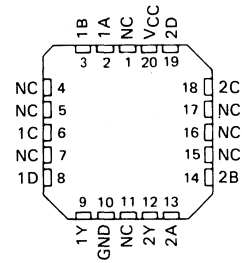


Pin numbers shown are for J and N packages.

SN54ALS20A, SN54AS20 . . . J PACKAGE
SN74ALS20A, SN74AS20 . . . N PACKAGE
SN74ALS20A, SN74AS20 . . . D PACKAGE
(TOP VIEW)



SN54ALS20A, SN54AS20 . . . FH OR FK PACKAGE
SN74ALS20A, SN74AS20 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS20A . . . . . −55 °C to 125 °C
SN74ALS20A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS20A			SN74ALS20A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS20A			SN74ALS20A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.22	0.4		0.22	0.4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		0.81	1.5		0.81	1.5	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS20A		SN74ALS20A		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	3	13	3	11	ns
t_{PHL}	Any	Y	3	12	3	10	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS20 . . . . . −55°C to 125°C
SN74AS20 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS20			SN74AS20			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS20			SN74AS20			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		1	1.6		1	1.6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		5.4	8.7		5.4	8.7	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS20		SN74AS20		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1	5.5	1	5	ns
t_{PHL}	Any	Y	1	5	1	4.5	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D2661, APRIL 1982—REVISED DECEMBER 1983

- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

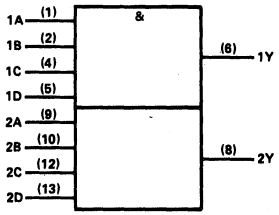
These devices contain two independent 4-input AND gates. They perform the Boolean functions $Y = A \cdot B \cdot C \cdot D$ or $Y = \overline{\overline{A}+\overline{B}+\overline{C}+\overline{D}}$ in positive logic.

The SN54ALS21 and SN54AS21 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS21 and SN74AS21 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

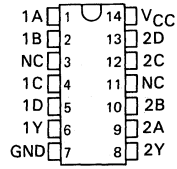
INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

logic symbol

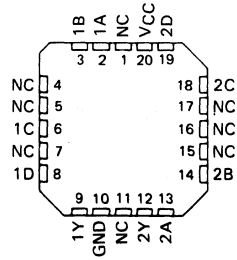


Pin numbers shown are for J and N packages.

SN54ALS21, SN54AS21 . . . J PACKAGE
SN74ALS21, SN74AS21 . . . N PACKAGE
SN74ALS21, SN74AS21 . . . D PACKAGE
(TOP VIEW)



SN54ALS21, SN54AS21 . . . FH OR FK PACKAGE
SN74ALS21, SN74AS21 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS21 . . . . . −55 °C to 125 °C
SN74ALS21 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS21			SN74ALS21			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS21			SN74ALS21			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		0.67	1.2		0.67	1.2	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		1.1	2		1.1	2	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS21		SN74ALS21		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	6	30	6	26	ns
t_{PHL}	Any	Y	3	12	3	10	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS21 . . . . . −55 °C to 125 °C
SN74AS21 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS21			SN74AS21			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS21			SN74AS21			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		2.9	4.6		2.9	4.6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		7.4	12		7.4	12	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS21		SN74AS21		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1	6.5	1	6	ns
t_{PHL}	Any	Y	1	6.5	1	6	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

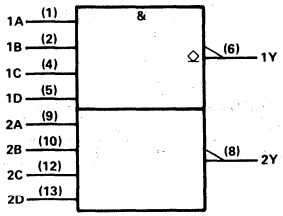
These devices contain two independent 4-input NAND gates. These gates perform the Boolean functions $Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A}+\overline{B}+\overline{C}+\overline{D}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS22B is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS22B is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

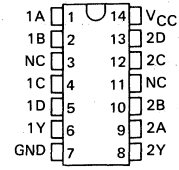
INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

logic symbol

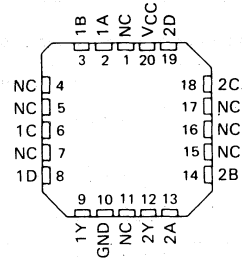


Pin numbers shown are for J and N packages.

SN54ALS22B . . . J PACKAGE
SN74ALS22B . . . N PACKAGE
SN74ALS22B . . . D PACKAGE
(TOP VIEW)



SN54ALS22B . . . FH OR FK PACKAGE
SN74ALS22B . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS22B . . . . . −55°C to 125°C
SN74ALS22B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS22B			SN74ALS22B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS22B			SN74ALS22B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.22	0.4		0.22	0.4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		0.8	1.5		0.8	1.5	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = MIN to MAX				UNIT
			SN54ALS22B		SN74ALS22B		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	23	50	23	45	ns
t_{PHL}	Any	Y	4	21	4	18	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12

TYPES SN54ALS27, SN54AS27, SN74ALS27, SN74AS27
TRIPLE 3-INPUT POSITIVE-NOR GATES

D2661, APRIL 1982—REVISED DECEMBER 1983

- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

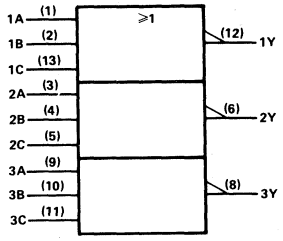
These devices contain three independent 3-input NOR gates. They perform the Boolean functions $Y = \overline{A+B+C}$ or $Y = \overline{A} \cdot \overline{B} \cdot \overline{C}$ in positive logic.

The SN54ALS27 and SN54AS27 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS27 and SN74AS27 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

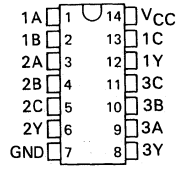
INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

logic symbol

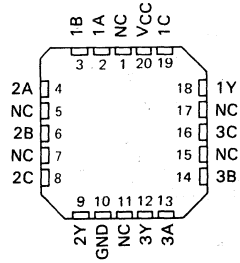


Pin numbers shown are for J and N packages.

SN54ALS27, SN54AS27 . . . J PACKAGE
SN74ALS27, SN74AS27 . . . N PACKAGE
SN74ALS27, SN74AS27 . . . D PACKAGE
(TOP VIEW)



SN54ALS27, SN54AS27 . . . FH OR FK PACKAGE
SN74ALS27, SN74AS27 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS27 . . . . . −55 °C to 125 °C
SN74ALS27 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS27			SN74ALS27			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS27			SN74ALS27			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.97	1.8		0.97	1.8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		2	4		2	4	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS27		SN74ALS27		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	4	22	4	15	ns
t_{PHL}	Any	Y	3	10	3	9	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS27 . . . . . −55°C to 125°C
SN74AS27 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS27			SN74AS27			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS27			SN74AS27			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		4	6.4		4	6.4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		10.6	17.1		10.6	17.1	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS27		SN74AS27		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1	6.5	1	5.5	ns
t_{PHL}	Any	Y	1	5	1	4.5	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D2661, APRIL 1982—REVISED DECEMBER 1983

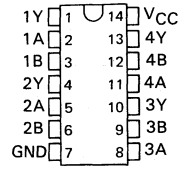
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain four independent 2-input NOR buffer gates. They perform the Boolean functions $Y = \overline{A+B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The SN54ALS28A is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS28A is characterized for operation from 0 °C to 70 °C.

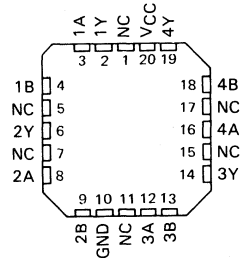
SN54ALS28A . . . J PACKAGE
SN74ALS28A . . . N PACKAGE
SN74ALS28A . . . D PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each gate)

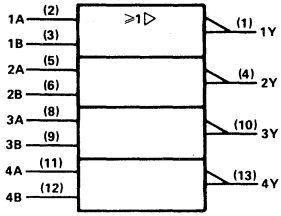
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

SN54ALS28A . . . FH OR FK PACKAGE
SN74ALS28A . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS28A . . . . . −55 °C to 125 °C
SN74ALS28A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS28A			SN74ALS28A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS28A			SN74ALS28A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_{IL} = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		1.7	2.8		1.7	2.8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		5.6	9		5.6	9	mA

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS28A		SN74ALS28A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2	10	2	8	ns
t_{PHL}	A or B	Y	2	10	2	7	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

March 1984

- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain a single 8-input NAND gate and perform the following Boolean functions in positive logic:

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H} \text{ OR}$$

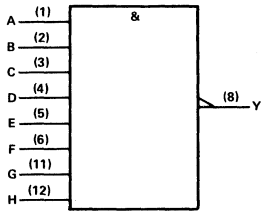
$$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$$

The SN54ALS30A and SN54AS30 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS30A and SN74AS30 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

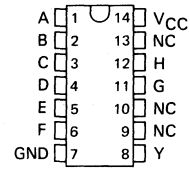
INPUTS A THRU H	OUTPUT Y
All inputs H	L
One or more inputs L	H

logic symbol

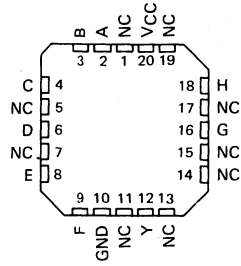


Pin numbers shown are for J and N packages.

SN54ALS30A, SN54AS30 . . . J PACKAGE
SN74ALS30A, SN74AS30 . . . N PACKAGE
SN74ALS30A, SN74AS30 . . . D PACKAGE
(TOP VIEW)



SN54ALS30A, SN54AS30 . . . FH OR FK PACKAGE
SN74ALS30A, SN74AS30 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS30A . . . . . −55 °C to 125 °C
SN74ALS30A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS30A			SN74ALS30A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS30A			SN74ALS30A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.22	0.36		0.22	0.36	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		0.54	0.9		0.54	0.9	mA

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS30A		SN74ALS30A		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	3	12	3	10	ns
t_{PHL}	Any	Y	3	15	3	12	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS30 . . . . . −55°C to 125°C
SN74AS30 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS30			SN74AS30			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS30			SN74AS30			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.9	1.5		0.9	1.5	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		3	4.9		3	4.9	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS30		SN74AS30		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1	5.5	1	5	ns
t_{PHL}	Any	Y	1	5	1	4.5	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12

D2661, APRIL 1982—REVISED DECEMBER 1983

- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

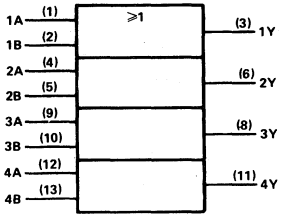
These devices contain four independent 2-input OR gates. They perform the Boolean functions $Y = A + B$ or $Y = \overline{\overline{A} \cdot \overline{B}}$ in positive logic.

The SN54ALS32 and SN54AS32 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS32 and SN74AS32 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each gate)

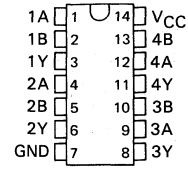
INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic symbol

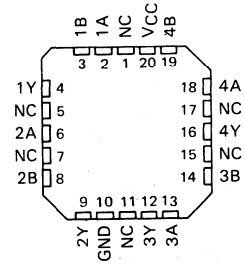


Pin numbers shown are for J and N packages.

SN54ALS32, SN54AS32 . . . J PACKAGE
SN74ALS32, SN74AS32 . . . N PACKAGE
SN74ALS32, SN74AS32 . . . D PACKAGE
(TOP VIEW)



SN54ALS32, SN54AS32 . . . FH OR FK PACKAGE
SN74ALS32, SN74AS32 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS32 . . . . . −55°C to 125°C
SN74ALS32 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS32			SN74ALS32			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS32			SN74ALS32			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.9	4		1.9	4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		2.6	4.9		2.6	4.9	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS32		SN74ALS32		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	3	16	3	14	ns
t_{PHL}	A or B	Y	3	13	3	12	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS32 . . . . . −55 °C to 125 °C
SN74AS32 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS32			SN74AS32			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS32			SN74AS32			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		7.3	12		7.3	12	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		16.5	26.6		16.5	26.6	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS32		SN74AS32		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	7.5	1	5.8	ns
t_{PHL}	A or B	Y	1	6.5	1	5.8	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

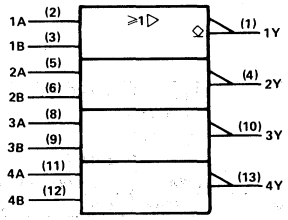
These devices contain four independent 2-input NOR buffer gates with open-collector outputs. Open-collector outputs require resistive pull-up to perform logically but can deliver higher V_{OH} levels and are commonly used in wired-AND applications. These devices perform the Boolean functions $Y = \overline{A+B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The SN54ALS33A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS33A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

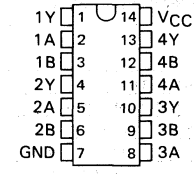
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol

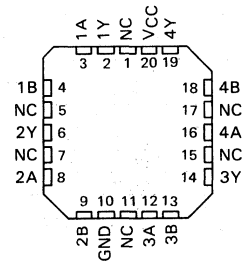


Pin numbers shown are for J and N packages.

SN54ALS33A . . . J PACKAGE
SN74ALS33A . . . N PACKAGE
SN74ALS33A . . . D PACKAGE
(TOP VIEW)



SN54ALS33A . . . FH OR FK PACKAGE
SN74ALS33A . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS33A . . . . . −55 °C to 125 °C
SN74ALS33A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS33A			SN74ALS33A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS33A			SN74ALS33A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		1.7	2.8		1.7	2.8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		5.6	9		5.6	9	mA

† All typical values are at V_{CC} = 5 V, T_A = 25 °C

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS33A		SN74ALS33A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	10	40	10	33	ns
t_{PHL}	A or B	Y	2	18	2	12	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D2261, DECEMBER 1983

- **Noninverters**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

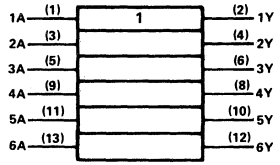
These devices contain six independent noninverters. They perform the Boolean functions Y = A.

The SN54ALS34 and SN54AS34 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS34 and SN74AS34 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each buffer)

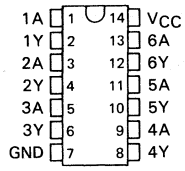
INPUT A	OUTPUT Y
H	H
L	L

logic symbol

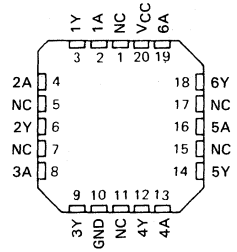


Pin numbers shown are for J and N packages.

SN54ALS34, SN54AS34 . . . J PACKAGE
SN74ALS34, SN74AS34 . . . N PACKAGE
SN74ALS34, SN74AS34 . . . D PACKAGE
(TOP VIEW)



SN54ALS34, SN54AS34 . . . FH OR FK PACKAGE
SN74ALS34, SN74AS34 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS34 . . . . . −55°C to 125°C
SN74ALS34 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS34			SN74ALS34			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS34			SN74ALS34			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		1			1		mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		3.5			3.5		mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS34			SN74ALS34			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y		8			8		ns
t_{PHL}				6			6		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS34 . . . . . −55 °C to 125 °C
SN74AS34 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS34			SN74AS34			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS34			SN74AS34			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		7.4	12		7.4	12	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		21.3	34.6		21.3	34.6	mA

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS34		SN74AS34		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	6.5	1	5.5	ns
t_{PHL}			1	7	1	6	

NOTE 1: For load circuit and voltage wavforms, see page 1-12.

D2661, DECEMBER 1983—REVISED MARCH 1984

- **Noninverters with Open-Collector Outputs**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

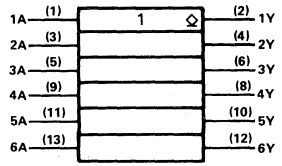
These devices contain six independent noninverters. They perform the Boolean functions Y = A. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS35 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS35 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each buffer)

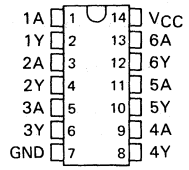
INPUT A	OUTPUT Y
H	H
L	L

logic symbol

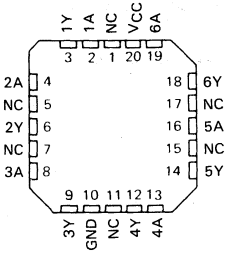


Pin numbers shown are for J and N packages.

SN54ALS35 . . . J PACKAGE
SN74ALS35 . . . N PACKAGE
SN74ALS35 . . . D PACKAGE
(TOP VIEW)



SN54ALS35 . . . FH OR FK PACKAGE
SN74ALS35 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

2

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS35 . . . . . −55 °C to 125 °C
SN74ALS35 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS35			SN74ALS35			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS35			SN74ALS35			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		2.7	4.1		2.7	4.1	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		4.1	6.3		4.1	6.3	mA

† All typical values are at V_{CC} = 5 V, T_A = 25 °C

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS35		SN74ALS35		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	20	55	20	50	ns
t_{PHL}	A	Y	2	15	2	12	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12

D2661, APRIL 1982—REVISED DECEMBER 1983

- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

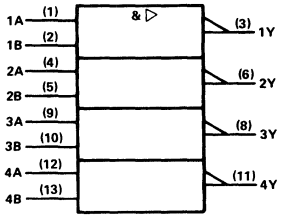
These devices contain four independent 2-input NAND buffer gates. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54ALS37A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS37A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each gate)

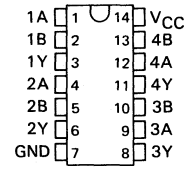
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol

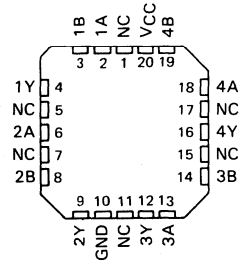


Pin numbers shown are for J and N packages.

SN54ALS37A . . . J PACKAGE
SN74ALS37A . . . N PACKAGE
SN74ALS37A . . . D PACKAGE
(TOP VIEW)



SN54ALS37A . . . FH OR FK PACKAGE
SN74ALS37A . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS37A . . . . . −55 °C to 125 °C
SN74ALS37A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS37A			SN74ALS37A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS37A			SN74ALS37A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_{IL} = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.86	1.6		0.86	1.6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		4.8	7.8		4.8	7.8	mA

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS37A		SN74ALS37A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2	10	2	8	ns
t_{PHL}	A or B	Y	2	10	2	7	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

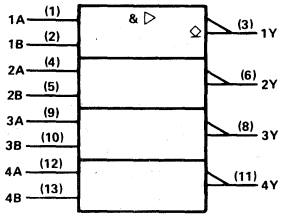
These devices contain four independent 2-input NAND buffer gates with open-collector outputs. These NAND buffers perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS38A is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS38A is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (each gate)

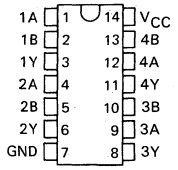
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol

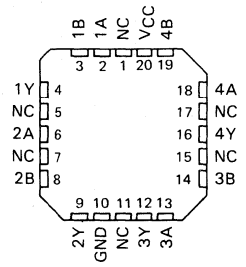


Pin numbers shown are for J and N packages.

SN54ALS38A . . . J PACKAGE
SN74ALS38A . . . N PACKAGE
SN74ALS38A . . . D PACKAGE
(TOP VIEW)



SN54ALS38A . . . FH OR FK PACKAGE
SN74ALS38A . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS38A . . . . . −55 °C to 125 °C
SN74ALS38A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS38A			SN74ALS38A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS38A			SN74ALS38A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.86	1.6		0.86	1.6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		4.8	7.8		4.8	7.8	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS38A		SN74ALS38A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	10	40	10	33	ns
t_{PHL}	A or B	Y	2	18	2	12	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D2661, APRIL 1982—REVISED DECEMBER 1982

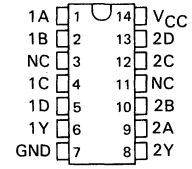
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain two independent 4-input NAND buffer gates. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

The SN54ALS40A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS40A is characterized for operation from 0°C to 70°C.

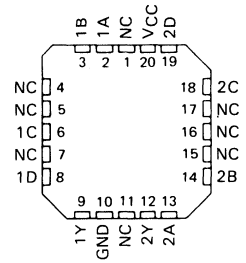
SN54ALS40A . . . J PACKAGE
SN74ALS40A . . . N PACKAGE
SN74ALS40A . . . D PACKAGE
(TOP VIEW)



FUNCTION TABLE (each gate)

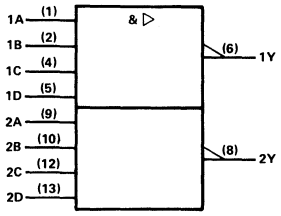
INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

SN54ALS40A . . . FH OR FK PACKAGE
SN74ALS40A . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS40A . . . . . −55 °C to 125 °C
SN74ALS40A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS40A			SN74ALS40A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS40A			SN74ALS40A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_{IL} = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.43	0.8		0.43	0.8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		2.4	3.9		2.4	3.9	mA

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

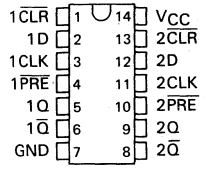
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS40A		SN74ALS40A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2	10	2	8	ns
t_{PHL}	A or B	Y	2	10	2	7	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY (C_L = 50 pF)	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'ALS74A	50 MHz	6 mW
'AS74	134 MHz	26 mW

SN54ALS74A, SN54AS74 . . . J PACKAGE
SN74ALS74A, SN74AS74 . . . N PACKAGE
SN74ALS74A, SN74AS74 . . . D PACKAGE
(TOP VIEW)



2

description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

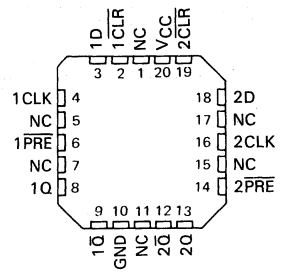
The SN54ALS74A and SN54AS74 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS74A and SN74AS74 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

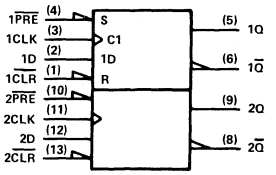
* The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at Preset and Clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

SN54ALS74A, SN54AS74 . . . FH OR FK PACKAGE
SN74ALS74A, SN74AS74 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS74A, SN54AS74 . . . . . −55°C to 125°C
SN74ALS74A, SN74AS74 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS74A			SN74ALS74A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		30	0		34	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	15			15			ns
		CLK high	16.5			14.5			
		CLK low	16.5			14.5			
t_{su}	Setup time before CLK↑	Data	15			15			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	10			10			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS74A			SN74ALS74A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	CLK or D	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	$\overline{PRE}$ or $\overline{CLR}$					0.2			0.2	
I_{IH}	CLK or D	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	$\overline{PRE}$ or $\overline{CLR}$					40			40	
I_{IL}	CLK or D	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	$\overline{PRE}$ or $\overline{CLR}$					−0.4			−0.4	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		2.4	4		2.4	4	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with D, CLK, and $\overline{PRE}$ grounded, then with D, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS74A		SN74ALS74A		
			MIN	MAX	MIN	MAX	
f_{max}			30		34		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	3	15	3	13	ns
t_{PHL}			5	17	5	15	
t_{PLH}	CLK	Q or $\overline{Q}$	5	18	5	16	ns
t_{PHL}			5	20	5	18	

NOTE 2: For load circuit and voltage waveforms, see page 1-12

recommended operating conditions

			SN54AS74			SN74AS74			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0		90	0		105	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	4			4			ns
		CLK high	4			4			
		CLK low	5.5			5.5			
t_{su}	Setup time before CLK↑	Data	4.5			4.5			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2			2			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS74			SN74AS74			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	CLK or D	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	$\overline{PRE}$ or $\overline{CLR}$					40			40	
I_{IL}	CLK or D	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	$\overline{PRE}$ or $\overline{CLR}$					−1.8			−1.8	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	See Note 1		10.5	16		10.5	16	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-current output current, I_{OS}.
NOTE 1: I_{CC} is measured with D, CLK, and $\overline{PRE}$ grounded, then with D, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see Note 2)

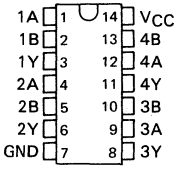
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS74		SN74AS74		
			MIN	MAX	MIN	MAX	
f_{max}			90		105		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	3	8.5	3	7.5	ns
t_{PHL}			3.5	11.5	3.5	10.5	
t_{PLH}	CLK	Q or $\overline{Q}$	3.5	9	3.5	8	ns
t_{PHL}			4.5	10.5	4.5	9	

NOTE 2: For load circuit and voltage wavforms, see page 1-12

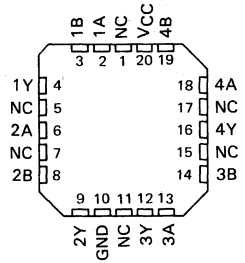
D2661, APRIL 1982—REVISED MARCH 1984

- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS86 . . . J PACKAGE
SN74ALS86 . . . N PACKAGE
SN74ALS86 . . . D PACKAGE
(TOP VIEW)



SN54ALS86 . . . FH OR FK PACKAGE
SN74ALS86 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

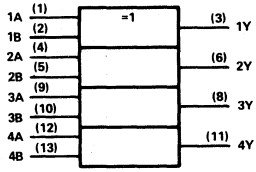
description

These devices contain four independent 2-input Exclusive-OR gates. They perform the Boolean functions $Y = A \oplus B = \overline{A}B + A\overline{B}$ in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input will be reproduced in true form at the output. If one of the inputs is high, the signal on the other input will be reproduced inverted at the output.

The SN54ALS86 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS86 is characterized for operation from 0°C to 70°C.

logic symbol



Pin numbers shown are for J and N packages.

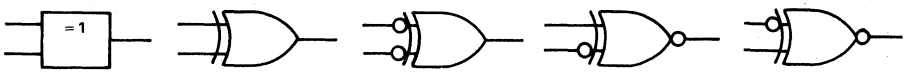
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

exclusive-OR logic

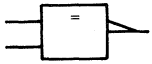
An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE-OR



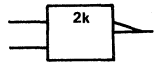
These are five equivalent Exclusive-OR symbols valid for an 'ALS86 gate in positive logic; negation may be shown at any two ports.

LOGIC IDENTITY ELEMENT



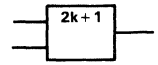
The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

EVEN-PARITY



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS86 . . . . . −55 °C to 125 °C
SN74ALS86 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS86			SN74ALS86			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS86			SN74ALS86			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V,	All inputs at 4.5 V		3.9	5.9		3.9	5.9	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

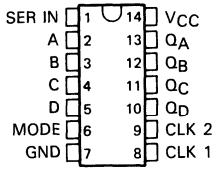
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS86		SN74ALS86		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	3	22	3	17	ns
t_{PHL}	(other input low)		2	14	2	12	
t_{PLH}	A or B	Y	3	22	3	17	ns
t_{PHL}	(other input high)		2	12	2	10	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

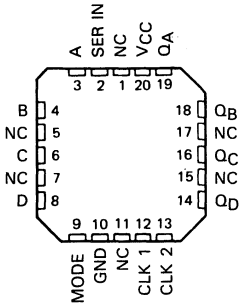
D2661, DECEMBER 1983—REVISED FEBRUARY 1984

- **Serial-to-Parallel Conversions**
- **Parallel Synchronous Loading**
- **Right or Left Shifts**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS95 . . . J PACKAGE
SN74AS95 . . . N PACKAGE
SN74AS95 . . . D PACKAGE
(TOP VIEW)



SN54AS95 . . . FH OR FK PACKAGE
SN74AS95 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

These four-bit registers feature parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The registers have three modes of operation:

Parallel (broadside) load
Shift right (the direction Q_A toward Q_D)
Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the Clock-2 input. During loading, the entry of serial data is inhibited.

Shift right is accomplished on the high-to-low transition of Clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of Clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.); and serial data is entered at input D. The clock input may be applied commonly to Clock 1 and Clock 2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low. However, conditions described in the last three lines of the function table will also ensure that the register contents are protected.

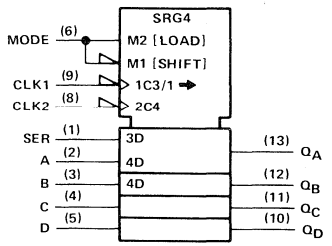
The SN54AS95 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS95 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

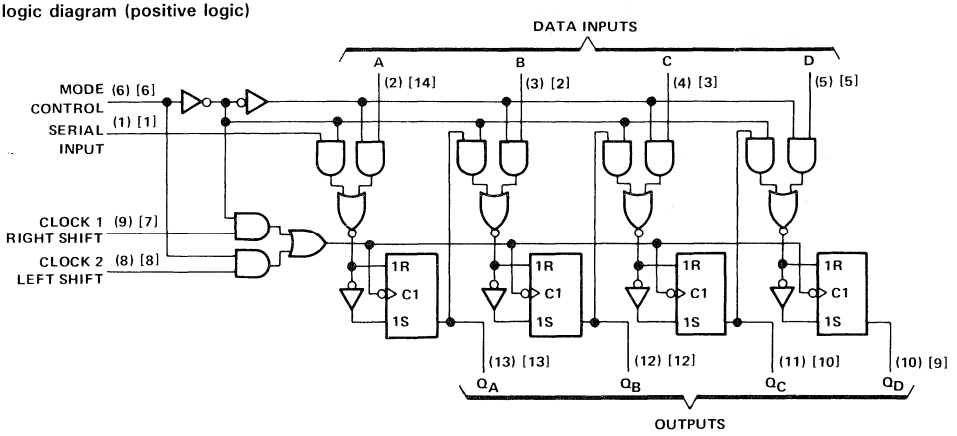
INPUTS								OUTPUTS			
MODE	CLOCKS		SERIAL	PARALLEL				Q_A	Q_B	Q_C	Q_D
CONTROL	2 (L)	1 (R)		A	B	C	D				
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

†Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.
H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions).
↓ = transition from high to low level, ↑ = transition from low to high level.
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most-recent ↓ transition of the clock.

logic symbol



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS95 . . . . . −55°C to 125°C
SN74AS95 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS95			SN74AS85			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0		100	0		100	MHz
t_w	Pulse duration, CLK high or low		5			5			ns
t_{su}	Setup time, data before CLK↓		2.5			2			ns
t_h	Hold time after CLK↓ (see Figure 1)	Data	2.5			2.5			ns
		CLK 1 to Mode	3.5			3			
		CLK 2 to Mode	1			0			
t_{en}	Clock enable time (see Figure 1)	CLK 1	13			12			ns
		CLK 2	13			12			
t_{in}	Clock inhibit time (see Figure 1)	CLK 1	3			2.5			ns
		CLK 2	1			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS95			SN74AS95			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	Mode	V_{CC} = 5.5 V,	V_{IL} = 0.4 V			−1			−1	mA
	All other					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.35 V	−30		−112	−30		−112	mA
I_{CCH}		V_{CC} = 5.5 V			21	34		21	34	mA
I_{CCL}		V_{CC} = 5.5 V			26	39		26	39	mA

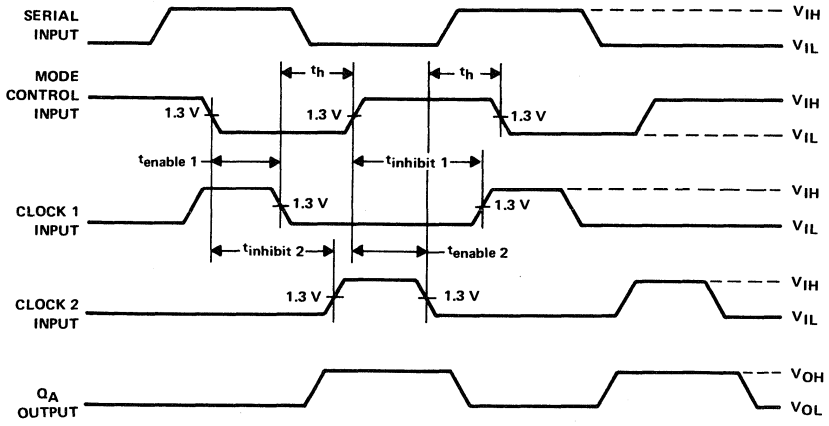
†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristice (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS95		SN74AS95		
			MIN	MAX	MIN	MAX	
f_{max}			100		100		MHz
t_{PLH}	CLK	Q	2	11	2	10	ns
t_{PHL}			2	10.5	2	9.5	

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of the TTL Data Book, Volume 2.

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

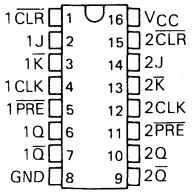
NOTES: A. Input A is at a low level.
B. V_{IH} = 3.5 V, V_{IL} = 0.3 V.

FIGURE 1–CLOCK ENABLE, INHIBIT, AND HOLD TIMES

- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'ALS109A	50 MHz	6 mW
'AS109	129 MHz	29 mW

SN54ALS109A, SN54AS109 . . . J PACKAGE
SN74ALS109A, SN74AS109 . . . N PACKAGE
SN74ALS109A, SN74AS109 . . . D PACKAGE
(TOP VIEW)



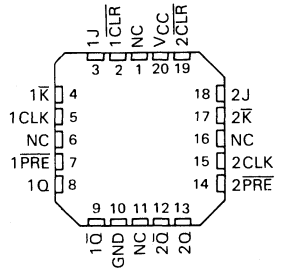
2

description

These devices contain two independent J-$\overline{K}$ positive-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and $\overline{K}$ input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and $\overline{K}$ inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding $\overline{K}$ and trying J high. They also can perform as D-type flip-flops if J and $\overline{K}$ are tied together.

The SN54ALS109A and SN54AS109 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS109A and SN74AS109 are characterized for operation from 0°C to 70°C.

SN54ALS109A, SN54AS109 . . . FH OR FK PACKAGE
SN74ALS109A, SN74AS109 . . . FN PACKAGE
(TOP VIEW)



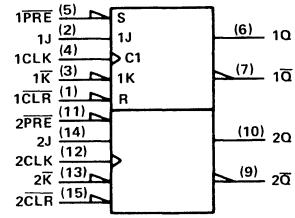
NC—No internal connection

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

* The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at Preset and Clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS109A, SN54AS109 . . . . . −55°C to 125°C
SN74ALS109A, SN74AS109 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS109A			SN74ALS109A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		30	0		34	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	15			15			ns
		CLK high	16.5			14.5			
		CLK low	16.5			14.5			
t_{su}	Setup time before CLK↑	Data	15			15			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	10			10			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS109A			SN74ALS109A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	CLK, J, or $\overline{K}$	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	$\overline{PRE}$ or $\overline{CLR}$					0.2			0.2	
I_{IH}	CLK, J, or $\overline{K}$	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	$\overline{PRE}$ or $\overline{CLR}$					40			40	
I_{IL}	CLK, J or $\overline{K}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	$\overline{PRE}$ or $\overline{CLR}$					−0.4			−0.4	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		2.4	4		2.4	4	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with J, $\overline{K}$, CLK, and $\overline{PRE}$ grounded, then with J, $\overline{K}$, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS109A		SN74ALS109A		
			MIN	MAX	MIN	MAX	
f_{max}			30		34		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	3	15	3	13	ns
t_{PHL}			5	17	5	15	
t_{PLH}	CLK	Q or $\overline{Q}$	5	18	5	16	ns
t_{PHL}			5	20	5	18	

NOTE 2: For load circuit and voltage waveforms, see page 1-12

recommended operating conditions

			SN54AS109			SN74AS109			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0		90	0		105	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	4			4			ns
		CLK high	4			4			
		CLK low	5.5			5.5			
t_{su}	Setup time before CLK↑	Data	5.5			5.5			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2			2			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS109			SN74AS109			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	CLK, J or $\overline{K}$	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	$\overline{PRE}$ or $\overline{CLR}$					40			40	
I_{IL}	CLK, J or $\overline{K}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			0.5	mA
	$\overline{PRE}$ or $\overline{CLR}$					−1.8			−1.8	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		11.5	17		11.5	17	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with J, $\overline{K}$, CLK, and $\overline{PRE}$ grounded, then with J, $\overline{K}$, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS109		SN74AS109		
			MIN	MAX	MIN	MAX	
f_{max}			90		105		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	3	9	3	8	ns
t_{PHL}			3.5	11.5	3.5	10.5	
t_{PLH}	CLK	Q or $\overline{Q}$	3.5	10	3.5	9	ns
t_{PHL}			4.5	10.5	4.5	9	

NOTE 2: For load circuit and voltage wavforms, see page 1-12

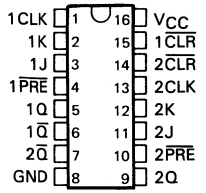
TYPES SN54ALS112A, SN54AS112, SN74ALS112A, SN74AS112
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

D2661, APRIL 1982—REVISED DECEMBER 1983

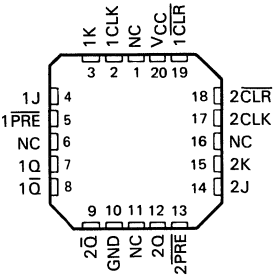
- **Fully Buffered to Offer Maximum Isolation from External Disturbance**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'ALS112A	50 MHz	6 mW
'AS112	175 MHz	95 mW

SN54ALS112A, SN54AS112 . . . J PACKAGE
SN74ALS112A, SN74AS112 . . . N PACKAGE
SN74ALS112A, SN74AS112 . . . D PACKAGE
(TOP VIEW)



SN54ALS112A, SN54AS112 . . . FH OR FK PACKAGE
SN74ALS112A, SN74AS112 . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

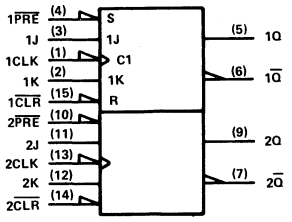
The SN54ALS112A and SN54AS112 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS112A and SN74AS112 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

*The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at Preset and Clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS112A, SN54AS112 . . . . . −55°C to 125°C
SN74ALS112A, SN74AS112 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS112A			SN74ALS112A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		25	0		30	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	15			10			ns
		CLK high	20			16.5			
		CLK low	20			16.5			
t_{su}	Setup time before CLK↓	Data	25			22			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	22			20			
t_h	Hold time, data after CLK↓		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS112A			SN74ALS112A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	$\overline{PRE}$ or $\overline{CLR}$					0.2			0.2	
I_{IH}	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	$\overline{PRE}$ or $\overline{CLR}$					40			40	
I_{IL}	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	$\overline{PRE}$ or $\overline{CLR}$					−0.4			−0.4	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		2.5	4.5		2.5	4.5	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with J, K, CLK, and $\overline{PRE}$ grounded, then with J, K, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS112A		SN74ALS112A		
			MIN	MAX	MIN	MAX	
f_{max}			25		30		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	3	20	3	15	ns
t_{PHL}			4	22	4	18	
t_{PLH}	CLK	Q or $\overline{Q}$	3	18	3	15	ns
t_{PHL}			5	23	5	19	

NOTE 2: For load circuit and voltage waveforms, see page 1-12.

recommended operating conditions

			SN54AS112			SN74AS112			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0			0			MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low							ns
		CLK high							
		CLK low							
t_{su}	Setup time before CLK↓	Data							ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive							
t_h	Hold time, data after CLK↓								ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS112			SN74AS112			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	J or K	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	$\overline{PRE}$ or $\overline{CLR}$					0.5			0.5	
	CLK					0.5			0.5	
I_{IH}	J or K	V_{CC} = 5.5 V,	V_I = 2.7 V			0.02			0.02	mA
	$\overline{PRE}$ or $\overline{CLR}$					0.1			0.1	
	CLK					0.1			0.1	
I_{IL}	J or K	V_{CC} = 5.5 V,	V_I = 0.4 V		−1			−1		mA
	$\overline{PRE}$ or $\overline{CLR}$				−5.5			−5.5		
	CLK				−5			−5		
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		38			38		mA

NOTE 1: I_{CC} is measured with D, CLK, and PRE grounded, then with J, K, CLK, and $\overline{PRE}$ grounded, with K, K, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS112			SN74AS112			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}				175			175		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$		3			3		ns
t_{PHL}				4			4		
t_{PLH}	CLK	Q or $\overline{Q}$		3			3		ns
t_{PHL}				4			4		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 2: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

PRODUCT PREVIEW

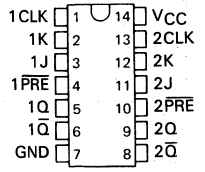
TYPES SN54ALS113A, SN54AS113, SN74ALS113A, SN74AS113
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

D2661, APRIL 1982—REVISED DECEMBER 1983

- **Fully Buffered to Offer Maximum Isolation from External Disturbance**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'ALS113A	40 MHz (C_L = 15 pF)	6 mW
'AS113	175 MHz (C_L = 50 pF)	95 mW

SN54ALS113A, SN54AS113 . . . J PACKAGE
SN74ALS113A, SN74AS113 . . . N PACKAGE
SN74ALS113A, SN74AS113 . . . D PACKAGE
(TOP VIEW)



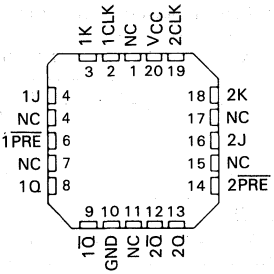
2

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset input sets the outputs regardless of the levels of the other inputs. When Preset ($\overline{PRE}$) is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54ALS113A and SN54AS113 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS113A and SN74AS113 are characterized for operation from 0°C to 70°C.

SN54ALS113A, SN54AS113 . . . FH OR FK PACKAGE
SN74ALS113A, SN74AS113 . . . FN PACKAGE
(TOP VIEW)

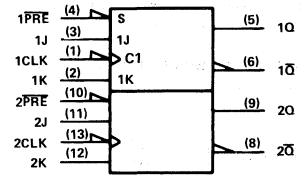


NC — No internal connection

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	H	L
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q}_0$

logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS113A, SN54AS113 . . . . . −55°C to 125°C
SN74ALS113A, SN74AS113 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS113A			SN74ALS113A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		25	0		30	MHz
t_w	Pulse duration	$\overline{PRE}$ low	15			10			ns
		CLK high	20			16.5			
		CLK low	20			16.5			
t_{su}	Setup time before CLK↓	Data	25			22			ns
		$\overline{PRE}$ inactive	22			20			
t_h	Hold time, data after CLK↓		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS113A			SN74ALS113A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	$\overline{PRE}$					0.2			0.2	
I_{IH}	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	$\overline{PRE}$					40			40	
I_{IL}	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	$\overline{PRE}$					−0.4			−0.4	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		2.5	4.5		2.5	4.5	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with J, K, CLK, and $\overline{PRE}$ grounded, then with J, K, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS113A		SN74ALS113A		
			MIN	MAX	MIN	MAX	
f_{max}			25		30		MHz
t_{PLH}	$\overline{PRE}$	Q or $\overline{Q}$	3	17	3	14	ns
t_{PHL}			4	20	4	16	
t_{PLH}	CLK	Q or $\overline{Q}$	3	18	3	15	ns
t_{PHL}			5	23	5	19	

NOTE 2: For load circuit and voltage waveforms, see page 1-12.

recommended operating conditions

			SN54AS113			SN74AS113			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0			0			MHz
t_w	Pulse duration	$\overline{PRE}$ low							ns
		CLK high							
		CLK low							
t_{su}	Setup time before CLK↓	Data							ns
		$\overline{PRE}$ inactive							
t_h	Hold time, data after CLK↓								ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS113			SN74AS113			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	J or K	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	$\overline{PRE}$					0.5			0.5	
	CLK					0.5			0.5	
I_{IH}	J or K	V_{CC} = 5.5 V,	V_I = 2.7 V			0.02			0.02	mA
	$\overline{PRE}$					0.1			0.1	
	CLK					0.1			0.1	
I_{IL}	J or K	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	$\overline{PRE}$					−5.5			−5.5	
	CLR					−5			−5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		38			38		mA

NOTE 1: I_{CC} is measured with D, CLK, and $\overline{PRE}$ grounded, then with D, CLK, and CLR grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS113			SN74AS113			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}				175			175		MHz
t_{PLH}	$\overline{PRE}$	Q or $\overline{Q}$		3			3		ns
t_{PHL}				4			4		
t_{PLH}	CLK	Q or $\overline{Q}$		3			3		ns
t_{PHL}				4			4		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 2: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

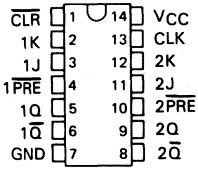
TYPES SN54ALS114A, SN54AS114, SN74ALS114A, SN74AS114
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

D2661, APRIL 1982—REVISED DECEMBER 1983

- **Fully Buffered to Offer Maximum Isolation from External Disturbance**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'ALS114A	40 MHz (C_L = 15 pF)	6 mW
'AS114	175 MHz (C_L = 50 pF)	95 mW

SN54ALS114A, SN54AS114 . . . J PACKAGE
SN74ALS114A, SN74AS114 . . . N PACKAGE
SN74ALS114A, SN74AS114 . . . D PACKAGE
(TOP VIEW)



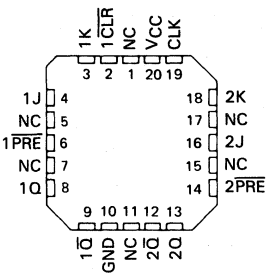
2

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54ALS114A and SN54AS114 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS114A and SN74AS114 are characterized for operation from 0°C to 70°C.

SN54ALS114A, SN54AS114 . . . FH OR FK PACKAGE
SN74ALS114A, SN74AS114 . . . FN PACKAGE
(TOP VIEW)



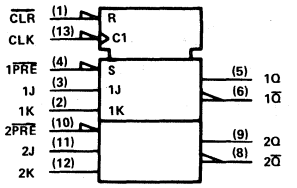
NC — No internal connection

FUNCTION TABLE

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$

*The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at Preset and Clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS114A, SN54AS114 . . . . . −55°C to 125°C
SN74ALS114A, SN74AS114 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS114A			SN74ALS114A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		25	0		30	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	15			10			ns
		CLK high	20			16.5			
		CLK low	20			16.5			
t_{su}	Setup time before CLK↓	Data	25			22			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	22			20			
t_h	Hold time, data after CLK↓		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteistics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS114A			SN74ALS114A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4				V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	$\overline{PRE}$ or $\overline{CLR}$					0.2			0.2	
I_{IH}	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	$\overline{PRE}$ or $\overline{CLR}$					40			40	
I_{IL}	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	$\overline{PRE}$ or $\overline{CLR}$					−0.4			−0.4	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		2.5	4.5		2.5	4.5	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with J, K, CLK, and $\overline{PRE}$ grounded, then with J, K, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS114A		SN74ALS114A		
			MIN	MAX	MIN	MAX	
f_{max}			25		30		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	3	20	3	15	ns
t_{PHL}			4	22	4	18	
t_{PLH}	CLK	Q or $\overline{Q}$	3	18	3	15	ns
t_{PHL}			5	23	5	19	

NOTE 2: For load circuit and voltage waveforms, see page 1-12.

recommended operating conditions

			SN54AS114			SN74AS114			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0			0			MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low							ns
		CLK high							
		CLK low							
t_{su}	Setup time before CLK↓	Data							ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive							
t_h	Hold time, data after CLK↓								ns
T_A	Operating free-air temperature		−55		125	0		70	°C

2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS114			SN74AS114			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	J or K	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	$\overline{PRE}$					0.5			0.5	
	$\overline{CLR}$					1			1	
	CLK					1			1	
I_{IH}	J or K	V_{CC} = 5.5 V,	V_I = 2.7 V			0.02			0.02	mA
	$\overline{PRE}$					0.1			0.1	
	$\overline{CLR}$					0.2			0.2	
	CLK					0.2			0.2	
I_{IL}	J or K	V_{CC} = 5.5 V,	V_I = 0.4 V		−1			−1		mA
	$\overline{PRE}$				−5.5			−5.5		
	$\overline{CLR}$				−11.5			−11.5		
	CLK				−10.5			−10.5		
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		38			38		mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with J, K, CLK,and $\overline{PRE}$ grounded, then with J, K, CLK, and $\overline{CLR}$ grounded.

Additional information on these products can be obtained from the factory as it becomes available.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS114			SN74AS114			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}				175			175		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$		3			3		ns
t_{PHL}				4			4		
t_{PLH}	CLK	Q or $\overline{Q}$		3			3		ns
t_{PHL}				4			4		

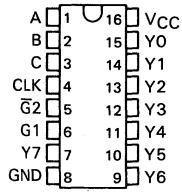
†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: For load circuit and voltage waveforms, see page 1-12.

TYPES SN54ALS131, SN54AS131, SN74ALS131, SN74AS131
3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS REGISTERS

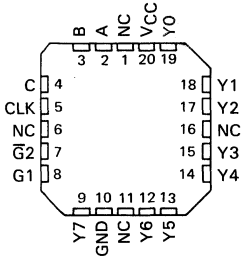
D2661, APRIL 1982—REVISED DECEMBER 1983

- **Combines Decoder and 3-Bit Address Register**
- **Incorporates 2 Enable Inputs to Simplify Cascading**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS131, SN54AS131 . . . J PACKAGE
SN74ALS131, SN74AS131 . . . N PACKAGE
SN74ALS131, SN74AS131 . . . D PACKAGE
(TOP VIEW)



SN54ALS131, SN54AS131 . . . FH OR FK PACKAGE
SN74ALS131, SN74AS131 . . . FN PACKAGE
(TOP VIEW)



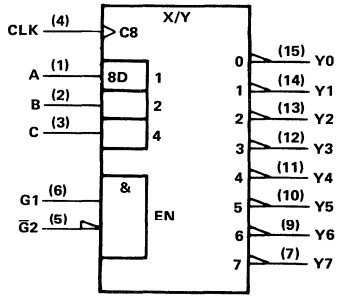
NC — No internal connection

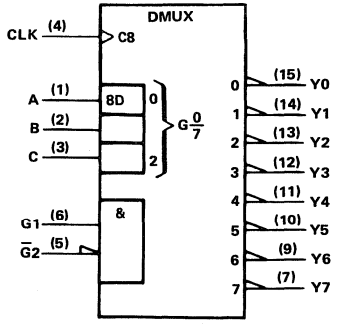
description

The 'ALS131 and 'AS131 are three-line to eight-line decoders/demultiplexers with registers on the three address inputs. When the clock input (CLK) goes from low to high, the 'ALS131 and 'AS131 act as decoders/demultiplexers and the address present at the select inputs (A, B, and C) is stored in the registers. Further address changes are ignored until the next transition of CLK. The output enable controls, G1 and $\overline{G}2$, control the state of the outputs independently of the select or CLK inputs. All of the outputs are high unless G1 is high and $\overline{G}2$ is low. The 'ALS131 and 'AS131 are ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

The SN54ALS131 and SN54AS131 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS131 and SN74AS131 are characterized for operation from 0°C to 70°C.

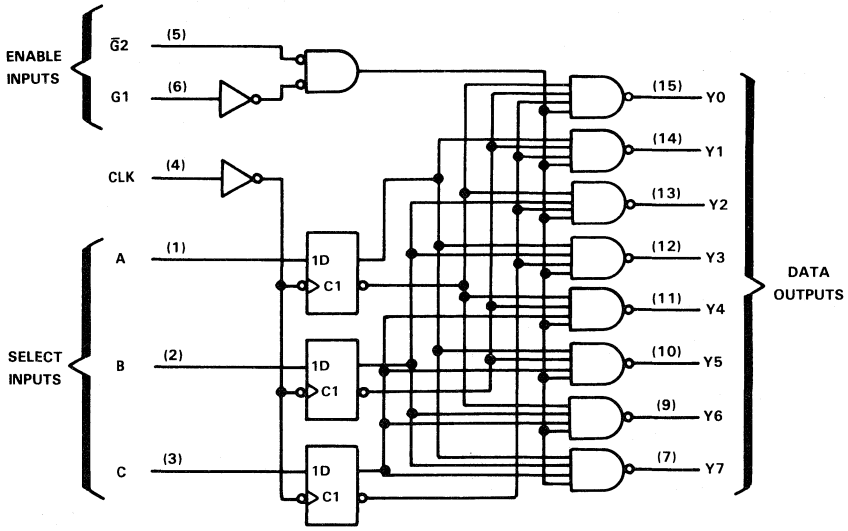
logic symbols (alternatives)





Pin numbers shown are for J and N packages.

logic diagram (positive logic)



Pin numbers shown are for J and N packages.

FUNCTION TABLE

INPUTS						OUTPUTS							
CLK	ENABLE		SELECT										
	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
↑	H	L	L	L	L	L	H	H	H	H	H	H	H
↑	H	L	L	L	H	H	L	H	H	H	H	H	H
↑	H	L	L	H	L	H	H	L	H	H	H	H	H
↑	H	L	L	H	H	H	H	H	L	H	H	H	H
↑	H	L	H	L	L	H	H	H	H	L	H	H	H
↑	H	L	H	L	H	H	H	H	H	H	L	H	H
↑	H	L	H	H	L	H	H	H	H	H	H	L	H
↑	H	L	H	H	H	H	H	H	H	H	H	H	L
L or H	H	L	X	X	X	OUTPUTS CORRESPONDING TO STORED ADDRESS, L; ALL OTHERS, H							

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS131, SN54AS131 . . . . . −55°C to 125°C
SN74ALS131, SN74AS131 . . . . . 0°C to 70°C
Storage temperature . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS131			SN74ALS131			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		40	0		50	MHz
t_w	Pulse duration	CLK high	12.5			10			ns
		CLK low	12.5			10			
t_{su}	Setup time at A, B, and C before CLK↑		15			10			ns
t_h	Hold time at A, B, and C after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS131			SN74ALS131			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			5	11		5	11	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS131		SN74ALS131		
			MIN	MAX	MIN	MAX	
f_{max}			40		50		MHz
t_{PLH}	CLK	Y	8	28	8	25	ns
t_{PHL}			7	24	7	20	
t_{PLH}	G1	Y	7	24	7	20	ns
t_{PHL}			6	20	6	17	
t_{PLH}	$\overline{G}2$	Y	5	18	5	15	ns
t_{PHL}			5	18	5	15	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

recommended operating conditions

			SN54AS131			SN74AS131			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	CLK high							ns
		CLK low							
t_{su}	Setup time at A, B, and C before CLK↑								ns
t_h	Hold time at A, B, and C after CLK↑								ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS131			SN74AS131			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V							mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V							μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V							mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			16			16		mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS131			SN74AS131			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}									MHz
t_{PLH}	CLK	Y		5.4			5.4		ns
t_{PHL}				5.3			5.3		
t_{PLH}	G1	Y		6.2			6.2		ns
t_{PHL}				5.6			5.6		
t_{PLH}	$\overline{G}2$	Y		5.4			5.4		ns
t_{PHL}				5.3			5.3		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain a single 13-input NAND gate. They perform the boolean functions in positive logic:

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot I \cdot J \cdot K \cdot L \cdot M}$$

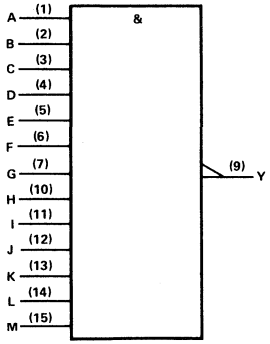
$$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H} + \overline{I} + \overline{J} + \overline{K} + \overline{L} + \overline{M}$$

The SN54ALS133 is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS133 is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE

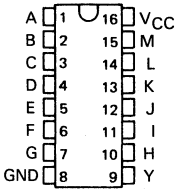
INPUTS A THRU M	OUTPUT Y
All inputs H	L
One or more inputs L	H

logic symbol

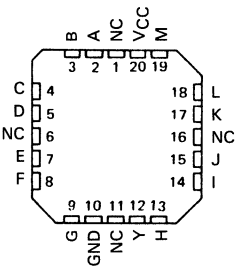


Pin numbers shown are for J and N packages.

SN54ALS133 . . . J PACKAGE
SN74ALS133 . . . N PACKAGE
SN74ALS133 . . . D PACKAGE
(TOP VIEW)



SN54ALS133 . . . FH OR FK PACKAGE
SN74ALS133 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS133 . . . . . −55°C to 125°C
SN74ALS133 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS133			SN74ALS133			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS133			SN74ALS133			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.24	0.34		0.24	0.34	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		0.56	0.8		0.56	0.8	mA

†All typical values aree at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

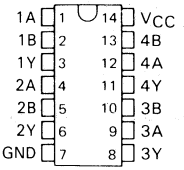
switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS133		SN74ALS133		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	3	14	3	11	ns
t_{PHL}	Any	Y	5	28	5	25	ns

NOTE 2: For load circuit and voltage waveforms, see page 1-12.

- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS136 . . . J PACKAGE
SN74ALS136 . . . N PACKAGE
SN74ALS136 . . . D PACKAGE
(TOP VIEW)



2

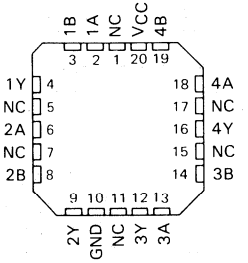
description

These devices contain four independent Exclusive-OR gates with open-collector outputs. They perform the Boolean functions $Y = A \oplus B = \overline{A}B + A\overline{B}$ in positive logic.

A common application is a true/complement element. If one of the inputs is low, the other input will be reproduced in true form at the output. If one of the inputs is high, the signal on the other input will be reproduced inverted at the output.

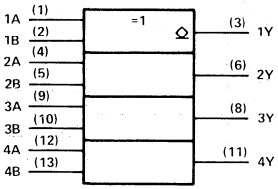
The SN54ALS136 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS136 is characterized for operation from 0°C to 70°C.

SN54ALS136 . . . FH OR FK PACKAGE
SN74ALS136 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

logic symbol



Pin numbers shown are for J and N packages.

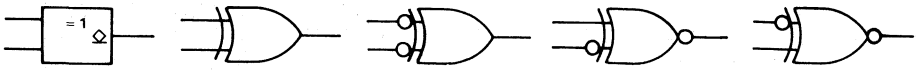
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

exclusive-OR logic

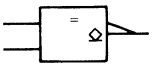
An Exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE-OR



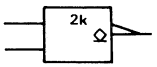
These are five equivalent Exclusive-OR symbols valid for an 'ALS136 gate in positive logic; negation may be shown at any two ports.

LOGIC IDENTITY ELEMENT



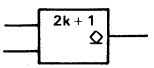
The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

EVEN-PARITY



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS136 . . . . . −55°C to 125°C
SN74ALS136 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS136			SN74ALS136			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS136			SN74ALS136			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CC}	V_{CC} = 5.5 V,	All inputs at 4.5 V		3.9	5.9		3.9	5.9	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Note 1)

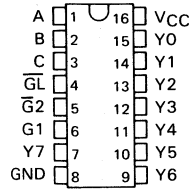
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = MIN to MAX				UNIT
			SN54ALS136		SN74ALS136		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	20	55	20	50	ns
t_{PHL}	(other input low)		3	18	3	15	
t_{PLH}	A or B	Y	20	55	20	50	ns
t_{PHL}	(other input high)		3	15	3	12	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

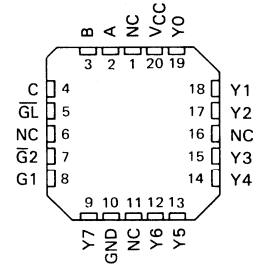
D2661, APRIL 1982—REVISED DECEMBER 1983

- **Combines Decoder and 3-Bit Address Latch**
- **Incorporates 2 Output Enables to Simplify Cascading**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS137, SN54AS137 . . . J PACKAGE
SN74ALS137, SN74AS137 . . . N PACKAGE
SN74ALS137, SN74AS137 . . . D PACKAGE
(TOP VIEW)



SN54ALS137, SN54AS137 . . . FH OR FK PACKAGE
SN74ALS137, SN74AS137 . . . FN PACKAGE
(TOP VIEW)



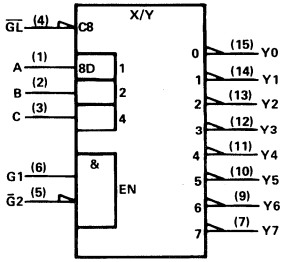
NC — No internal connection

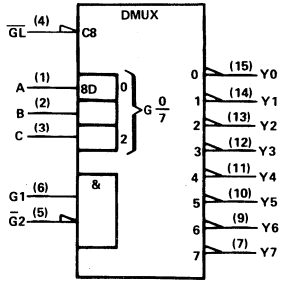
description

The 'ALS137 and 'AS137 are three-line to eight-line decoder/demultiplexer with latches on the three address inputs. When the latch-enable input ($\overline{GL}$) is low, the 'ALS137 and 'AS137 acts as a decoder/demultiplexer. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A, B, and C) is stored in the latches. Further address changes are ignored as long as $\overline{GL}$ remains high. The output enable controls, G1 and $\overline{G2}$, control the outputs independently of the select or latch-enable inputs. All of the outputs are forced high if G1 is low or $\overline{G2}$ is high. The 'ALS137 and 'AS137 are ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

The SN54ALS137 and SN54AS137 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS137 and SN74AS137 are characterized for operation from 0°C to 70°C.

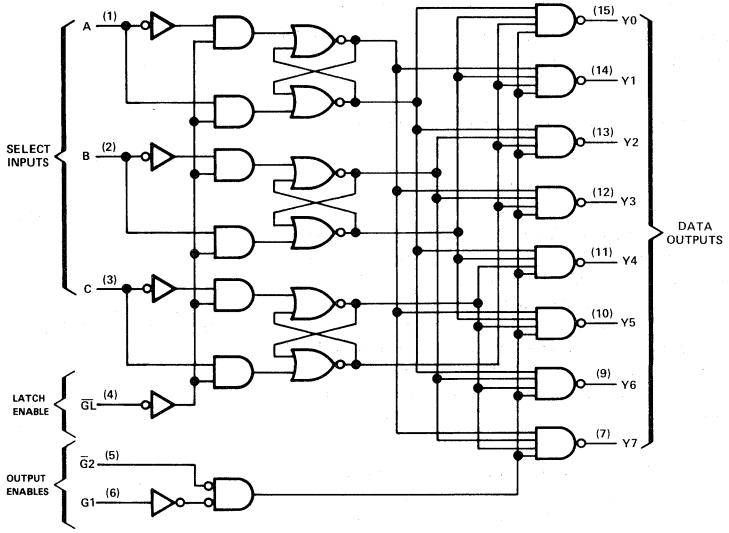
logic symbols (alternatives)





Pin numbers shown are for J and N packages.

logic diagram (positive logic)



Pin numbers shown are for J and N packages.

FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{GL}$	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output corresponding to stored address, L; all others, H							

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS137, SN54AS137 . . . . . −55°C to 125°C
SN74ALS137, SN74AS137 . . . . . 0°C to 70°C
Storage temperature . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS137			SN74ALS137			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
t_w	Pulse duration, $\overline{GL}$ low	15			10			ns
t_{su}	Setup time at A, B, and C before $\overline{GL}$↑	15			10			ns
t_h	Hold time at A, B, and C after $\overline{GL}$↑	5			5			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS137			SN74ALS137			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			5	11		5	11	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS137		SN74ALS137		
			MIN	MAX	MIN	MAX	
t_{PLH}	A, B, C	Y	5	25	5	20	ns
t_{PHL}			6	25	6	20	
t_{PLH}	$\overline{G2}$	Y	4	15	4	12	ns
t_{PHL}			5	18	5	15	
t_{PLH}	G1	Y	5	21	5	17	ns
t_{PHL}			5	19	5	15	
t_{PLH}	$\overline{GL}$	Y	7	27	7	22	ns
t_{PHL}			7	25	7	20	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

recommended operating conditions

		SN54AS137			SN74AS137			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
t_w	Pulse duration, $\overline{GL}$ low							ns
t_{su}	Setup times at A, B, and C before $\overline{GL}$↑							ns
t_h	Hold time at A, B, and C after $\overline{GL}$↑							ns
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS137			SN74AS137			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	Enable	V_{CC} = 5.5 V,	V_I = 7 V							mA
	A, B, C									
I_{IH}	Enable	V_{CC} = 5.5 V,	V_I = 2.7 V							μA
	A, B, C									
I_{IL}	Enable	V_{CC} = 5.5 V,	V_I = 0.4 V		−0.05			−0.05		mA
	A, B, C				−0.05			−0.05		
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			16			16		mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS137			SN74AS137			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A, B, C	Y		6.6			6.6		ns
t_{PHL}				7.1			7.1		
t_{PLH}	$\overline{G}2$	Y		5.4			5.4		ns
t_{PHL}				5.3			5.3		
t_{PLH}	G1	Y		6.2			6.2		ns
t_{PHL}				5.6			5.6		
t_{PLH}	$\overline{GL}$	Y		5.4			5.4		ns
t_{PHL}				5.3			5.3		

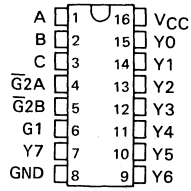
†All typical values are at V_{CC} 5 V, T_A = 25°C.

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

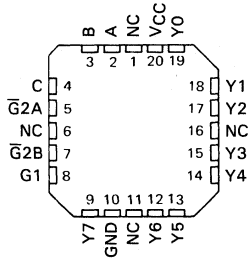
D2661, APRIL 1982—REVISED DECEMBER 1983

- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporates 3 Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS138, SN54AS138 . . . J PACKAGE
SN74ALS138, SN74AS138 . . . N PACKAGE
SN74ALS138, SN74AS138 . . . D PACKAGE
(TOP VIEW)



SN54ALS138, SN54AS138 . . . FH OR FK PACKAGE
SN74ALS138, SN74AS138 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

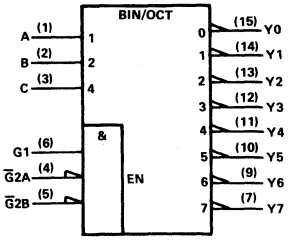
description

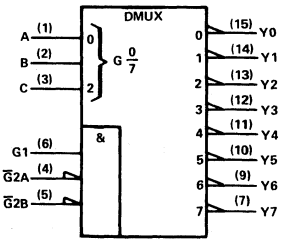
The 'ALS138 and 'AS138 circuits are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decorders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

The conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The SN54ALS138 and SN54AS138 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS138 and SN74AS138 are characterized for operation from 0°C to 70°C.

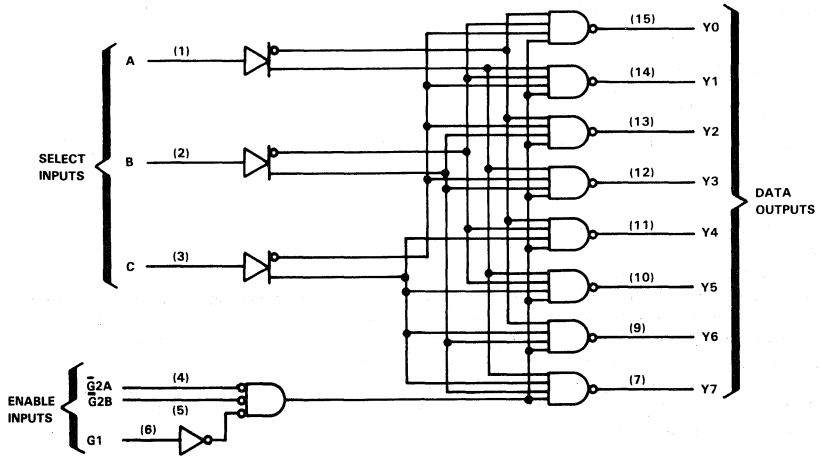
logic symbols (alternatives)





Pin numbers shown are for J and N packages.

logic diagram (positive logic)



Pin numbers shown are for J and N packages.

FUNCTION TABLE

ENABLE INPUTS		SELECT INPUTS			OUTPUTS							
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*$\overline{G2} = \overline{G2A} + \overline{G2B}$

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS138, SN54AS138 . . . . . −55°C to 125°C
SN74ALS138, SN74AS138 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS138			SN74ALS138			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS138			SN74ALS138			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			5	10		5	10	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS138		SN74ALS138		
			MIN	MAX	MIN	MAX	
t_{PLH}	A, B, C	Any Y	6	27	6	22	ns
t_{PHL}			6	22	6	18	
t_{PLH}	Enable	Any Y	4	20	4	17	ns
t_{PHL}			5	20	5	17	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

recommended operating conditions

		SN54AS138			SN74AS138			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS138			SN74AS138			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA							V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V							mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V							μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V							mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			13			13		mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS138			SN74AS138			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A, B, C	Any Y		5.6			5.6		ns
t_{PHL}				6.1			6.1		
t_{PLH}	Enable	Any Y		5.8			5.8		ns
t_{PHL}				5.5			5.5		

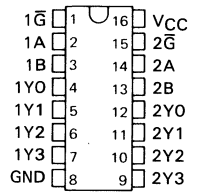
†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TYPES SN54ALS139, SN54AS139, SN74ALS139, SN74AS139
DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

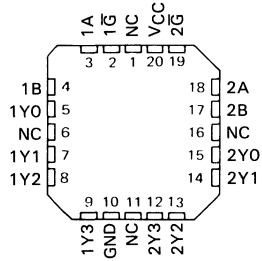
D2661, APRIL 1982—REVISED DECEMBER 1983

- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporates 2 Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS139, SN54AS139 . . . J PACKAGE
SN74ALS139, SN74AS139 . . . N PACKAGE
SN74ALS139, SN74AS139 . . . D PACKAGE
(TOP VIEW)



SN54ALS139, SN54AS139 . . . FH OR FK PACKAGE
SN74ALS139, SN74AS139 . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

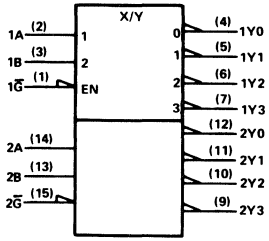
description

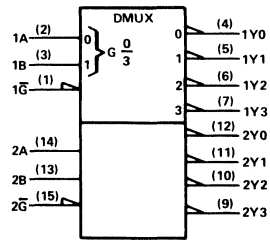
The 'ALS139 and 'AS139 circuits are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

The 'ALS139 and 'AS139 are comprised of two individual two-line to four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

The SN54ALS139 and SN54AS139 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS139 and SN74AS139 are characterized for operation from 0°C to 70°C.

logic symbols (alternatives)





Pin numbers shown are for J and N packages

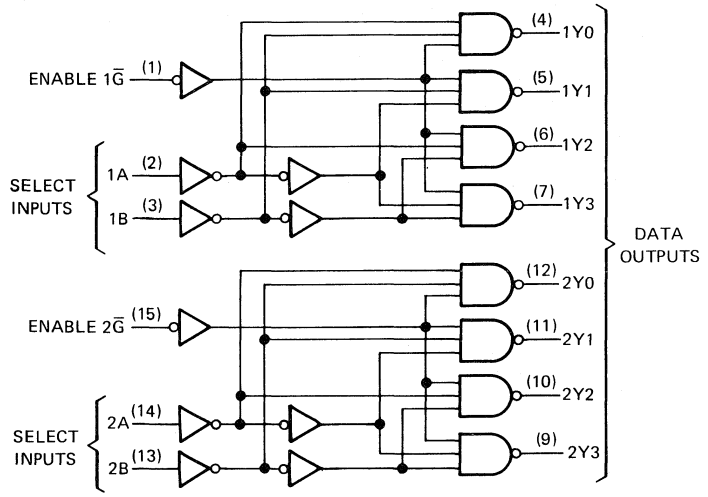
PRODUCT PREVIEW

TEXAS INSTRUMENTS

FUNCTION TABLE

INPUTS			OUTPUTS			
ENABLE	SELECT					
$\overline{G}$	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

functional block diagram (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS139, SN54AS139 . . . . . −55°C to 125°C
SN74ALS139, SN74AS139 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS139			SN74ALS139			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS139			SN74ALS139			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			4.5			4.5		mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS139			SN74ALS139			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A or B	Y		10			10		ns
t_{PHL}				10			10		
t_{PLH}	$\overline{G}$	Y		8			8		ns
t_{PHL}				8			8		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

recommended operating conditions

		SN54AS139			SN74AS139			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS139			SN74AS139			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			13			13		mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS139			SN74AS139			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A or B	Y		5.5			5.5		ns
t_{PHL}				6			6		
t_{PLH}	$\overline{G}$	Y		5.5			5.5		ns
t_{PHL}				5			5		

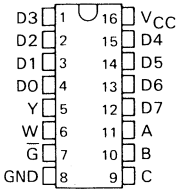
†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

D2661, APRIL 1982 – REVISED FEBRUARY 1984

- 8-Line to 1-Line Multiplexers Can Perform As:
  - Boolean Function Generators
  - Parallel-to-Serial Converters
  - Data Source Selectors
- Input Clamping Diodes Simplify System Design
- Fully Compatible With Most TTL Circuits
- Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS151, SN54AS151 . . . J PACKAGE
SN74ALS151, SN74AS151 . . . N PACKAGE
SN74ALS151, SN74AS151 . . . D PACKAGE
(TOP VIEW)



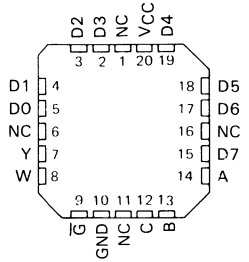
2

description

These monolithic data selectors/multiplexers provide full binary decoding to select one of eight data sources. The strobe input ($\overline{G}$) must be at a low logic level to enable the inputs. A high level at the strobe terminal forces the W output high and the Y output low.

The SN54ALS151 and SN54AS151 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS151 and SN74AS151 are characterized for operation from 0°C to 70°C.

SN54ALS151, SN54AS151 . . . FH OR FK PACKAGE
SN74ALS151, SN74AS151 . . . FN PACKAGE
(TOP VIEW)



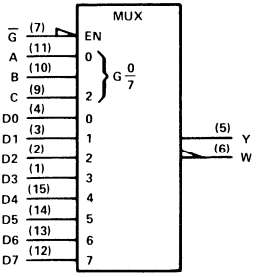
NC No internal connection

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	$\overline{G}$	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

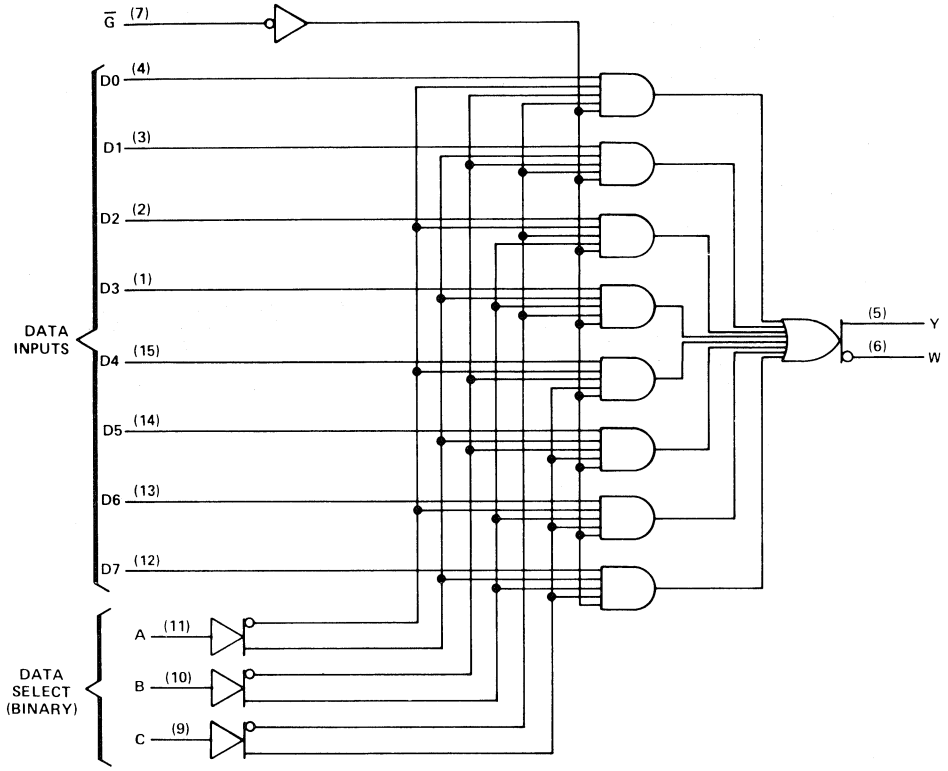
H = high level, L = low level, X = irrelevant
D0, D1 . . . D7 = the level of the D respective input

logic symbol



Pin numbers shown are for J and N packages.

logic diagram (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS151, SN54AS151 . . . . . 55 °C to 125 °C
SN74ALS151, SN74AS151 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150°C

recommended operating conditions

		SN54ALS151			SN74ALS151			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS151			SN74ALS151			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V,	Inputs at 4.5 V		7.5	12		7.5	12	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS151		SN74ALS151		
			MIN	MAX	MIN	MAX	
t_{PLH}	A, B, or C	Y	4	21	4	18	ns
t_{PHL}			8	28	8	24	
t_{PLH}	A, B, or C	W	7	28	7	24	ns
t_{PHL}			7	26	7	23	
t_{PLH}	Any D	Y	3	12	3	10	ns
t_{PHL}			5	18	5	15	
t_{PLH}	Any D	W	3	18	3	15	ns
t_{PHL}			4	18	4	15	
t_{PLH}	$\overline{G}$	Y	4	21	4	18	ns
t_{PHL}			4	23	4	19	
t_{PLH}	$\overline{G}$	W	5	23	5	19	ns
t_{PHL}			5	26	5	23	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

recommended operating conditions

		SN54AS151			SN74AS151			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			32			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS151			SN74AS151			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	A, B, or C	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	A, B, or C	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All others					20			20	
I_{IL}	A, B, or C	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	All others					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,			18.6	30		18.6	30	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

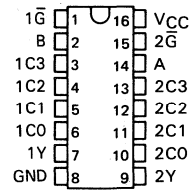
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS151		SN74AS151		
			MIN	MAX	MIN	MAX	
t_{PLH}	A, B, or C	Y	4.5	16	4.5	14.5	ns
t_{PHL}			4.5	16	4.5	15	
t_{PLH}	A, B, or C	W	4	14.5	4	12	ns
t_{PHL}			4	14.5	4	12	
t_{PLH}	Any D	Y	3	11.5	3	10.5	ns
t_{PHL}			3	12	3	11	
t_{PLH}	Any D	W	2	8	2	6.5	ns
t_{PHL}			1	5.5	1	4.5	
t_{PLH}	$\overline{G}$	Y	4.5	16	4.5	14	ns
t_{PHL}			3	12.5	3	11	
t_{PLH}	$\overline{G}$	W	1.5	7	1.5	6	ns
t_{PHL}			3	11	3	10	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

D2661, APRIL 1982—REVISED DECEMBER 1983

- **Permits Multiplexing from N Lines to 1 Line**
- **Performs Parallel-to-Serial Conversion**
- **Strobe (Enable) Line Provided for Cascading (N lines to n lines)**
- **Fully Compatible with Most TTL Circuits**
- **'ALS253 and 'AS253 Are 3-State Versions of These Parts**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS153, SN54AS153 . . . J PACKAGE
SN74ALS153, SN74AS153 . . . N PACKAGE
SN74ALS153, SN74AS153 . . . D PACKAGE
(TOP VIEW)



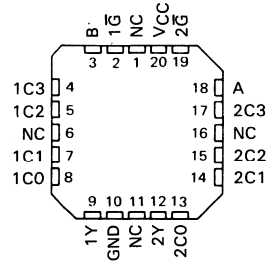
2

description

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate strobe inputs (G) are provided for each of the two four-line sections.

The SN54ALS153 and SN54AS153 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS153 and SN74AS153 are characterized for operation from 0°C to 70°C.

SN54ALS153, SN54AS153 . . . FH OR FK PACKAGE
SN74ALS153, SN74AS153 . . . FN PACKAGE
(TOP VIEW)



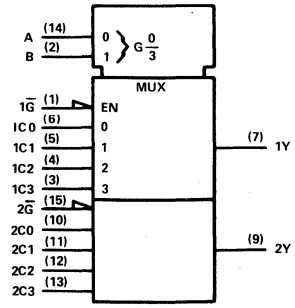
NC — No internal connection

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G̅	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

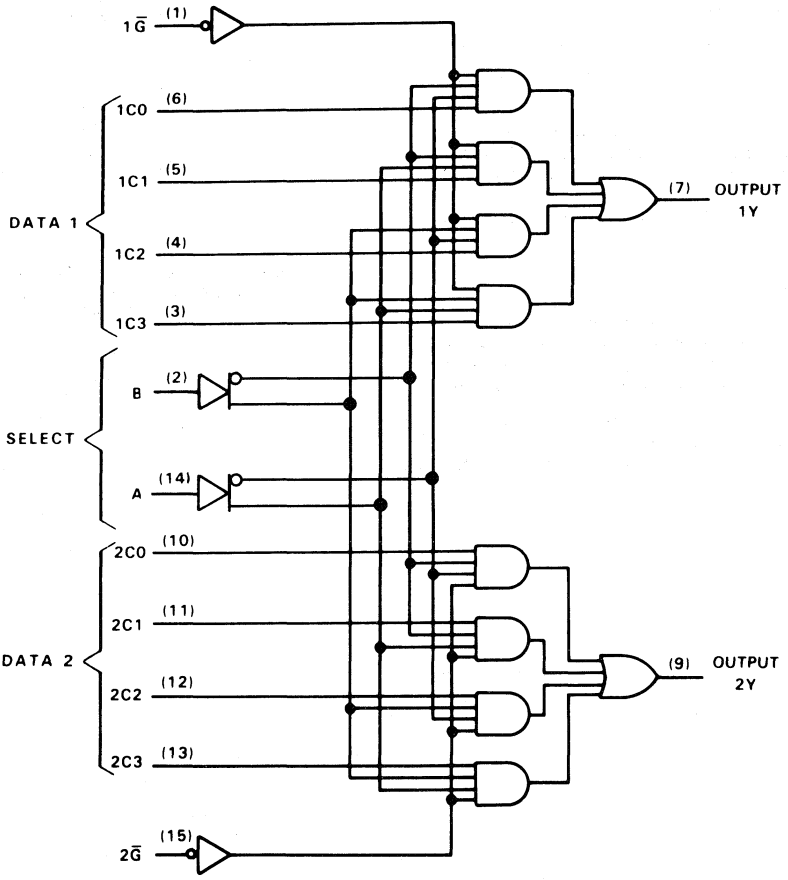
Select inputs A and B are common to both sections.

logic symbol



Pin numbers shown are for J and N packages.

logic diagram (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS153, SN54AS153 . . . . . −55 °C to 125 °C
SN74ALS153, SN74AS153 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS153			SN74ALS153			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS153			SN74ALS153			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V,	All inputs at 4.5 V		7.5	14		7.5	14	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS153		SN74ALS153		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	5	25	5	21	ns
t_{PHL}			5	25	5	21	
t_{PLH}	Data (Any C)	Y	3	12	3	10	ns
t_{PHL}			4	18	4	15	
t_{PLH}	G	Y	5	22	5	18	ns
t_{PHL}			5	22	5	18	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

recommended operating conditions

		SN54AS153			SN74AS153			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			32			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS153			SN74AS153			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V	I_{OL} = 48 mA					0.35	0.5	
I_I	A, B	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	A, B	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All others					20			20	
I_{IL}	A, B	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	All others					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	Outputs high		16	26		16	26	mA
			Outputs low		21	33		21	33	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS153		SN74AS153		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	3	14	3	12.5	ns
t_{PHL}			3	12.5	3	11	
t_{PLH}	Data (Any C)	Y	2	8	2	7	ns
t_{PHL}			2	8.5	2	8	
t_{PLH}	$\overline{G}$	Y	3	13	3	11.5	ns
t_{PHL}			2	10	2	9	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- **Buffered Inputs and Outputs**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

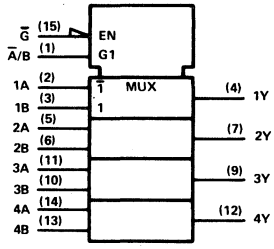
description

These monolithic data selectors/multiplexers contain inverters and drivers to supply full data selection to the four output gates. A separate strobe input ($\overline{G}$) is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The 'ALS157 and 'AS157 present true data whereas the 'ALS158 and 'AS158 present inverted data to minimize propagation delay time.

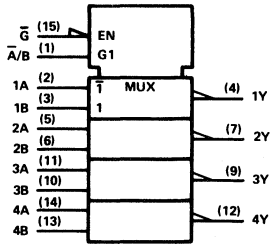
The SN54' family is characterized for operation over the full military temperature range −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

logic symbols

'ALS157, 'AS157

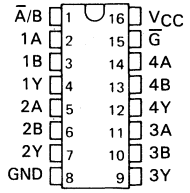


'ALS158, 'AS158

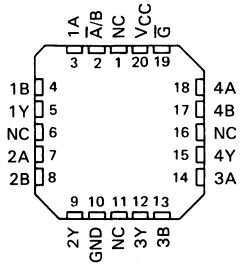


Pin numbers shown are for J and N packages.

SN54ALS', SN54AS'... J PACKAGE
SN74ALS', SN74AS'... N PACKAGE
SN74ALS', SN74AS'... D PACKAGE
(TOP VIEW)



SN54ALS', SN54AS'... FH OR FK PACKAGE
SN74ALS', SN74AS'... FN PACKAGE
(TOP VIEW)



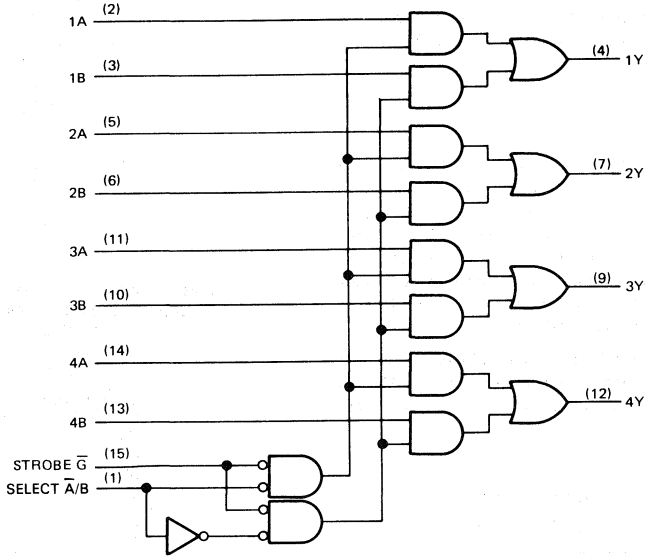
NC — No internal connection

FUNCTION TABLE

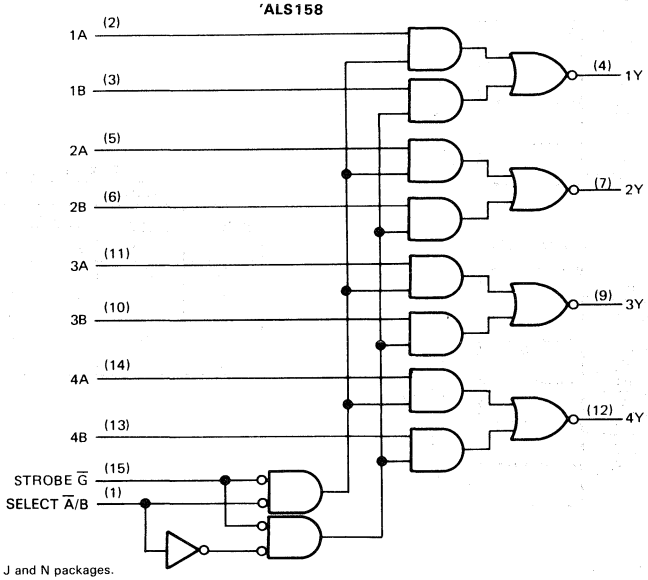
INPUTS				OUTPUT Y	
STROBE	SELECT	DATA		'ALS157	'ALS158
$\overline{G}$	A/B	A	B	'AS157	'AS158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

logic diagrams (positive logic)

'ALS157



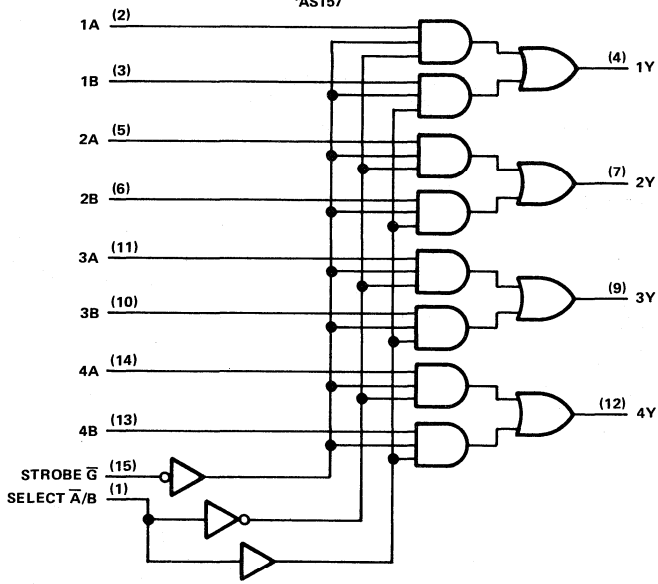
'ALS158



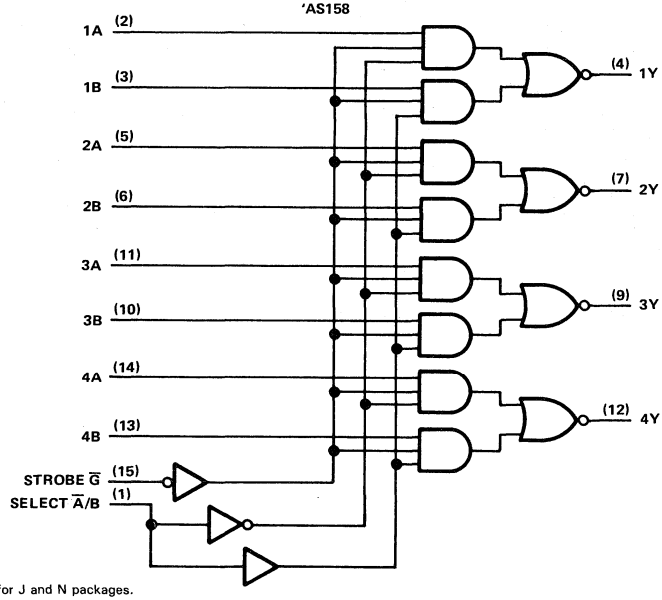
Pin numbers shown are for J and N packages.

logic diagrams (positive logic)

'AS157



'AS158



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS157, SN54ALS158 . . . . . −55°C to 125°C
SN74ALS157, SN74ALS158 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS157 SN54ALS158			SN74ALS157 SN74ALS158			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS157 SN54ALS158			SN74ALS157 SN74ALS158			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS157	V_{CC} = 5.5 V,			7.8			7.8		mA
	'ALS158				2.3			2.3		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit current, I_{OS}.

'ALS157 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS157			SN74ALS157			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A or B	Y		3.5			3.5		ns
t_{PHL}				5			5		
t_{PLH}	$\overline{A}$/B	Y		6			6		ns
t_{PHL}				6.5			6.5		
t_{PLH}	$\overline{G}$	Y		6			6		ns
t_{PHL}				6.5			6.5		

'ALS158 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS158			SN74ALS158			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A or B	Y		3.5			3.5		ns
t_{PHL}				5			5		
t_{PLH}	$\overline{A}$/B	Y		6			6		ns
t_{PHL}				6.5			6.5		
t_{PLH}	$\overline{G}$	Y		6			6		ns
t_{PHL}				6.5			6.5		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS157, SN54AS158 . . . . . −55°C to 125°C
SN74AS157, SN74AS158 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS157 SN54AS158			SN74AS157 SN74AS158			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS157 SN54AS158			SN74AS157 SN74AS158			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	$\overline{A}$/B	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	A, B, or $\overline{G}$					0.1			0.1	
I_{IH}	$\overline{A}$/B	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	A, B, or $\overline{G}$					20			20	
I_{IL}	$\overline{A}$/B	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	A, B or $\overline{G}$					−0.5			−0.5	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS157	V_{CC} = 5.5 V,			17.5	28		17.5	28	mA
	'AS158				15.6	22.5		15.6	22.5	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit current, I_{OS}.

'AS157 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS157		SN74AS157		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	7.5	1	6	ns
t_{PHL}			1	6.5	1	5.5	
t_{PLH}	$\overline{A}$/B,	Y	2	12	2	11	ns
t_{PHL}			2	12	2	10	
t_{PLH}	$\overline{G}$	Y	2	12.5	2	10.5	ns
t_{PHL}			2	8.5	2	7.5	

'AS158 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS158		SN74AS158		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	6	1	5	ns
t_{PHL}			1	5.5	1	4.5	
t_{PLH}	$\overline{A}$/B	Y	2	11	2	9.5	ns
t_{PHL}			2	11.5	2	10.5	
t_{PLH}	$\overline{G}$	Y	2	8	2	6.5	ns
t_{PHL}			2	11.5	2	10	

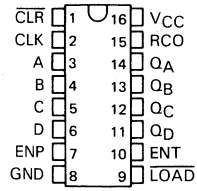
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

SN54ALS160B THRU SN54ALS163B, SN54AS160 THRU SN54AS163
SN74ALS160B THRU SN74ALS163B, SN74AS160 THRU SN74AS163
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

D2661, APRIL 1982—REVISED JUNE 1984

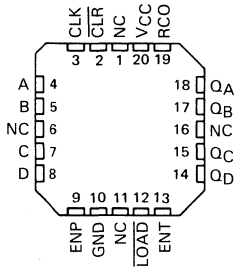
- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Synchronous Counting**
- **Synchronously Programmable**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . N PACKAGE
SN74ALS', SN74AS' . . . D PACKAGE
(TOP VIEW)



2

SN54ALS', SN54AS' . . . FH OR FK PACKAGE
SN74ALS', SN74AS' . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 'ALS160B, 'ALS162B, 'AS160, and 'AS162 are decade counters, and the 'ALS161B, 'ALS163B, 'AS161, and 'AS163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

The clear function for the 'ALS160B, 'ALS161B, 'AS160, and 'AS161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load, or enable inputs.

The clear function for the 'ALS162B, 'ALS163B, 'AS162, and 'AS163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

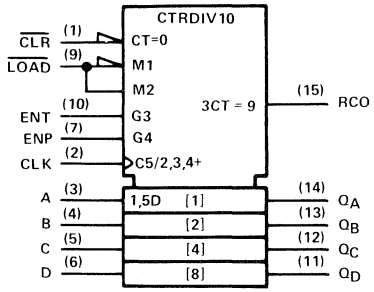
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (ENP and ENT) must be high to count, and ENT is fed forward to enable the ripple carry output. The ripple carry output (RCO) thus enabled will produce a high-level pulse while the count is maximum (9 or 15 with Q_A high). This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the ENP or ENT are allowed regardless of the level of the clock input.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{\text{LOAD}}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

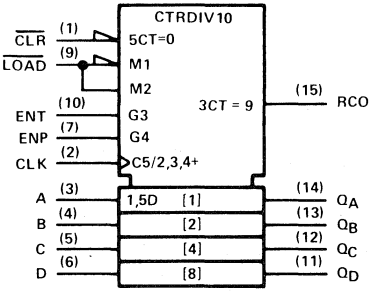
The SN54ALS160B through SN54ALS163B and SN54AS160 through SN54AS163 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS160B through SN74ALS163B and SN74AS160 through SN74AS163 are characterized for operation from 0°C to 70°C.

logic symbols

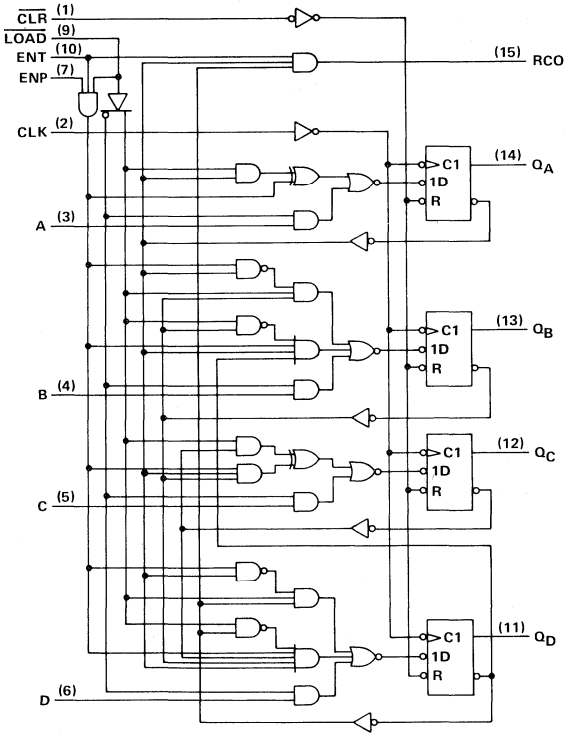
'ALS160B AND 'AS160 DECADE COUNTERS WITH DIRECT CLEAR



'ALS162B AND 'AS162 DECADE COUNTERS WITH SYNCHRONOUS CLEAR



'ALS160B and 'AS160 logic diagram (positive logic)

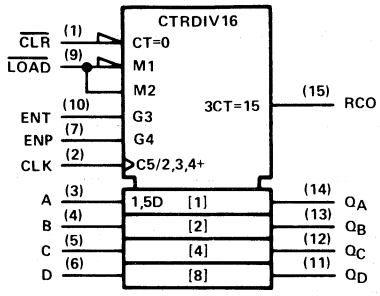


'ALS162B and 'AS162 decade counters are similar; however the clear is synchronous as shown for the 'ALS163B and 'AS163 binary counters.

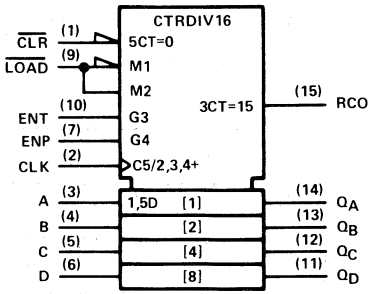
Pin numbers shown are for J and N packages.

logic symbols

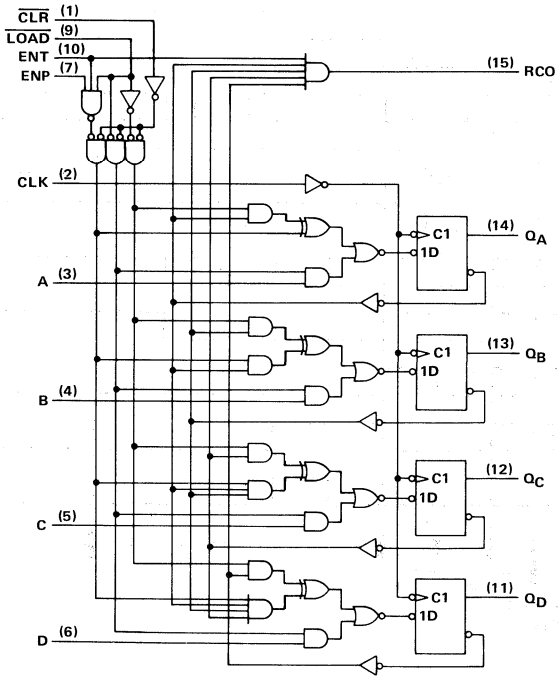
'ALS161B and 'AS161 BINARY COUNTERS WITH DIRECT CLEAR



'ALS163B AND 'AS163 BINARY COUNTERS WITH SYNCHRONOUS CLEAR



'ALS163B and 'AS163 logic diagram (positive logic)



'ALS161B and 'AS161 synchronous binary counters are similar; however the clear is asynchronous as shown for the 'ALS160B and 'AS160 decade counters.

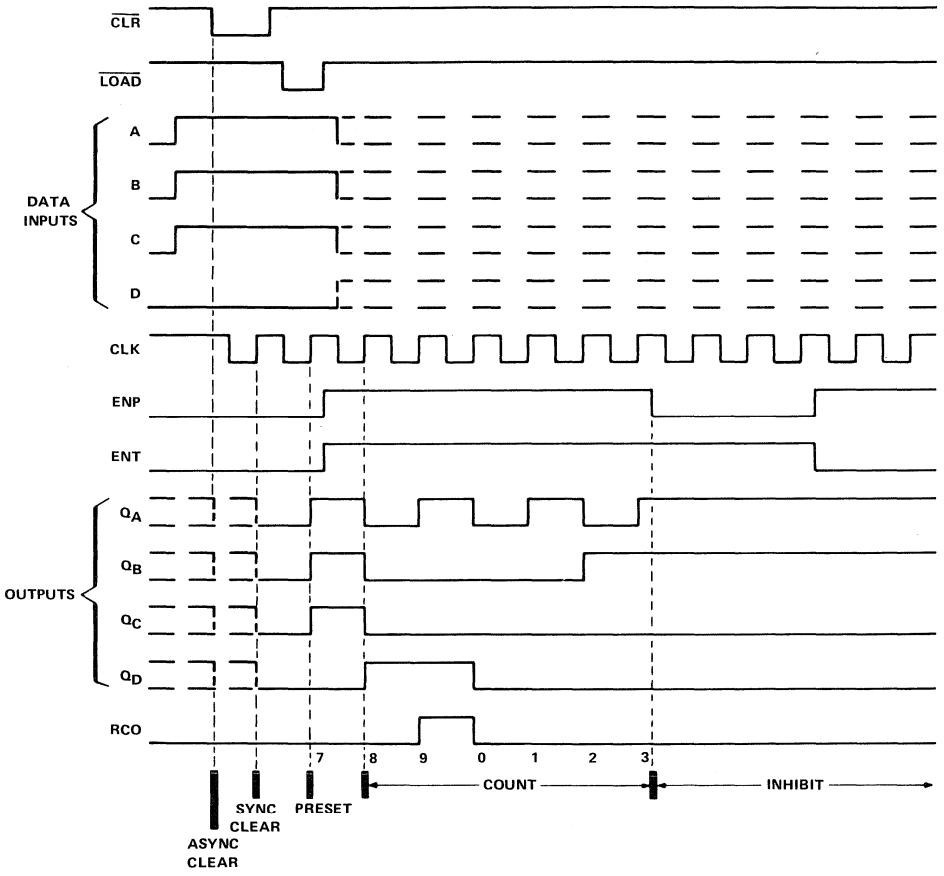
Pin numbers shown are for J and N packages.

typical clear, preset, count, and inhibit sequences

'ALS160B, 'AS160, 'ALS162B, 'AS162

Illustrated below is the following sequence:

1. Clear outputs to zero ('ALS160B and 'AS160 are asynchronous; 'ALS162B and 'AS162 are synchronous)
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit

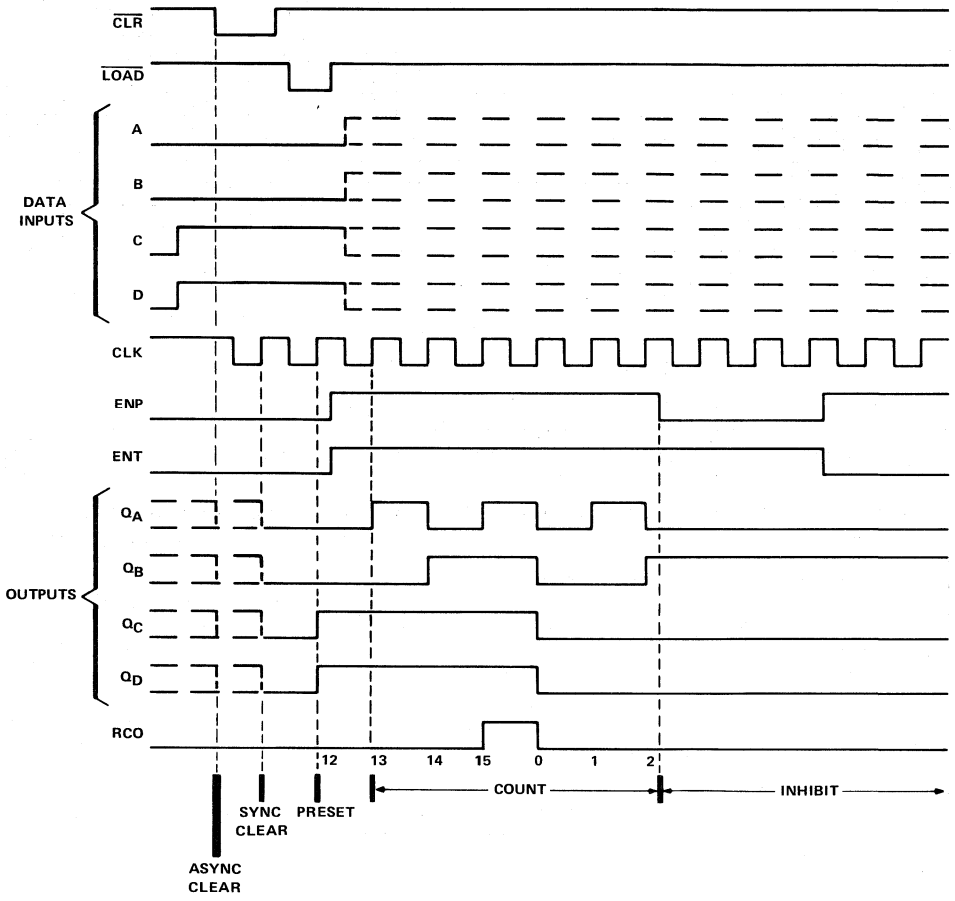


typical clear, preset, count, and inhibit sequences

'ALS161B, 'AS161, 'ALS163B, 'AS163

Illustrated below is the following sequence:

1. Clear outputs to zero ('ALS161B and 'AS161 are asynchronous; 'ALS163B and 'AS163 are synchronous)
2. Preset to binary twelve
3. Count to thirteen, fourteen, fifteen, zero, one, and two
4. Inhibit



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS160B thru SN54ALS163B . . . . . −55°C to 125°C
SN74ALS160B thru SN74ALS163B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

				SN54ALS160B THRU SN54ALS163B			SN74ALS160B THRU SN74ALS163B			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
I_{OH}	High-level output current					−0.4			−0.4	mA
I_{OL}	Low-level output current					4			8	mA
f_{clock}	Clock frequency			0		35	0		40	MHz
t_w	Pulse duration	CLK high or low		14			12.5			ns
		'ALS160B, 'ALS161B $\overline{CLR}$ low		20			15			
t_{su}	Setup time before CLK↑	A, B, C, D		20			15			ns
		$\overline{LOAD}$		20			15			
		ENP, ENT	'ALS160B, 'ALS161B	20			15			
			'ALS162B, 'ALS163B	20			15			
		'ALS160B, 'ALS161B $\overline{CLR}$ inactive		10			10			
		'ALS162B, 'ALS163B	$\overline{CLR}$ low	20			15			
			$\overline{CLR}$ high (inactive)	10			10			
t_h	Hold time, all synchronous inputs after CLK↑			0			0			ns
T_A	Operating free-air temperature			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS160B THRU SN54ALS163B			SN74ALS160B THRU SN74ALS163B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			12	21		12	21	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS160B, 'ALS161B switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS160B SN54ALS161B		SN74ALS160B SN74ALS161B		
			MIN	MAX	MIN	MAX	
f_{max}			35		40		MHz
t_{PLH}	CLK	RCO	5	25	5	20	ns
t_{PHL}			5	25	5	20	
t_{PLH}	CLK	Any Q	4	18	4	15	ns
t_{PHL}			6	25	6	20	
t_{PLH}	ENT	RCO	3	16	3	13	ns
t_{PHL}			3	16	3	13	
t_{PHL}	$\overline{CLR}$	Any Q	8	27	8	24	ns
t_{PHL}	$\overline{CLR}$	RCO	11	28	11	23	ns

'ALS162B, 'ALS163B switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS162B SN54ALS163B		SN74ALS162B SN74ALS163B		
			MIN	MAX	MIN	MAX	
f_{max}			35		40		MHz
t_{PLH}	CLK	RCO	5	25	5	20	ns
t_{PHL}			5	25	5	20	
t_{PLH}	CLK	Any Q	4	18	4	15	ns
t_{PHL}			6	25	6	20	
t_{PLH}	ENT	RCO	3	16	3	13	ns
t_{PHL}			3	16	3	13	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS160 thru SN54AS163 . . . . . −55°C to 125°C
SN74AS160 thru SN74AS163 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

				SN54AS160 THRU SN54AS163			SN74AS160 THRU SN74AS163			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
I_{OH}	High-level output current					−2			−2	mA
I_{OL}	Low-level output current					20			20	mA
f_{clock}	Clock frequency			0		65	0		75	MHz
t_w	Pulse duration	CLK high or low		7.7			6.7			ns
		'AS160, 'AS161 $\overline{CLR}$ low		10			8			
t_{su}	Setup time before CLK↑	A, B, C, D		10			8			ns
		$\overline{LOAD}$		10			8			
		ENP, ENT		10			8			
		'AS160, 'AS161 $\overline{CLR}$ inactive		10			8			
		'AS162, 'AS163	$\overline{CLR}$ low	14			12			
			$\overline{CLR}$ high (inactive)	10			9			
t_h	Hold time, all synchronous inputs after CLK↑			2			0			ns
T_A	Operating free-air temperature			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS160 THRU SN54AS163			SN74AS160 THRU SN74AS163			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	V
I_I	$\overline{LOAD}$	V_{CC} = 5.5 V,	V_I = 7 V			0.3			0.3	mA
	ENT					0.2			0.2	
	All other					0.1			0.1	
I_{IH}	$\overline{LOAD}$	V_{CC} = 5.5 V,	V_I = 2.7 V			60			60	μA
	ENT					40			40	
	All other					20			20	
I_{IL}	$\overline{LOAD}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−1.5			−1.5	mA
	ENT					−1			−1	
	All other					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			35	53		35	53	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS160, 'AS161 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS160 SN54AS161		SN74AS160 SN74AS161		
			MIN	MAX	MIN	MAX	
f_{max}			65		75		MHz
t_{PHL}	CLK	RCO	2	14	2	12.5	ns
t_{PLH}		RCO (with $\overline{LOAD}$ high)	1	8.5	1	8	
t_{PLH}		RCO (with $\overline{LOAD}$ low)	3	17.5	3	16.5	
t_{PLH}	CLK	Any Q	1	7.5	1	7	ns
t_{PHL}			2	14	2	13	
t_{PLH}	ENT	RCO	1.5	10	1.5	9	ns
t_{PHL}			1	9.5	1	8.5	
t_{PHL}	$\overline{CLR}$	Any Q	2	14	2	13	ns
t_{PHL}	$\overline{CLR}$	RCO	2	14	2	12.5	ns

'AS162, 'AS163 switching characteristics (see Note 1)

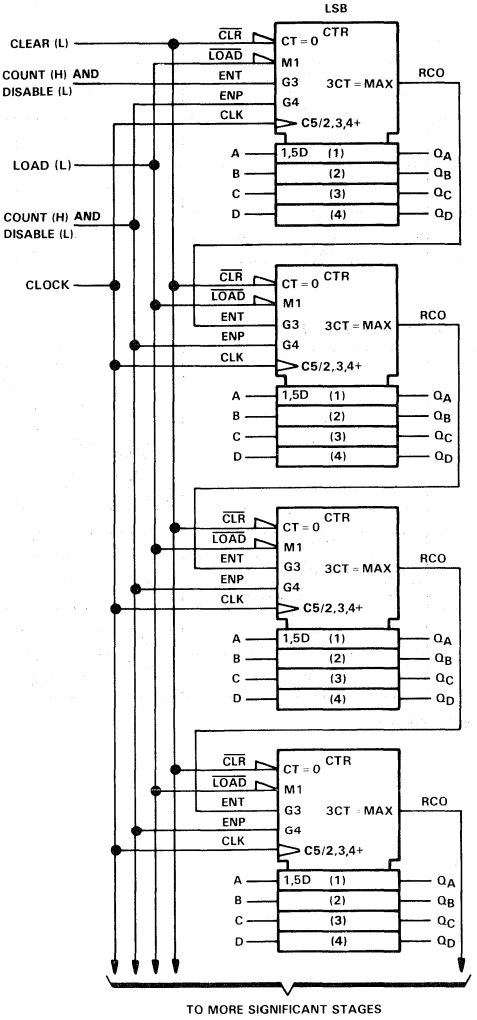
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS162 SN54AS163		SN74AS162 SN74AS163		
			MIN	MAX	MIN	MAX	
f_{max}			65		75		MHz
t_{PHL}	CLK	RCO	2	14	2	12.5	ns
t_{PLH}		RCO (with $\overline{LOAD}$ high)	1	8.5	1	8	
t_{PLH}		RCO (with $\overline{LOAD}$ low)	3	17.5	3	16.5	
t_{PLH}	CLK	Any Q	1	7.5	1	7	ns
t_{PHL}			2	14	2	13	
t_{PLH}	ENT	RCO	1.5	10	1.5	9	ns
t_{PHL}			1	9.5	1	8.5	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

TYPICAL APPLICATION DATA

N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The 'ALS160B, 'AS160, 'ALS162B, and 'AS162 will count in BCD and the 'ALS161B, 'AS161, 'ALS163B and 'AS163 will count in binary. Virtually any count mode (modulo-N, N_1-to-N_2, N_1-to-maximum) can be used with this fast look-ahead circuit.

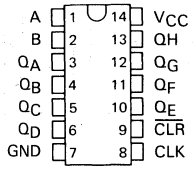


TYPES SN54ALS164, SN74ALS164
8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

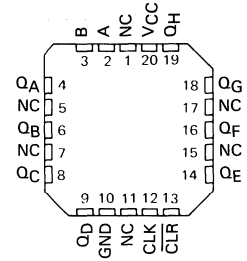
D2661, APRIL 1982—REVISED DECEMBER 1983

- **AND-Gated (Enable/Disable) Serial Inputs**
- **Fully Buffered Clock and Serial Inputs**
- **Direct Clear**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS164 . . . J PACKAGE
SN74ALS164 . . . N PACKAGE
SN74ALS164 . . . D PACKAGE
(TOP VIEW)



SN54ALS164 . . . FH OR FK PACKAGE
SN74ALS164 . . . FN PACKAGE
(TOP VIEW)



NC—No Internal connection

description

These 8-bit shift registers feature AND-gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

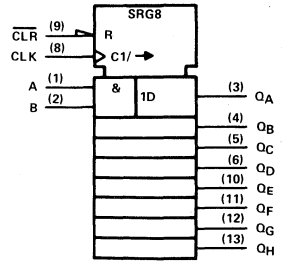
The SN54ALS164 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS164 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS				OUTPUTS		
CLEAR	CLOCK	A	B	Q_A	Q_B . . . Q_H	
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level.
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most-recent ↑ transition of the clock; indicates a one-bit shift.

logic symbol



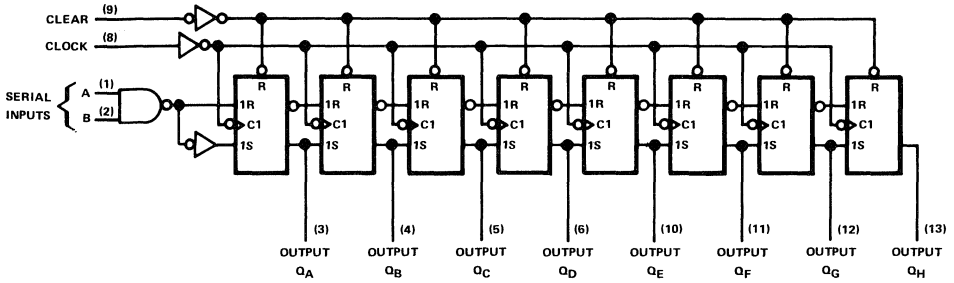
Pin numbers shown are for J and N packages.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

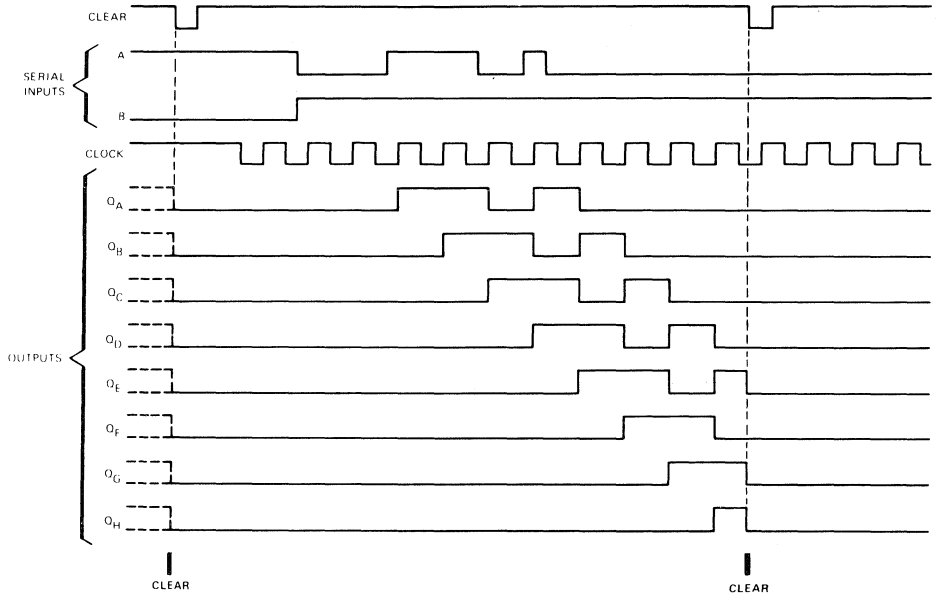
TEXAS INSTRUMENTS

logic diagram (positive logic)



Pin numbers shown are for J and N packages.

typical clear, shift, and clear sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS164 . . . . . −55 °C to 125 °C
SN74ALS164 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54ALS164			SN74ALS164			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	$\overline{CLR}$ low							ns
		CLK high							
		CLK low							
t_{su}	Setup time before CLK↑	SH/LD							ns
		Data							
		$\overline{CLR}$ inactive							
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS164			SN74ALS164			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	See Note 1		10			10		mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: With 4.5 Volts applied to the serial input and all other inputs except the clock grounded, I_{CC} is measured after a clock transition from 0 to 4.5 volts.

switching characteristics (see Note 2)

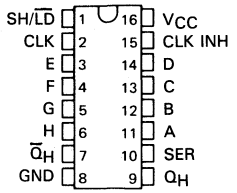
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS164			SN74ALS164			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}				60			60		MHz
t_{PHL}	$\overline{CLR}$	Any Q		12			12		ns
t_{PLH}	CLK	Any Q		10			10		ns
t_{PHL}				11			11		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: For load circuit and voltage waveforms, see page 1-12.

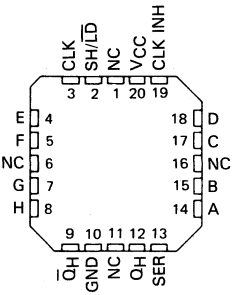
Additional information on these products can be obtained from the factory as it becomes available.

- **Complementary Outputs**
- **Direct Overriding Load (Data) Inputs**
- **Gated Clock Inputs**
- **Parallel-to-Serial Data Conversion**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS165 . . . J PACKAGE
SN74ALS165 . . . N PACKAGE
SN74ALS165 . . . D PACKAGE
(TOP VIEW)



SN54ALS165 . . . FH OR FK PACKAGE
SN74ALS165 . . . FN PACKAGE
(TOP VIEW)



NC – no internal connection

description

The 'ALS165 is an 8-bit serial shift register that, when clocked, shifts the data toward serial output $\overline{Q}_H$. Parallel-in access to each stage is provided by eight individual direct data inputs that are enabled by a low level at the SH/LD input. The 'ALS165 also features a clock inhibit function and a complemented serial output $\overline{Q}_H$.

Clocking is accomplished by a low-to-high transition of the CLK input while SH/$\overline{LD}$ is held high and CLK INH is held low. The functions of the CLK and CLK INH (clock inhibit) inputs are interchangeable. Since a low CLK input and a low-to-high transition of CLK INH will also accomplish clocking, CLK INH should be changed to the high level only while the CLK input is high. Parallel loading is inhibited when SH/$\overline{LD}$ is held high. The parallel inputs to the register are enabled while SH/$\overline{LD}$ is low independently of the levels of CLK, CLK INH, or SER inputs.

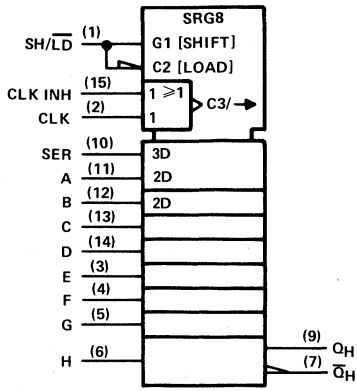
The SN54ALS165 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS165 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS			FUNCTION
SH/$\overline{LD}$	CLK	CLK INH	
L	X	X	PARALLEL LOAD
H	H	X	NO CHANGE
H	X	H	NO CHANGE
H	L	↑	SHIFT
H	↑	L	SHIFT

SHIFT – content of each internal register shifts toward serial output Q_H. Data at serial input is shifted into first register.

logic symbol



Pin numbers shown are for J and N packages.

PRODUCT PREVIEW

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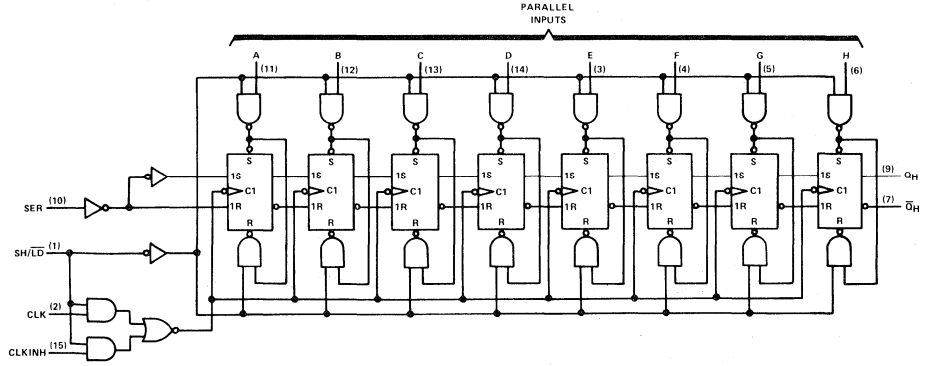
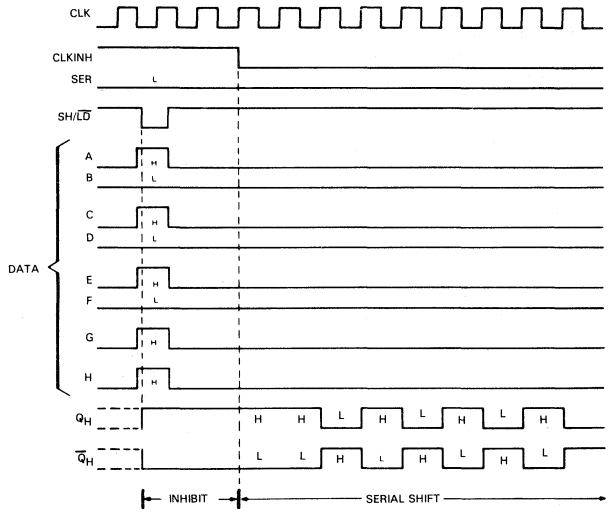
logic diagram (positive logic)



Pin numbers shown are for J and N packages

typical shift, load, and inhibit sequences

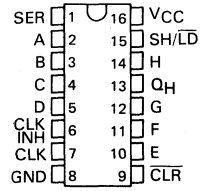


absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

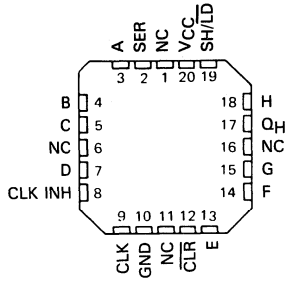
Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS165 . . . . . −55°C to 125°C
SN74ALS165 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

- Synchronous Load
- Direct Overriding Clear
- Parallel to Serial Conversion
- Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS166 . . . J PACKAGE
SN74ALS166 . . . N PACKAGE
SN74ALS166 . . . D PACKAGE
(TOP VIEW)



SN54ALS166 . . . FH OR FK PACKAGE
SN74ALS166 . . . FN PACKAGE
(TOP VIEW)



NC—No Internal connection

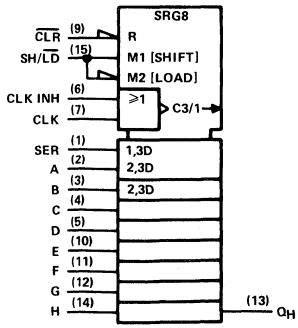
description

The 'ALS166 8-bit shift register is compatible with most other TTL logic families. All inputs are buffered to lower the drive requirements. Input clamping diodes minimize switching transients and simplify system design.

These parallel-in or serial-in, serial-out registers have a complexity of 77 equivalent gates on a monolithic chip. They feature gated clock inputs and an overriding clear input. The parallel-in or serial-in modes are established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This, of course, allows the system clock to be free-running and the register can be stopped on command with the clock input. The clock-inhibit input should be changed to the high level only when the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

The SN54ALS166 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS166 is characterized for operation from 0°C to 70°C.

logic symbol



Pin numbers shown are for J and N packages.

FUNCTION TABLE

INPUTS						INTERNAL OUTPUTS		OUTPUT
CLEAR	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a . . . h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

PRODUCT PREVIEW

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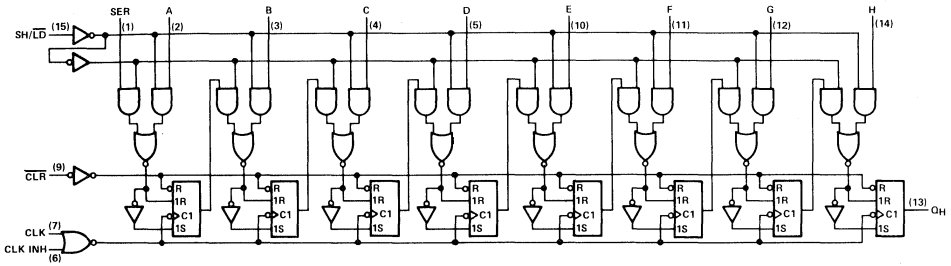
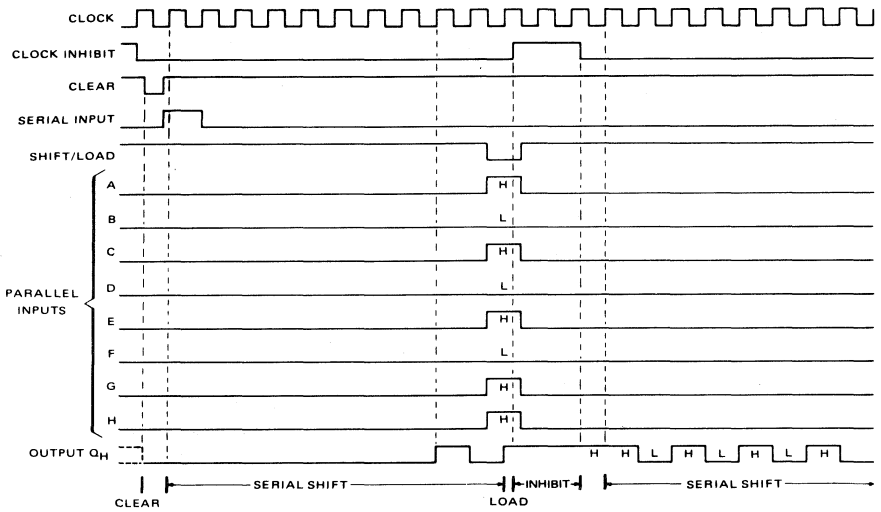
logic diagram (positive logic)



Pin numbers shown are for J and N packages.

typical clear, shift, load, inhibit, and shift sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS166 . . . . . −55 °C to 125 °C
SN74ALS166 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54ALS166			SN74ALS166			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	$\overline{CLR}$ low							ns
		CLK high							
		CLK low							
t_{su}	Setup time before CLK↑	SH/$\overline{LD}$							ns
		Data							
		$\overline{CLR}$ inactive							
t_h	Hold time, data after CLK↑								ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS166			SN74ALS166			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	See Note 1		16			16		mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: With 4.5 Volts applied to the serial input and all other inputs except the clock grounded, I_{CC} is measured after a clock transition from 0 to 4.5 volts.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS166			SN74ALS166			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}				60			60		MHz
t_{PHL}	$\overline{CLR}$	Q_H		10			10		ns
t_{PLH}	CLK	Q_H		12			12		ns
t_{PHL}				13			13		

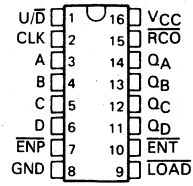
†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: For load circuit and voltage waveforms, see page 1-12.
Additional information on these products can be obtained from the factory as it becomes available.

SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS

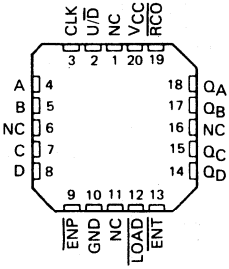
MARCH 1984 – REVISED JULY 1984

- **Fully Synchronous Operation for Counting and Programming**
- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Fully Independent Clock Circuit**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . N PACKAGE
SN74ALS', SN74AS' . . . D PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FH OR FK PACKAGE
SN74ALS', SN74AS' . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. The 'ALS168B and 'AS168 are decade counters and the 'ALS169B and 'AS169 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

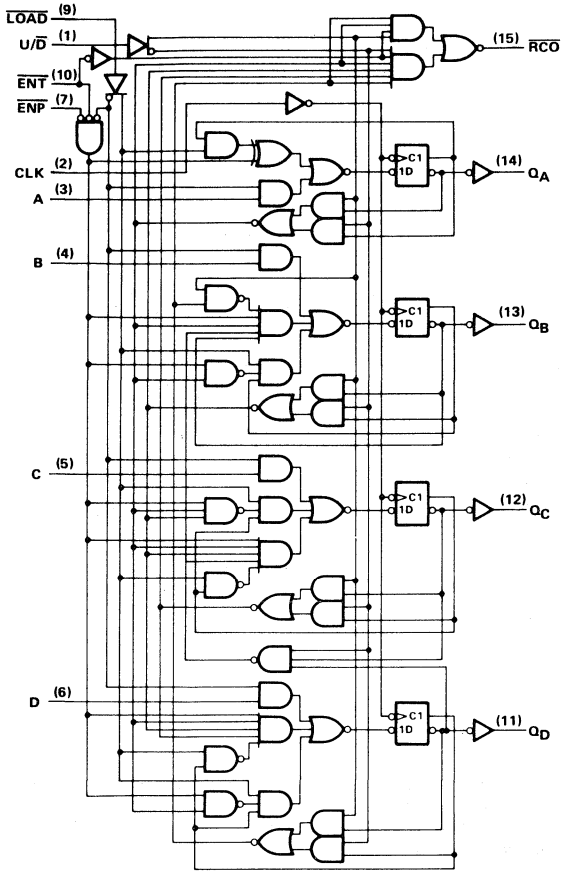
These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous application without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ($\overline{ENP}$ and $\overline{ENT}$) must be low to count. The direction of the count is determined by the level of the U/$\overline{D}$ input. When U/$\overline{D}$ is high, the counter counts up; when low, it counts down. Input $\overline{ENT}$ is fed forward to enable the carry output. The riple carry output ($\overline{RCO}$) thus enabled will produce a low-level pulse while the count is zero (all inputs low) counting down or maximum (9 or 15) counting up. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transistions at $\overline{ENP}$ or $\overline{ENT}$ are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

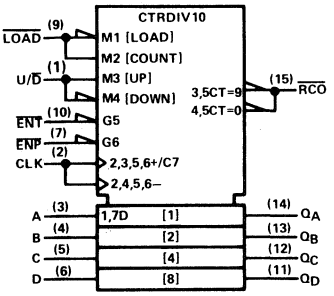
These counters feature a fully independent clock circuit. Changes at control inputs ($\overline{ENP}$, $\overline{ENT}$, $\overline{LOAD}$, U/$\overline{D}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

The SN54ALS168B, SN54AS168, SN54ALS169B, and SN54AS169 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS168B, SN74AS168, SN74ALS169B, and SN74AS169 are characterized for operation from 0°C to 70°C.

'ALS168B, 'AS168 logic diagram (positive logic)

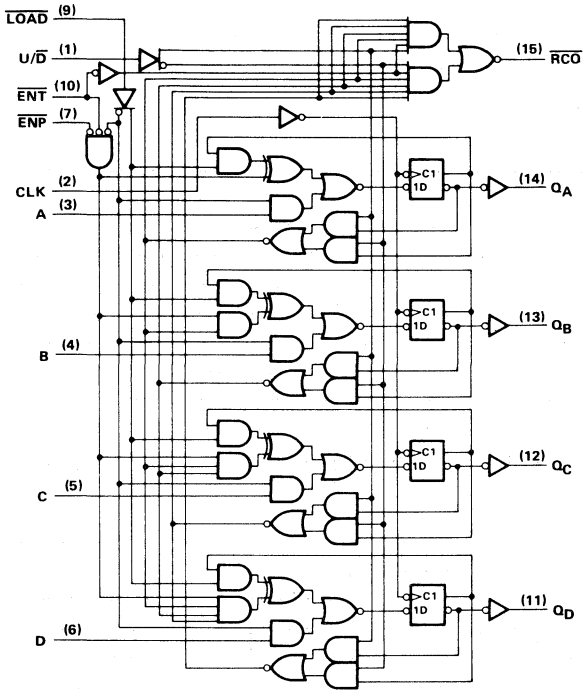


'ALS168B, 'AS168 logic symbol

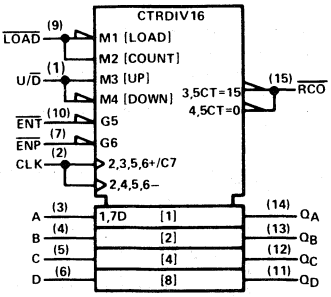


Pin numbers shown are for J and N packages.

'ALS169B, 'AS169 logic diagram (positive logic)



'ALS169B, 'AS169 logic symbol

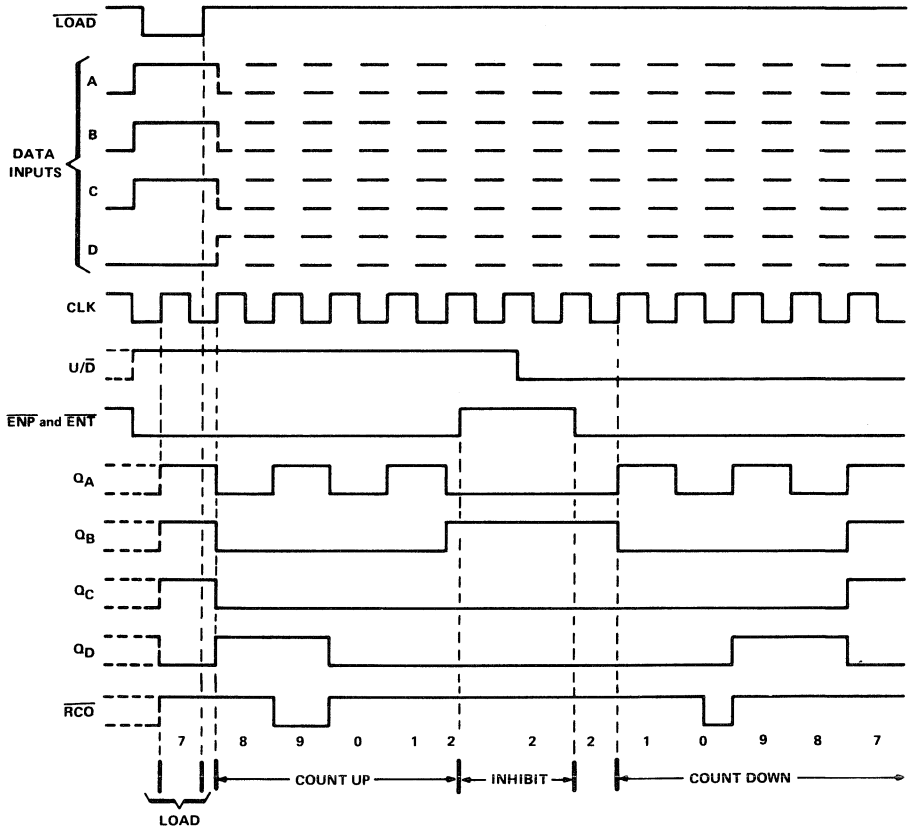


Pin numbers shown are for J and N packages.

'ALS168B, 'AS168 typical load, count, and inhibit sequences

Illustrated below is the following sequence:

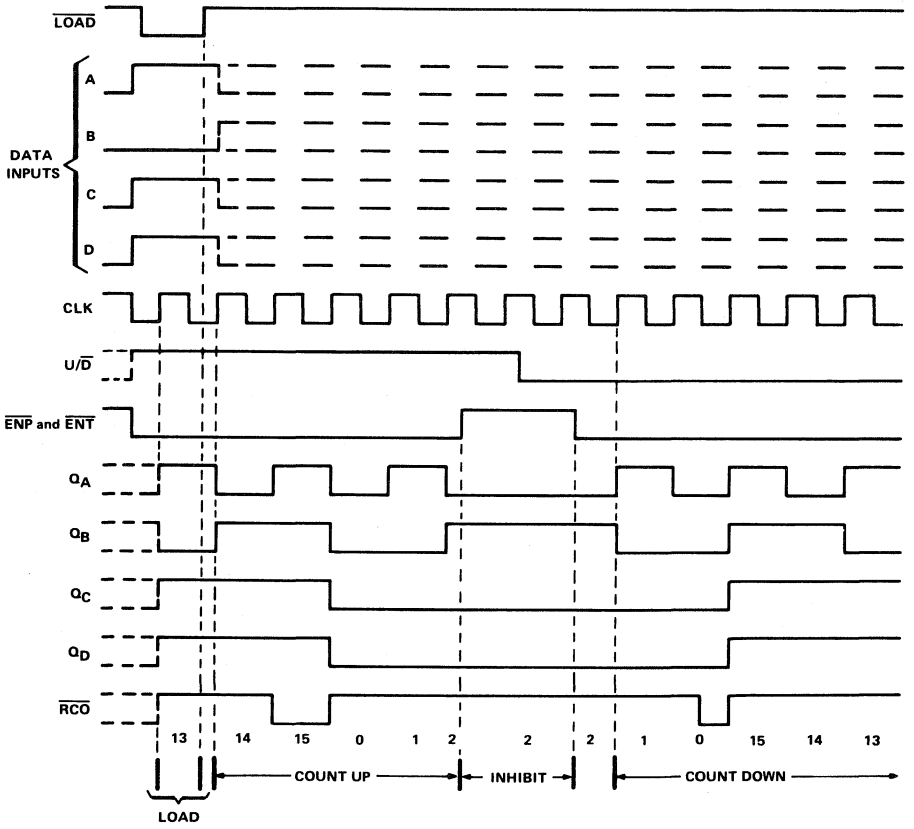
1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven



'ALS169B, 'AS169 typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen
2. Count up to fourteen, fifteen (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS168B, SN54ALS169B . . . . . −55°C to 125°C
SN74ALS168B, SN74ALS169B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS168B SN54ALS169B			SN74ALS168B SN74ALS169B			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		35	0		40	MHz
t_w	Pulse duration	CLK high or low	14			12.5			ns
t_{su}	Setup time before CLK↑	A, B, C, or D	20			15			ns
		$\overline{ENP}$ or $\overline{ENT}$	25			15			
		$\overline{LOAD}$	20			15			
		U/$\overline{D}$	20			15			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS168B SN54ALS169B			SN74ALS168B SN74ALS169B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			15	25		15	25	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS168B, 'ALS169B switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, RL = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS168B SN54ALS169B		SN74ALS168B SN74ALS169B		
			MIN	MAX	MIN	MAX	
f_{max}			35		40		MHz
t_{PLH}	CLK	$\overline{RCO}$	3	25	3	20	ns
t_{PHL}			6	25	6	20	
t_{PLH}	CLK	Any Q	2	20	2	15	ns
t_{PHL}			5	25	5	20	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	2	16	2	13	ns
t_{PHL}			3	19	3	16	
t_{PLH}	U/$\overline{D}$	$\overline{RCO}$	5	22	5	19	ns
t_{PHL}			5	22	5	19	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS168, SN54AS169 . . . . . −55 °C to 125 °C
SN74AS168, SN74AS169 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54AS168 SN54AS169			SN74AS168 SN74AS169			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0		65	0		75	MHz
t_w	Pulse duration	CLK high or low	7.7			6.7			ns
t_{su}	Setup time before CLK↑	A, B, C, or D	10			8			ns
		$\overline{ENP}$ or $\overline{ENT}$	10			8			
		$\overline{LOAD}$	10			8			
		U/$\overline{D}$	10			8			
t_h	Hold time, data after CLK↑		2			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS168 SN54AS169			SN74AS168 SN74AS169			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	V
I_I	$\overline{LOAD}$, $\overline{ENT}$, U/$\overline{D}$	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	$\overline{LOAD}$, $\overline{ENT}$, U/$\overline{D}$	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All others					20			20	
I_{IL}	$\overline{LOAD}$, $\overline{ENT}$, U/$\overline{D}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	All others,					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			41	63		41	63	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS168, 'AS169 switching characteristics (see Note 1)

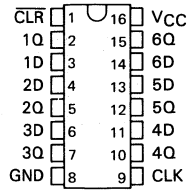
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, RL = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS168 SN54AS169		SN74AS168 SN74AS169		
			MIN	MAX	MIN	MAX	
f_{max}			65		75		MHz
t_{PLH}	CLK	$\overline{RCO}$ ($\overline{LOAD}$ high or low)	3	17.5	3	16.5	ns
t_{PHL}			2	14	2	13	
t_{PLH}	CLK	Any Q	1	7.5	1	7	ns
t_{PHL}			2	14	2	13	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	1.5	10	1.5	9	ns
t_{PHL}			1.5	10	1.5	9	
t_{PLH}	U/$\overline{D}$	$\overline{RCO}$	2	14	2	12	ns
t_{PHL}			2	14.5	2	13	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

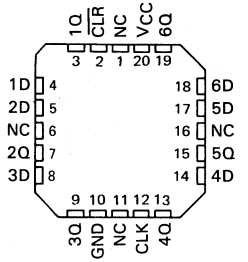
D2661, APRIL 1982—REVISED FEBRUARY 1984

- **'ALS174 and 'AS174 Contain Six Flip-Flops with Single-Rail Outputs**
- **'ALS175 and 'AS175 Contain Four Flip-Flops with Double-Rail Outputs**
- **Buffered Clock and Direct Clear Inputs**
- **Applications Include:**
  Buffer/Storage Registers
  Shift Registers
  Pattern Generators
- **Fully Buffered Outputs for Maximum Isolation from External Disturbance ('AS only)**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

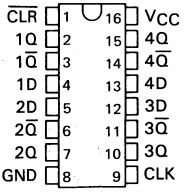
SN54ALS174, SN54AS174 . . . J PACKAGE
SN74ALS174, SN74AS174 . . . N PACKAGE
SN74ALS174, SN74AS174 . . . D PACKAGE
(TOP VIEW)



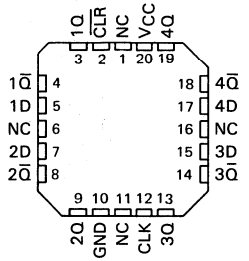
SN54ALS174, SN54AS174 . . . FH OR FK PACKAGE
SN74ALS174, SN74AS174 . . . FN PACKAGE
(TOP VIEW)



SN54ALS175, SN54AS175 . . . J PACKAGE
SN74ALS175, SN74AS175 . . . N PACKAGE
SN74ALS175, SN74AS175 . . . D PACKAGE
(TOP VIEW)



SN54ALS175, SN54AS175 . . . FH OR FK PACKAGE
SN74ALS175, SN74AS175 . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection.

description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input and the 'ALS175 and 'AS175 feature complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These circuits are fully compatible for use with most TTL circuits.

The SN54ALS174, SN54ALS175, SN54AS174, and SN54AS175 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS174, SN74ALS175, SN74AS174, and SN74AS175 are characterized for operation from 0°C to 70°C.

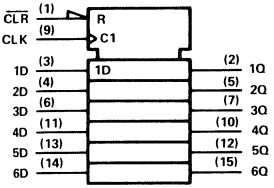
FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
$\overline{CLR}$	CLK	D	Q	$\overline{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

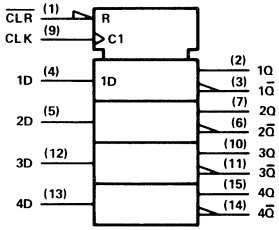
† 'ALS175 and 'AS175 only

logic symbols

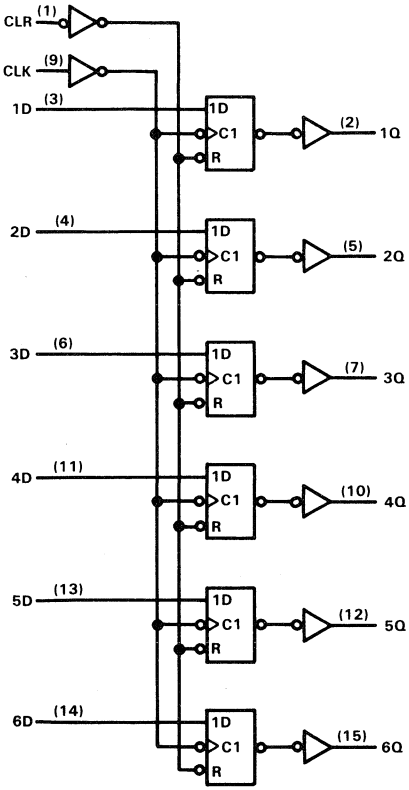
'ALS174, 'AS174

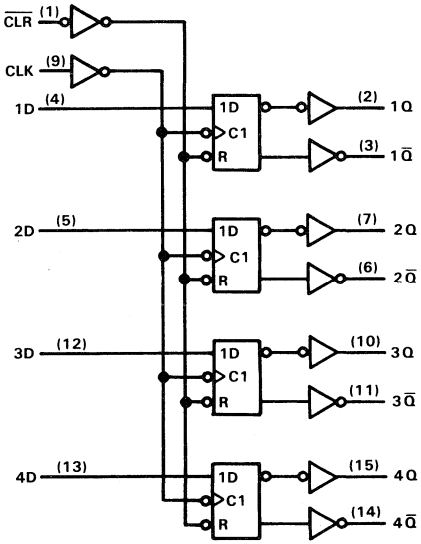


'ALS175, 'AS175



logic diagrams (positive logic)





Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS174, SN54ALS175 . . . . . −55°C to 125°C
SN74ALS174, SN74ALS175 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS174 SN54ALS175			SN74ALS174 SN74ALS175			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		40	0		50	MHz
t_w	Pulse duration	$\overline{CLR}$ low	15			10			ns
		CLK high	12.5			10			
		CLK low	12.5			10			
t_{su}	Setup time	Data	15			10			ns
	before CLK↑	$\overline{CLR}$ inactive	8			6			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS174 SN54ALS175			SN74ALS174 SN74ALS175			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS174	V_{CC} = 5.5 V,	See Note 1		11	19		11	19	mA
	'ALS175				8	14		9	14	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with D inputs and $\overline{CLR}$ grounded, and CLK at 4.5 V.

switching characteristics (see Note 2)

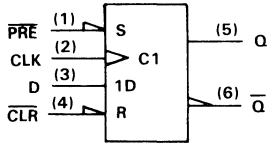
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS174 SN54ALS175		SN74ALS174 SN74ALS175		
			MIN	MAX	MIN	MAX	
f_{max}			40		50		MHz
t_{PLH}	$\overline{CLR}$	Any $\overline{Q}$ ('ALS175)	5	20	5	18	ns
t_{PHL}		Any Q	8	26	8	23	
t_{PLH}	CLK	Any Q	3	17	3	15	ns
t_{PHL}		(or $\overline{Q}$, 'ALS175)	5	20	5	17	

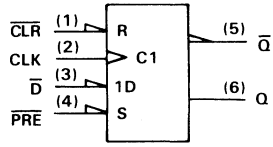
NOTE 2: For load circuit and voltage waveforms, see page 1-12.

D flip-flop signal conventions

It is TI practice to name the outputs and other inputs of a D-type flip-flop and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active low.

In some applications it may be advantageous to redesignate the data input $\overline{D}$. In that case all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.





Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (▷) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 ($\overline{Q}$) is still in phase with the data input $\overline{D}$, but now both are considered active-low.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS174, SN54AS175 . . . . . −55°C to 125°C
SN74AS174, SN74AS175 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

				SN54AS174 SN54AS175			SN74AS174 SN74AS175			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
I_{OH}	High-level output current					−2			−2	mA
I_{OL}	Low-level output current					20			20	mA
f_{clock}	Clock frequency			0		100	0		100	MHz
t_w	Pulse duration	$\overline{CLR}$ low		5.5			5			ns
		CLK high		4			4			
		CLK low	'AS174	6			6			
			'AS175	5			3			
t_{su}	Setup time before CLK↑	Data	'AS174	4			4			ns
			'AS175	3			3			
		$\overline{CLR}$ inactive		6			6			
t_h	Hold time, data after CLK↑			1			1			ns
T_A	Operating free-air temperature			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS174 SN54AS175			SN74AS174 SN74AS175			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS174	V_{CC} = 5.5 V,	See Note 1		30	45		30	45	mA
	'AS175				22.5	34		22.5	34	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with D, CLK, and PRE grounded, then with D, CLK, and CLR grounded.

'AS174 switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS174		SN74AS174		
			MIN	MAX	MIN	MAX	
f_{max}			100		100		MHz
t_{PHL}	$\overline{CLR}$	Any Q	5	15	5	14	ns
t_{PLH}	CLK	Any Q	3.5	9.5	3.5	8	ns
t_{PHL}			4.5	11.5	4.5	10	

'AS175 switching characteristics (see Note 2)

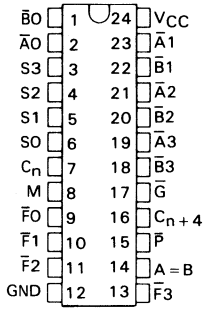
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS175		SN74AS175		
			MIN	MAX	MIN	MAX	
f_{max}			100		100		MHz
t_{PLH}	$\overline{CLR}$	Any Q or $\overline{Q}$	4	10	4	9	ns
t_{PHL}			4.5	15	4.5	13	
t_{PLH}	CLK	Any Q or $\overline{Q}$	4	8.5	4	7.5	ns
t_{PHL}			4	11	4	10	

NOTE 2: For load circuit and voltage waveforms, see page 1-12

D2661, DECEMBER 1982—REVISED DECEMBER 1983

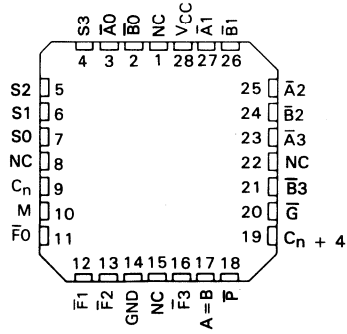
- Package Options Include the 'AS181A in Compact 300-mil or Standard 600-mil DIPs. The 'AS881A is Offered in 300-mil DIPs. Both Devices Are Available in Small Outline (SO) and Plastic and Ceramic Chip Carriers
- Full Look-Ahead for High-Speed Operations on Long Words
- Arithmetic Operating Modes:
  - Addition
  - Subtraction
  - Shift Operand A One Position
  - Magnitude Comparison
  - Plus Twelve Other Arithmetic Operations
- Logic Function Modes
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
  - 'AS881A Provides Status
  - Register Checks
  - Plus Ten Other Logic Operations
- Dependable Texas Instruments Quality and Reliability

SN54AS181A . . . J OR JT PACKAGE
SN54AS881A . . . J PACKAGE
SN74AS181A . . . N OR NT PACKAGE
SN74AS881A . . . NT PACKAGE
(TOP VIEW)



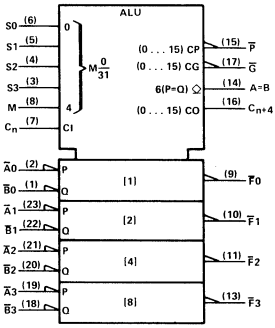
SN54AS181A, SN54AS881A . . . FH OR FK PACKAGE
SN74AS181A, SN74AS881A . . . FN PACKAGE

'AS181A, 'AS881A
(TOP VIEW)



NC – no internal connection

logic symbol



Pin numbers shown are J, JT, N and NT packages.

TYPICAL ADDITION TIMES (C_L = 15 pF, R_L = 280 Ω, T_A = 25°C)

NUMBER OF BITS	ADDITION TIMES USING 'AS881A AND 'AS882	ADDITION TIMES USING 'AS181A AND 'AS882	ADDITION TIMES USING 'S181 AND 'S182	PACKAGE COUNT ARITHMETIC LOGIC UNITS	PACKAGE COUNT LOOK-AHEAD CARRY GENERATORS	CARRY METHOD BETWEEN ALU's
1 to 4	5 ns	5 ns	11 ns	1		NONE
5 to 8	10 ns	10 ns	18 ns	2		RIPPLE
9 to 16	14 ns	14 ns	19 ns	3 or 4	1	FULL LOOK-AHEAD
17 to 64	19 ns	19 ns	28 ns	5 to 16	2 to 5	FULL LOOK-AHEAD

ADVANCE INFORMATION
This document contains information on a new product. Specifications are subject to change without notice.

TEXAS INSTRUMENTS

description

The 'AS181A and 'AS881A are arithmetic logic units (ALU)/function generators that have a complexity of 75 and 77 equivalent gates respectively, on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the SN54AS882 or SN74AS882 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown previously illustrate the little additional time required for addition of longer words when full carry look-ahead is employed. The method of cascading 'AS882 circuits with these ALU's to provide multi-level full carry look-ahead is illustrated under signal designations.

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The 'AS181A and 'AS881A will accommodate active-high or active-low data if the pin designations are interpreted as follows:

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-low data (Table 1)	$\overline{A}0$	$\overline{B}0$	$\overline{A}1$	$\overline{B}1$	$\overline{A}2$	$\overline{B}2$	$\overline{A}3$	$\overline{B}3$	$\overline{F}0$	$\overline{F}1$	$\overline{F}2$	$\overline{F}3$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$
Active-high data (Table 2)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A − B − 1, which requires an end-around or forced carry to provide A − B.

The 'AS181A and 'AS881A can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU must be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

INPUT C_n	OUTPUT C_{n+4}	ACTIVE-LOW DATA (FIGURE 1)	ACTIVE-HIGH DATA (FIGURE 2)
H	H	A ≥ B	A ≤ B
H	L	A < B	A > B
L	H	A > B	A < B
L	L	A ≤ B	A ≥ B

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

description (continued)

The 'AS881A has the same pinout and same functionality as the 'AS181A except for the $\overline{P}$, $\overline{G}$, and C_{n+4} outputs when the device is in the logic mode (M = H).

In the logic mode the 'AS881 provides the user with a status check on the input words, A and B, and the output word F. While in the logic mode the $\overline{P}$, $\overline{G}$ and C_{n+4} outputs supply status information based upon the following logical combinations:

$\overline{P} = F0 + F1 + F2 + F3$
$\overline{G} = H$
$C_{n+4} = PC_n$

FUNCTION TABLE FOR INPUT BITS EQUAL/NOT EQUAL

S0 = S3 = H, S1 = S2 = L, and M = H

C_n	DATA INPUTS				OUTPUTS		
					$\overline{G}$	$\overline{P}$	C_{n+4}
H	A0 = B0	A1 = B1	A2 = B2	A3 = B3	H	L	H
L	A0 = B0	A1 = B1	A2 = B2	A3 = B3	H	L	L
X	A0≠B0	X	X	X	H	H	L
X	X	A1≠B1	X	X	H	H	L
X	X	X	A2≠B2	X	H	H	L
X	X	X	X	A3≠B3	H	H	L

FUNCTION TABLE FOR INPUT PAIRS HIGH/NOT HIGH

S0 = S1 = S3 = L, S2 = H, and M = H

C_n	DATA INPUTS				OUTPUTS		
					$\overline{G}$	$\overline{P}$	C_{n+4}
H	$\overline{A}0$ or $\overline{B}0$ = L	$\overline{A}1$ or $\overline{B}1$ = L	$\overline{A}2$ or $\overline{B}2$ = L	$\overline{A}3$ or $\overline{B}3$ = L	H	L	H
L	$\overline{A}0$ or $\overline{B}0$ = L	$\overline{A}1$ or $\overline{B}1$ = L	$\overline{A}2$ or $\overline{B}2$ = L	$\overline{A}3$ or $\overline{B}3$ = L	H	L	L
X	$\overline{A}0 = \overline{B}0$ = H	X	X	X	H	H	L
X	X	$\overline{A}1 = \overline{B}1$ = H	X	X	H	H	L
X	X	X	$\overline{A}2 = \overline{B}2$ = H	X	H	H	L
X	X	X	X	$\overline{A}3 = \overline{B}3$ = H	H	H	L

The combination of signals on the S3 through S0 control lines determine the operation performed on the data words to generate the output bits Fi. By monitoring the $\overline{P}$ and C_{n+4} outputs, the user can determine if all pairs of input bits are equal (see table above) or if any pair of inputs are both high (see table above). The 'AS881A has the unique feature of providing an A = B status while the exclusive-OR ($\oplus$) function is being utilized. When the control inputs (S3, S2, S1, S0) equal H, L, L, H; a status check is generated to determine whether all pairs (Ai, Bi) are equal in the following manner: $\overline{P} = (A0 \oplus B0) + (A1 \oplus B1) + (A2 \oplus B2) + (A3 \oplus B3)$. This unique bit-by-bit comparison of the data words which is available on the totem pole $\overline{P}$ output is particularly useful when cascading 'AS881's. As the A = B condition is sensed in the first stage the signal is propagated through the same ports used for carry generation in the arithmetic mode ($\overline{P}$ and $\overline{G}$). Thus the A = B status is transmitted to the second stage more quickly without the need for external multiplexing logic. The A = B open-collector output allows the user to check the validity of the bit-by-bit result by comparing the two signals for parity.

If the user wishes to check for any pair of data inputs ($\overline{A}$i, $\overline{B}$i) being high, it is necessary to set the control lines (S3,S2,S1,S0) to L, H, L, L. The data pairs will then be ANDed together and the results ORed in the following manner: $\overline{P} = \overline{A}0\overline{B}0 + \overline{A}1\overline{B}1 + \overline{A}2\overline{B}2 + \overline{A}3\overline{B}3$.

S3	S2	S1	S0	M	$\overline{P} = F0 + F1 + F2 + F3$
L	H	L	L	H	$\overline{A}0\overline{B}0 + \overline{A}1\overline{B}1 + \overline{A}2\overline{B}2 + \overline{A}3\overline{B}3$
H	L	L	H	H	$(A0 \oplus B0) + (A1 \oplus B1) + (A2 \oplus B2) + (A3 \oplus B3)$

signal designations

In both Figures 1 and 2, the polarity indicators (⏤◺) indicate that the associated input or output is active-low with respect to the function shown inside the symbol and the symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-low data, and are for use with the logic functions and arithmetic operations shown in Table 1. The signal designations have been changed in Figure 2 to accommodate the logic functions and arithmetic operations for the active-high data given in Table 2. The 'AS181 and 'AS881 together with the 'AS882 and 'S182 can be used with the signal designation of either Figure 1 or Figure 2.

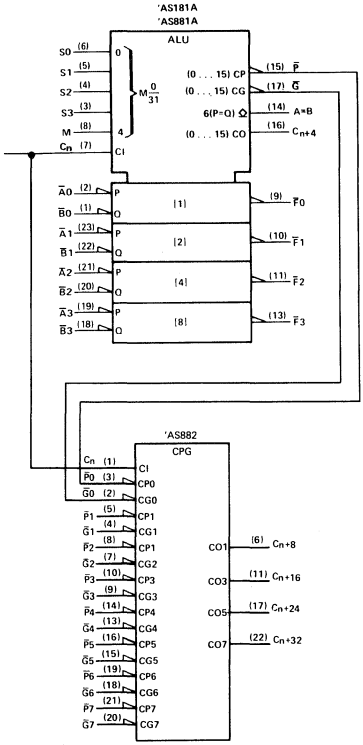


FIGURE 1
(USE WITH TABLE 1)

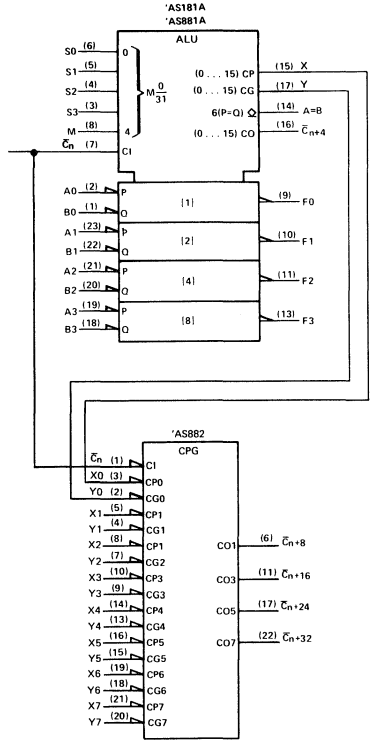


FIGURE 2
(USE WITH TABLE 2)

TABLE 1

SELECTION				ACTIVE-LOW DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	$F = \overline{A}$	F = A MINUS 1	F = A
L	L	L	H	$F = \overline{A+B}$	F = AB MINUS 1	F = AB
L	L	H	L	$F = \overline{A}+B$	F = $A\overline{B}$ MINUS 1	F = $A\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	$F = \overline{A+\overline{B}}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L	H	L	H	$F = \overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L	H	H	L	$F = A \oplus B$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	$F = A+\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H	L	L	L	$F = A\overline{B}$	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	$F = A \oplus B$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = $A\overline{B}$ PLUS (A + B)	F = $A\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = (A + B)	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	$F = A\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	F = $A\overline{B}$ PLUS A	F = $A\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A	F = A PLUS 1

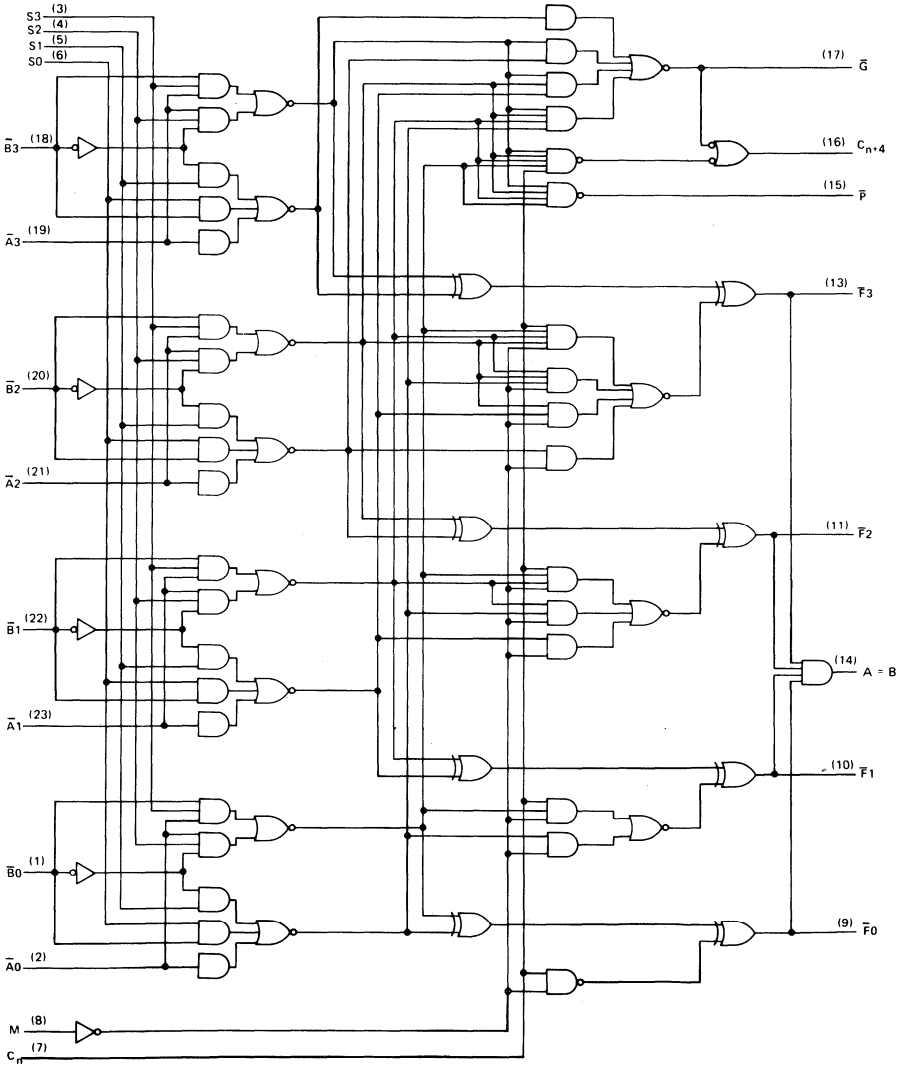
TABLE 2

SELECTION				ACTIVE-HIGH DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	$\overline{C}_n$ = H (no carry)	$\overline{C}_n$ = L (with carry)
L	L	L	L	$F = \overline{A}$	F = A	F = A PLUS 1
L	L	L	H	$F = \overline{A+B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	$F = \overline{A}B$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L	H	L	L	$F = \overline{A\overline{B}}$	F = A PLUS $A\overline{B}$	F = A PLUS $A\overline{B}$ PLUS 1
L	H	L	H	$F = \overline{B}$	F = (A + B) PLUS $A\overline{B}$	F = (A + B) PLUS $A\overline{B}$ PLUS 1
L	H	H	L	$F = A \oplus B$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	$F = A\overline{B}$	F = $A\overline{B}$ MINUS 1	F = $A\overline{B}$
H	L	L	L	$F = \overline{A}+B$	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	$F = \overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

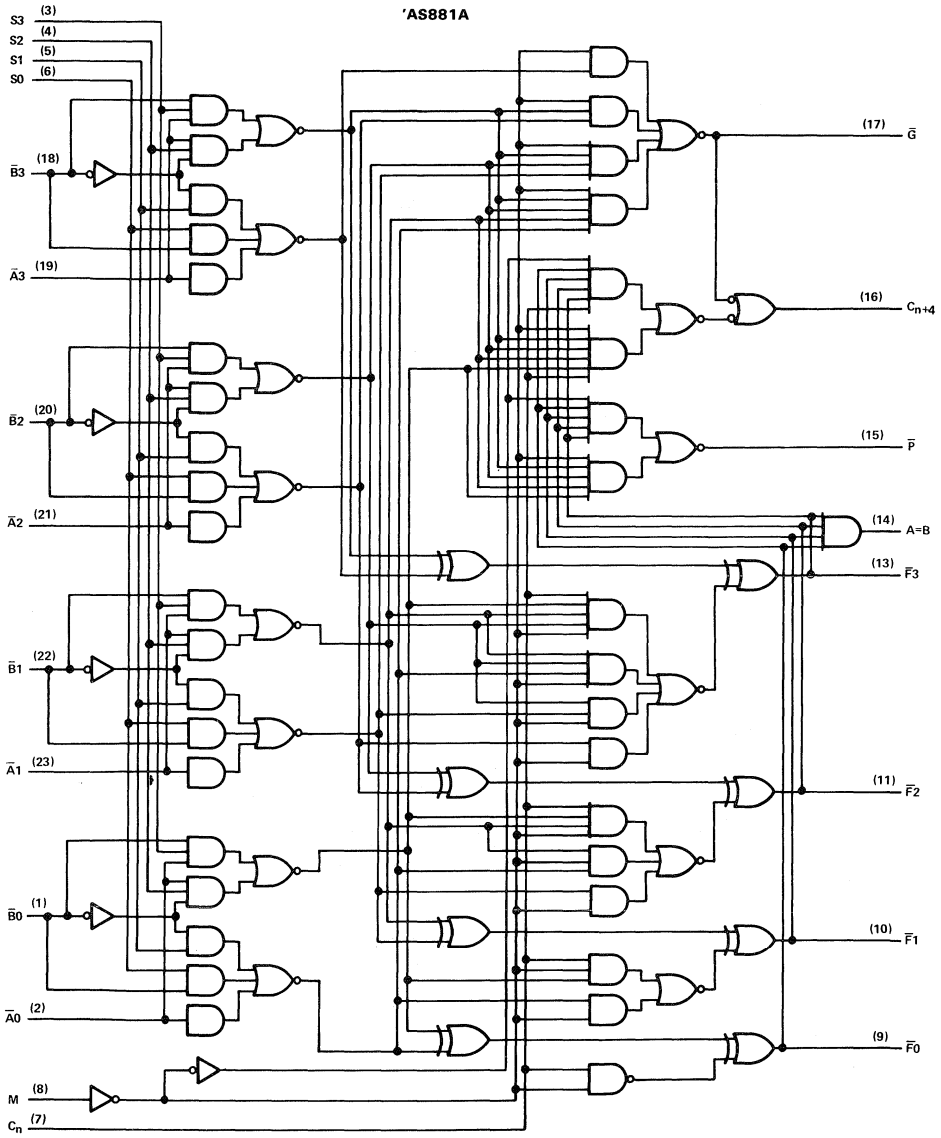
*Each bit is shifted to the next more significant position.

logic diagram (positive logic)

'AS181A



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage (A = B output only) . . . . . 7 V
Operating free-air temperature range: SN54AS181A, SN54AS881A . . . . . −55 °C to 125 °C
SN74AS181A, SN74AS881A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54AS'			SN74AS'			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{OH}	High-level output voltage	A = B output only			5.5			5.5	V
I_{OH}	High-level output current	All outputs except A = B and $\overline{G}$			−2			−2	mA
		$\overline{G}$			−3			−3	mA
I_{OL}	Low-level output current	All outputs except $\overline{G}$			20			20	mA
		$\overline{G}$			48			48	mA
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS'			SN74AS'			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	Any output except A = B	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	$\overline{G}$	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
I_{OH}	A = B	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	Any output except $\overline{G}$	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
	$\overline{G}$	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.4	0.5		0.4	0.5	V
I_I	M input	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	Any A or B input					0.3			0.3	
	Any S input					0.4			0.4	
	Carry input					0.6			0.6	
I_{IH}	M input	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	Any A or B input					60			60	
	Any S input					80			80	
	Carry input					120			120	
I_{IL}	M input	V_{CC} = 5.5 V,	V_I = 0.4 V			−2			−2	mA
	Any A or B input					−6			−6	
	Any S input					−8			−8	
	Carry input					−12			−12	
I_O‡	All outputs except A = B and $\overline{G}$	V_{CC} = 5.5 V,	V_O = 2.25 V	−30	−45	−112	−30	−45	−112	mA
	$\overline{G}$				−165			−165		
I_{CC}		V_{CC} = 5.5 V	'AS181A		135	200		135	200	mA
			'AS881A		135	210		135	210	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω (280 Ω for A = B), T_A = 25 °C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF (15 pF for A = B), R_L = 500 Ω (280 Ω for A = B), T_A = MIN to MAX						UNIT
				'AS181A 'AS881A	SN54AS181A SN54AS881A			SN74AS181A SN74AS881A			
				MIN TYP† MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{pd}	C_n	C_{n+4}		5	2	7	11	2	7	9	ns
t_{pd}	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	M = 0 V, S1 = S2 = 0 V, S0 = S3 = 4.5 V ($\overline{SUM}$ mode)	6	2	8	14	2	8	12	ns
t_{pd}	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)	7	2	8	20	2	8	16	ns
t_{pd}	C_n	Any $\overline{F}$	M = 0 V ($\overline{SUM}$ or $\overline{DIFF}$ mode)	5	3	6	11	3	6	9	ns
t_{pd}	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = 0 V, S1 = S2 = 0 V, S0 = S3 = 4.5 V ($\overline{SUM}$ mode)	4	2	5	9	2	5	7	ns
t_{pd}	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)	5	2	6	12	2	6	9	ns
t_{pd}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	M = 0 V, S1 = S2 = 0 V, S0 = S3 = 4.5 V ($\overline{SUM}$ mode)	5	2	6	11	2	6	8	ns
t_{pd}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)	5	2	6	13	2	6	10	ns
t_{pd}	$\overline{A}$i or $\overline{B}$i	$\overline{F}$i	M = 0 V, S1 = S2 = 0 V, S0 = S3 = 4.5 V ($\overline{SUM}$ mode)	5	2	5	11	2	5	8	ns
t_{pd}	$\overline{A}$i or $\overline{B}$i	$\overline{F}$i	M = 0 V, S0 = S1 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)	5	2	6	12	2	6	10	ns
t_{pd}	$\overline{A}$i or $\overline{B}$i	$\overline{F}$i	M = 4.5 V (LOGIC mode)	6	2	6	16	2	6	11	ns
t_{pd}	Any A or B	A = B	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)	12	4	14	26	4	14	21	ns

addditional 'AS881A switching characteristics involving status checks (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC} = 5 V, C_L = 15 pF, R_L = 500 Ω, T_A = 25 °C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
				'AS881A	SN54AS881A			SN74AS881A			
				MIN TYP† MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{pd}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	C_n = 4.5V, M = 4.5 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V, Equality ($\overline{A}$i = $\overline{B}$i or $\overline{A}$i≠$\overline{B}$i)	8	2	10	19	2	10	15	ns
t_{pd}	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	C_n = 4.5 V, M = 4.5 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V, Equality ($\overline{A}$i = $\overline{B}$i or $\overline{A}$i≠$\overline{B}$i)	10	2	12	24	2	12	18	ns
t_{pd}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	C_n = 4.5 V, M = 4.5 V, S2 = 4.5 V, S0 = S1 = S3 = 0 V, ($\overline{A}$i = $\overline{B}$i = H or $\overline{A}$i or $\overline{B}$i = L)	8	2	10	19	2	10	15	ns
t_{pd}	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	C_n = 4.5 V, M = 4.5 V, S2 = 4.5 V, S0 = S1 = S3 = 0 V, ($\overline{A}$i = $\overline{B}$i = H or $\overline{A}$i or $\overline{B}$i = L)	11	2	13	25	2	13	19	ns

t_{pd} = t_{PHL} or t_{PLH}
†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

PARAMETER MEASUREMENT INFORMATION

$\overline{\text{SUM}}$ MODE TEST TABLE

FUNCTION INPUTS: S0 = S3 = 4.5 V, S1 = S2 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE A)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PLH} / t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase

$\overline{\text{DIFF}}$ MODE TEST TABLE

FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE A)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$A = B$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$A = B$	Out-of Phase
t_{PLH} / t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4} or any $\overline{F}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_{n+4}	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_{n+4}	In -Phase

NOTE A: For load circuit and voltage waveforms, see page 1-12.

PARAMETER MEASUREMENT INFORMATION

LOGIC MODE TEST TABLE
FUNCTION INPUTS: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE A)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	Out-ot-Phase

INPUT BITS EQUAL/NOT EQUAL TEST TABLE
FUNCTION INPUTS: S0 = S3 = M = 4.5 V, S1 = S2 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE A)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	In-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}	In-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}	Out-of-Phase

INPUT PAIRS HIGH/NOT HIGH TEST TABLE
FUNCTION INPUTS: S2 = M = 4.5 V, S0 = S1 = S3 = 0V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (SEE NOTE A)
		APPLY 4.5 V	APPLY GND	APPLY 4.5V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$, C_n	Remaining $\overline{B}$	$\overline{P}$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{P}$	In-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$, C_n	Remaining $\overline{B}$	C_{n+4}	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	C_{n+4}	Out-of-Phase

NOTE A: For load circuit and voltage waveforms, see page 1-12.

D2661, DECEMBER 1983

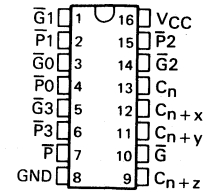
- **High-Speed Replacement for the 'S182**
- **Offers Carry Functions in a Compatible Form for Direct Connections to the ALU**
- **Cascadable to Perform Look-Ahead Across n-Bit Adders**
- **Dependable Texas Instruments Quality and Reliability**

PIN DESIGNATIONS

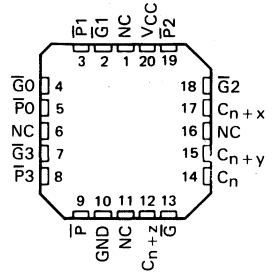
ALTERNATIVE	DESIGNATIONS†	FUNCTION
$\overline{G0}$, $\overline{G1}$, $\overline{G2}$, $\overline{G3}$	G0, G1, G2, G3	Carry Generate Inputs
$\overline{P0}$, $\overline{P1}$, $\overline{P2}$, $\overline{P3}$	P0, P1, P2, P3	Carry Propagate Inputs
C_n	$\overline{C}_n$	Carry Input
C_{n+x}, C_{n+y}, C_{n+z}	$\overline{C}_{n+x}$, $\overline{C}_{n+y}$, $\overline{C}_{n+z}$	Carry Outputs
$\overline{G}$	Y	Carry Generate Output
$\overline{P}$	X	Carry Propagate Output
V_{CC}		Supply Voltage
GND		Ground

† Interpretations are illustrated in connection with the Function Tables for the 'AS181A and 'AS881A.

SN54AS182 . . . J PACKAGE
SN74AS182 . . . N PACKAGE
SN74AS182 . . . D PACKAGE
(TOP VIEW)



SN54AS182 . . . FH OR FK PACKAGE
SN74AS182 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

The 'AS182 look-ahead carry generators are capable of anticipating a carry across four binary adders or group of adders. They are cascadable to perform full look-ahead across n-bit adders.

This generator, when used in conjunction with the 'AS181 or 'AS881 Arithmetic Logic Unit ALU, provides high-speed carry look-ahead capability for any word length. The 'AS182 generates the look-ahead (anticipated carry) across a group of four ALUs. In addition, other carry look-ahead circuits may be employed to anticipate carry-across sections of four look-ahead packages up to n-bits. The method of cascading 'AS182 circuits to perform multilevel look-ahead is illustrated under the typical application data.

The carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connections to the ALU. Reinterpretations of carry functions as explained on the 'AS181A and 'AS881A data sheet are also applicable to and compatible with the look-ahead generator. Logic equations for the 'AS182 are:

$$C_{n+x} = G0 + P0\,C_n$$
$$C_{n+y} = G1 + P1\,G0 + P1\,P0\,C_n$$
$$C_{n+z} = G2 + P2\,G1 + P2\,P1\,G0 + P2\,P1\,P0\,C_n$$
$$\overline{G} = \overline{G3 + P3\,G2 + P3\,P2\,G1 + P3\,P2\,P1\,G0}$$
$$\overline{P} = \overline{P3\,P2\,P1\,P0}$$

or

$$\overline{C}_{n+x} = \overline{Y0\,(X0 + C_n)}$$
$$\overline{C}_{n+y} = \overline{Y1\,[X1 + Y0\,(X0 + C_n)]}$$
$$\overline{C}_{n+z} = \overline{Y2\,\{X2 + Y1\,[X1 + Y0\,(X0 + C_n)]\}}$$
$$Y = Y3\,(X3 + Y2)\,(X3 + X2 + Y1)\,(X3 + X2 + X1 + Y0)$$
$$X = X3 + X2 + X1 + X0$$

PRODUCT PREVIEW

This page contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

FUNCTION TABLE FOR $\overline{G}$ OUTPUT

INPUTS							OUTPUT
$\overline{G}3$	$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All other combinations							H

FUNCTION TABLE FOR $\overline{P}$ OUTPUT

INPUTS				OUTPUT
$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	$\overline{P}$
L	L	L	L	L
All other combinations				H

FUNCTION TABLE FOR C_{n+x} OUTPUT

INPUTS			OUTPUT
$\overline{G}0$	$\overline{P}0$	Cn	C_{n+x}
L	X	X	H
X	L	H	H
All other combinations			L

FUNCTION TABLE C_{n+y} OUTPUT

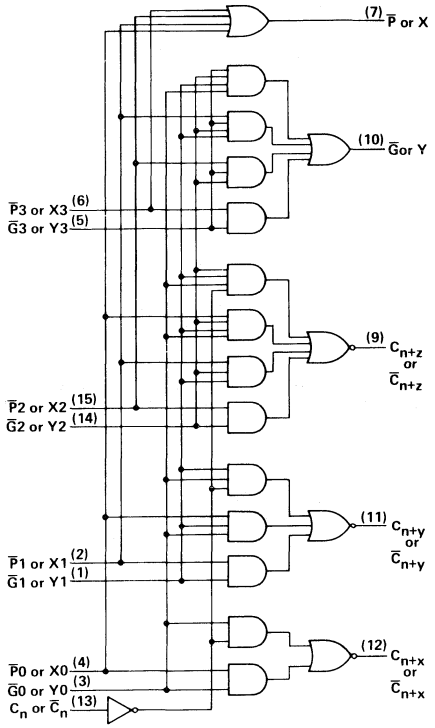
INPUTS					OUTPUT
$\overline{G}1$	$\overline{G}0$	$\overline{P}1$	$\overline{P}0$	C_n	C_{n+y}
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

FUNCTION TABLE FOR C_{n+z} OUTPUT

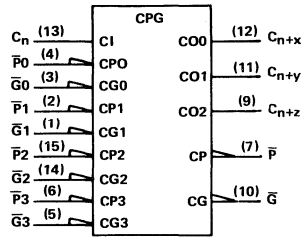
INPUTS							OUTPUT
$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	C_n	C_{n+z}
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All other combinations							L

H = High-level, L = Low-level, = Irrelevant
Any inputs not shown in a given table are irrelevant with respect to that output.

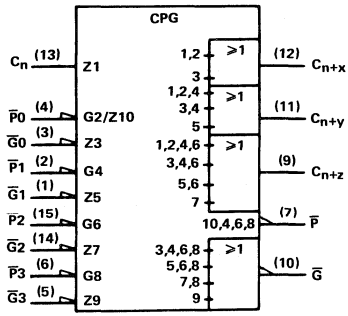
logic diagram (positive logic)



logic symbols



OR



Pin numbers shown are for J and N packages only.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS182 . . . . . −55°C to 125°C
SN74AS182 . . . . . 0°C to 70°CC
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS182			SN74AS182			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70°	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS182			SN74AS182			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I	C_n	V_{CC} = 5.5 V,	V_I = 7.0 V			0.1			0.1	mA
	$\overline{P}3$					0.2			0.2	
	$\overline{P}2$					0.3			0.3	
	$\overline{P}0$, $\overline{P}1$, $\overline{G}3$					0.4			0.4	
	$\overline{G}0$, $\overline{G}2$					0.7			0.7	
	$\overline{G}1$					0.8			0.8	
I_{IH}	C_n	V_{CC} = 5.5 V,	V_I = 2.7 V			0.02			0.02	mA
	$\overline{P}3$					0.04			0.04	
	$\overline{P}2$					0.06			0.06	
	$\overline{P}0$, $\overline{P}1$, $\overline{G}3$					0.08			0.08	
	$\overline{G}1$, $\overline{G}2$					0.14			0.14	
	$\overline{G}1$					0.16			0.16	
I_{IL}	C_n	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	$\overline{P}3$					−1			−1	
	$\overline{P}2$					−1.5			−1.5	
	$\overline{P}2$, $\overline{P}1$, $\overline{G}3$					−2			−2	
	$\overline{G}0$, $\overline{G}2$					−3.5			−3.5	
	$\overline{G}1$					−4			−4	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}		V_{CC} = 5.5 V			17			17		mA
I_{CCL}					23			23		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS182			SN74AS182			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	C_n	C_{n+y}, C_{n+y}		5			5		ns
t_{PHL}		C_{n+z}		5			5		
t_{PLH}	$\overline{P}$ or $\overline{G}$	C_{n+x}, C_{n+y}		5			5		ns
t_{PHL}		C_{n+z}		5			5		
t_{PLH}	$\overline{P}$ or $\overline{G}$	$\overline{G}$		6			6		ns
t_{PHL}				5			5		
t_{PLH}	$\overline{P}$	$\overline{P}$		5			5		ns
t_{PHL}				5			5		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TYPICAL APPLICATION DATA

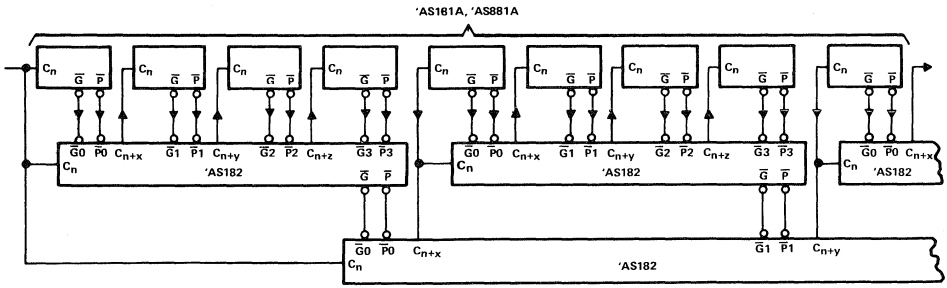


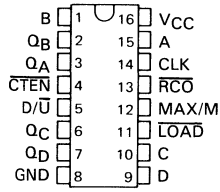
FIGURE 1—THE 'AS182 IN A 64-BIT LOOK-AHEAD CARRY CIRCUIT

TYPES SN54ALS190, SN54ALS191, SN74ALS190, SN74ALS191
SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS

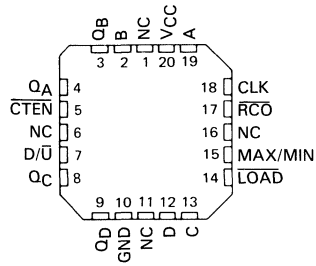
D2661, DECEMBER 1982—REVISED DECEMBER 1983

- **Single Down/Up Count Control Line**
- **Look-Ahead Circuitry Enhances Speed of Cascaded Counters**
- **Fully Synchronous in Count Modes**
- **Asynchronously Presettable with Load Control**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS190, SN54ALS191 . . . J PACKAGE
SN74ALS190, SN74ALS191 . . . N PACKAGE
SN74ALS190, SN74ALS191 . . . D PACKAGE
(TOP VIEW)



SN54ALS190, SN54ALS191 . . . FH OR FK PACKAGE
SN74ALS190, SN74ALS191 . . . FN PACKAGE
(TOP VIEW)



NC — no internal connection.

descriptions

The 'ALS190 and 'ALS191 are synchronous, reversible up/down counters. The 'ALS190 is a 4-bit decade counter and the 'ALS191 is a 4-bit binary counter. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input ($\overline{CTEN}$) is low. A high at $\overline{CTEN}$ inhibits counting. The direction of the count is determined by the level of the down/up (D/$\overline{U}$) input. When D/$\overline{U}$ is low, the counter counts up and when D/$\overline{U}$ is high, it counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs ($\overline{CTEN}$ and D/$\overline{U}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

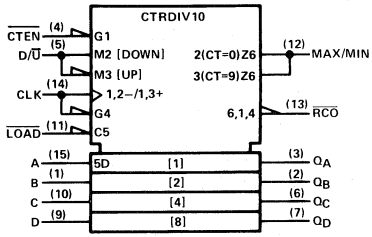
These counters are fully programmable; that is, the outputs may each be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The CLK, D/$\overline{U}$, and LOAD inputs are buffered to lower the drive requirement, which significantly reduces the loading on, or current required by, clock drivers, etc., for long parallel words.

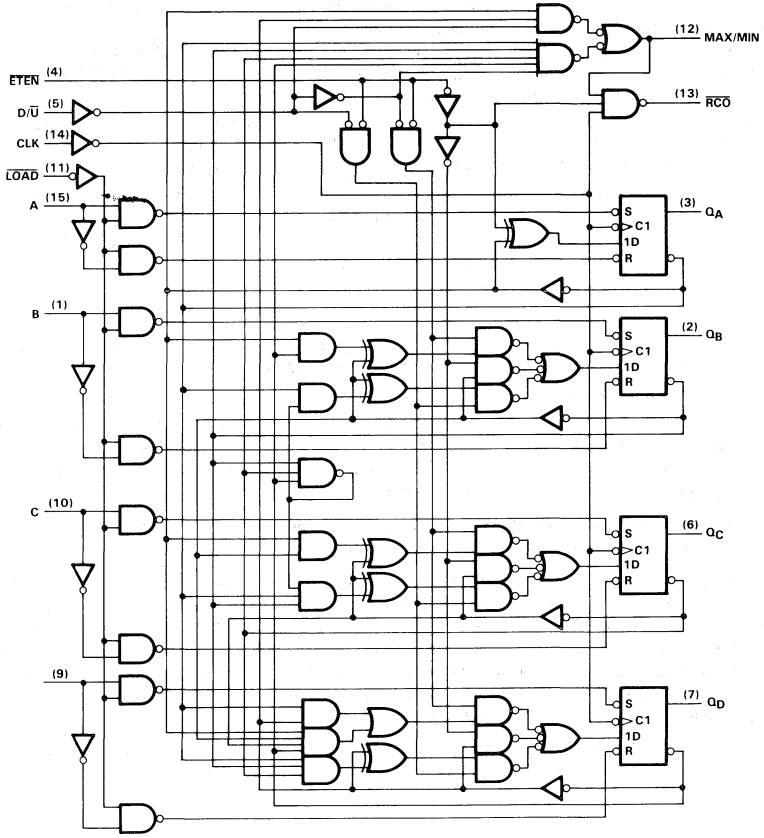
Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (9 or 15) counting up. The ripple clock output produces a low-level output pulse under those same conditions but only while the clock input is low. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

The SN54ALS190 and SN54ALS191 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS190 and SN74ALS191 are characterized for operation from 0 °C to 70 °C.

'ALS190 logic symbol

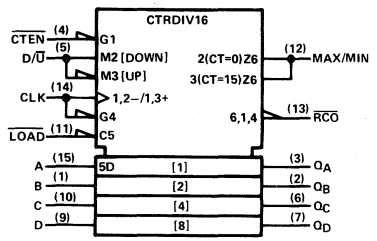


'ALS190 logic diagram (positive logic)

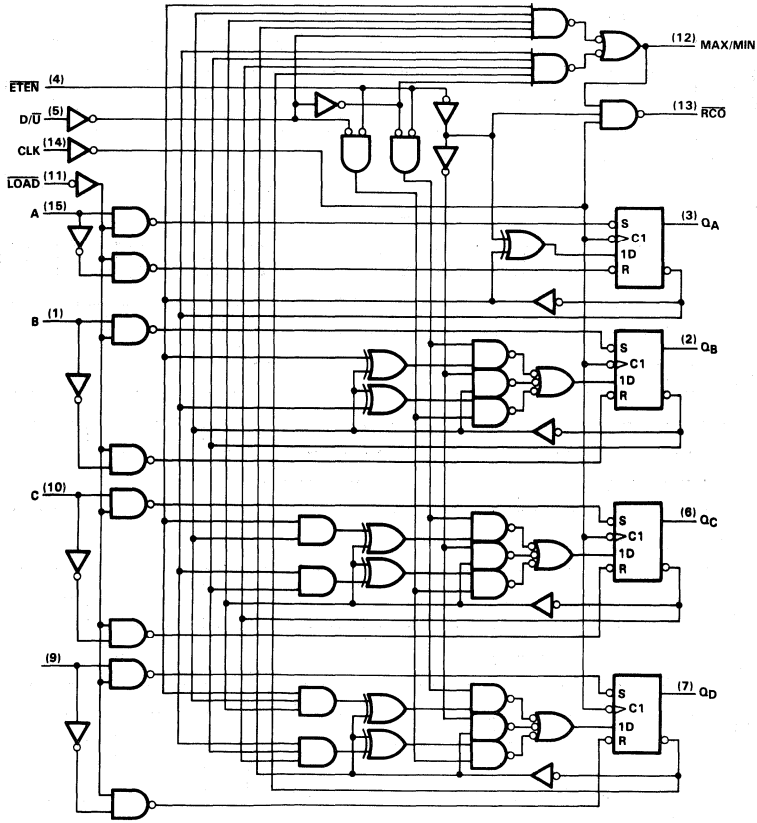


Pin numbers shown are for J and N packages.

'ALS191 logic symbol



'ALS191 logic diagram (positive logic)



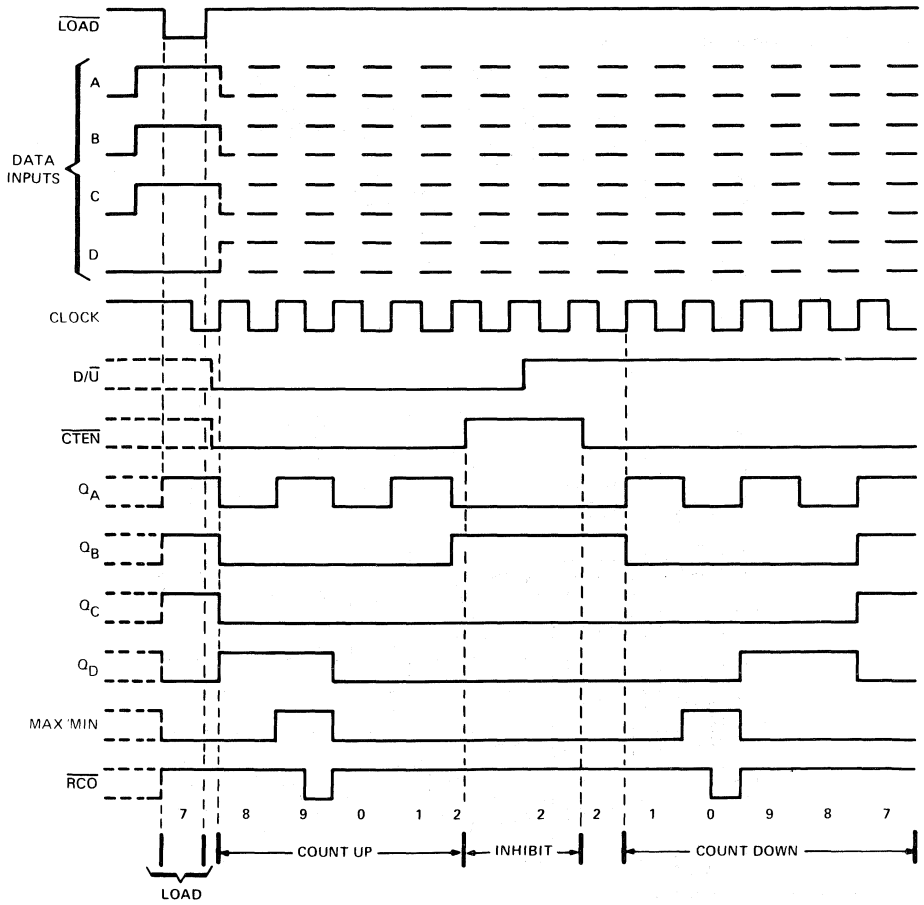
Pin numbers shown are for J and N packages.

typical load, count, and inhibit sequences

'ALS190

Illustrated below is the following sequence:

1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), nine, eight, and seven.

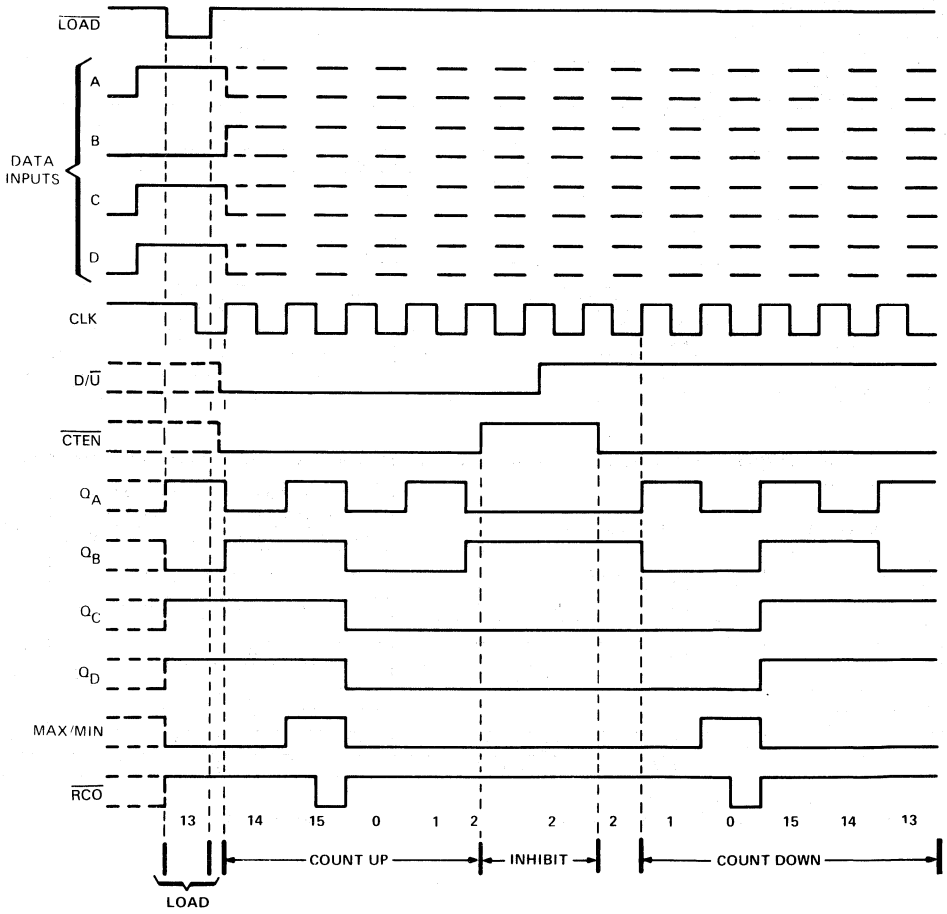


typical load, count, and inhibit sequences

'ALS191

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS190, SN54ALS191 . . . . . −55 °C to 125 °C
SN74ALS190, SN74ALS191 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

				SN54ALS190 SN54ALS191			SN74ALS190 SN74ALS191			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
I_{OH}	High-level output current					−0.4			−0.4	mA
I_{OL}	Low-level output current					4			8	mA
f_{clock}	Clock frequency	'ALS190		0		20	0		25	MHz
		'ALS191		0		25	0		30	
t_w	Pulse duration	CLK high or low	'ALS190	25			20			ns
			'ALS191	20			16.5			
		$\overline{LOAD}$ low		25			20			
t_{su}	Setup time	Data before $\overline{LOAD}$↑		25			20			ns
		$\overline{CTEN}$ before CLK↑		25			20			
		D/$\overline{U}$ before CLK↑		20			20			
		$\overline{LOAD}$ inactive before CLK↑		20			20			
t_h	Hold time	Data after $\overline{LOAD}$↑		5			5			ns
		$\overline{CTEN}$ after CLK↑		0			0			
		D/$\overline{U}$ after CLK↑		0			0			
T_A	Operating free-air temperature			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS190 SN54ALS191			SN74ALS190 SN74ALS191			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	$\overline{CTEN}$ or CLK	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	All others					−0.1			−0.1	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	All inputs at 0 V		12	22		12	22	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS190 SN54ALS191		SN74ALS190 SN74ALS191		
			MIN	MAX	MIN	MAX	
f_{max}	'ALS190		20		25		MHz
	'ALS191		25		30		
t_{PLH}	$\overline{LOAD}$	Any Q	8	34	8	30	ns
t_{PHL}			8	34	8	30	
t_{PLH}	A, B, C, D	Any Q	4	25	4	21	ns
t_{PHL}			4	25	4	21	
t_{PLH}	CLK	$\overline{RCO}$	5	24	5	20	ns
t_{PHL}			5	24	5	20	
t_{PLH}	CLK	Any Q	3	22	3	18	ns
t_{PHL}			3	22	3	18	
t_{PLH}	CLK	MAX/MIN	8	34	8	31	ns
t_{PHL}			8	34	8	31	
t_{PLH}	D/$\overline{U}$	$\overline{RCO}$	15	42	15	37	ns
t_{PHL}			10	33	10	28	
t_{PLH}	D/$\overline{U}$	MAX/MIN	8	30	8	25	ns
t_{PHL}			8	30	8	25	
t_{PLH}	$\overline{CTEN}$	$\overline{RCO}$	4	21	4	18	ns
t_{PHL}			4	21	4	18	

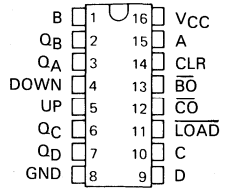
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TYPES SN54ALS192, SN54ALS193, SN74ALS192, SN74ALS193
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

D2661, DECEMBER 1982—REVISED DECEMBER 1983

- **Look-Ahead Circuitry Enhances Cascaded Counters**
- **Fully Synchronous in Count Modes**
- **Parallel Asynchronous Load for Modulo-N Count Lengths**
- **Asynchronous Clear**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS192, SN54ALS193 . . . J PACKAGE
SN74ALS192, SN74ALS193 . . . N PACKAGE
SN74ALS192, SN74ALS193 . . . D PACKAGE
(TOP VIEW)



2

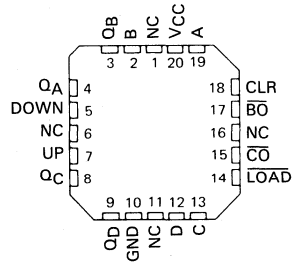
description

The 'ALS192 and 'ALS193 are synchronous, reversible up/down counters. The 'ALS192 is a 4-bit decade counter and the 'ALS193 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered by a low-to-high-level transition of either count (clock) input (Up or Down). The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

SN54ALS192, SN54ALS193 . . . FH OR FK PACKAGE
SN74ALS192, SN74ALS193 . . . FN PACKAGE
(TOP VIEW)



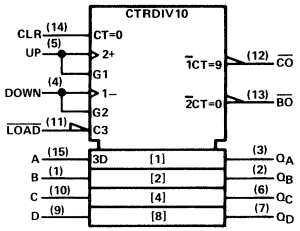
NC — no internal connection.

A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs. The clock, count, and load inputs are buffered to lower the drive requirements. This significantly reduces the loading on clock drivers, etc., for long parallel words.

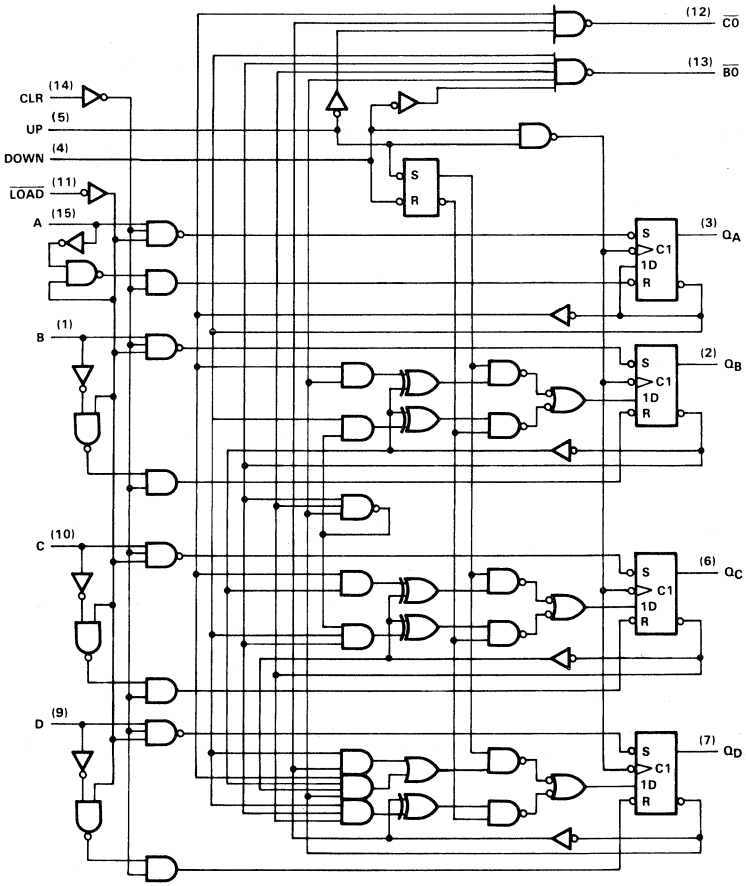
These counters were designed to be cascaded without the need for external circuitry. The borrow output (BO) produces a low-level pulse while the count is zero (all outputs low) and the count-down input is low. Similarly, the carry output ($\overline{CO}$) produces a low-level pulse while the count is maximum (9 or 15) and the count-up input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs, respectively, of the succeeding counter.

The SN54ALS192 and SN54ALS193 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS192 and SN74ALS193 are characterized for operation from 0 °C to 70 °C.

'ALS192 logic symbol

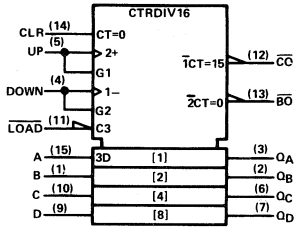


'ALS192 logic diagram (positive logic)

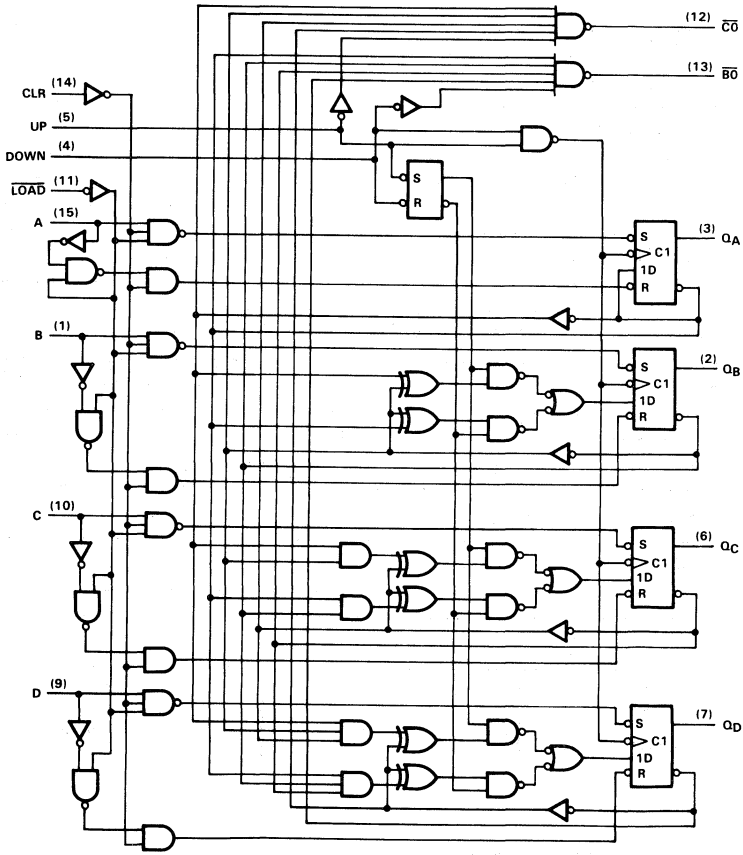


Pin numbers shown are for J and N packages.

'ALS193 logic symbol



'ALS193 logic diagrams (positive logic)



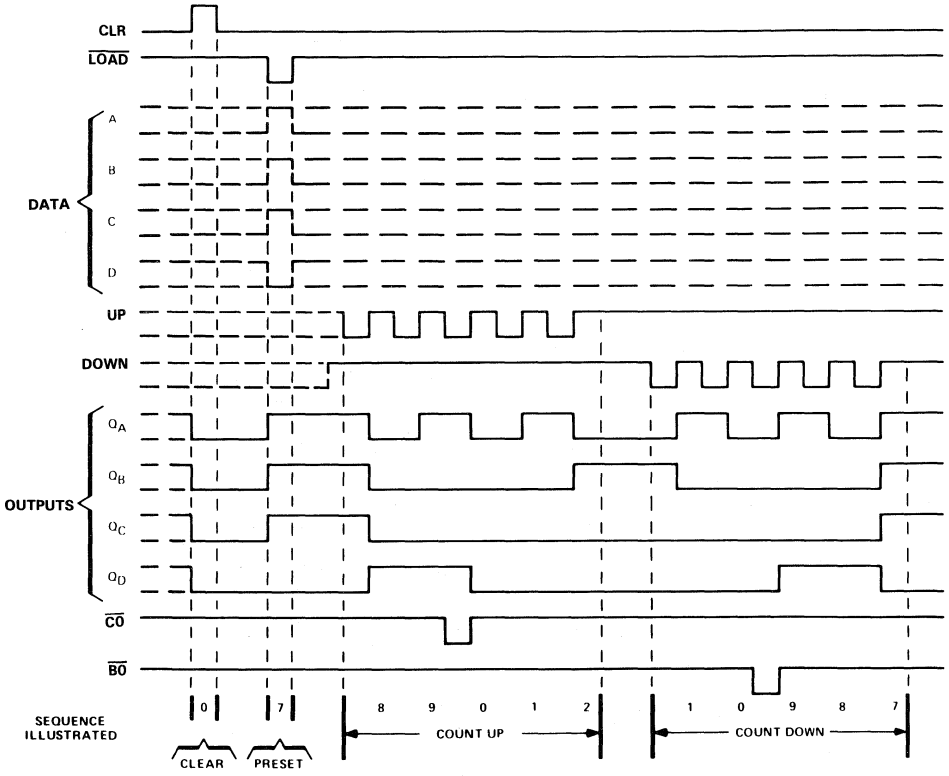
Pin numbers shown are for J and N packages.

typical clear, load, and count sequence

'ALS192

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.



NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

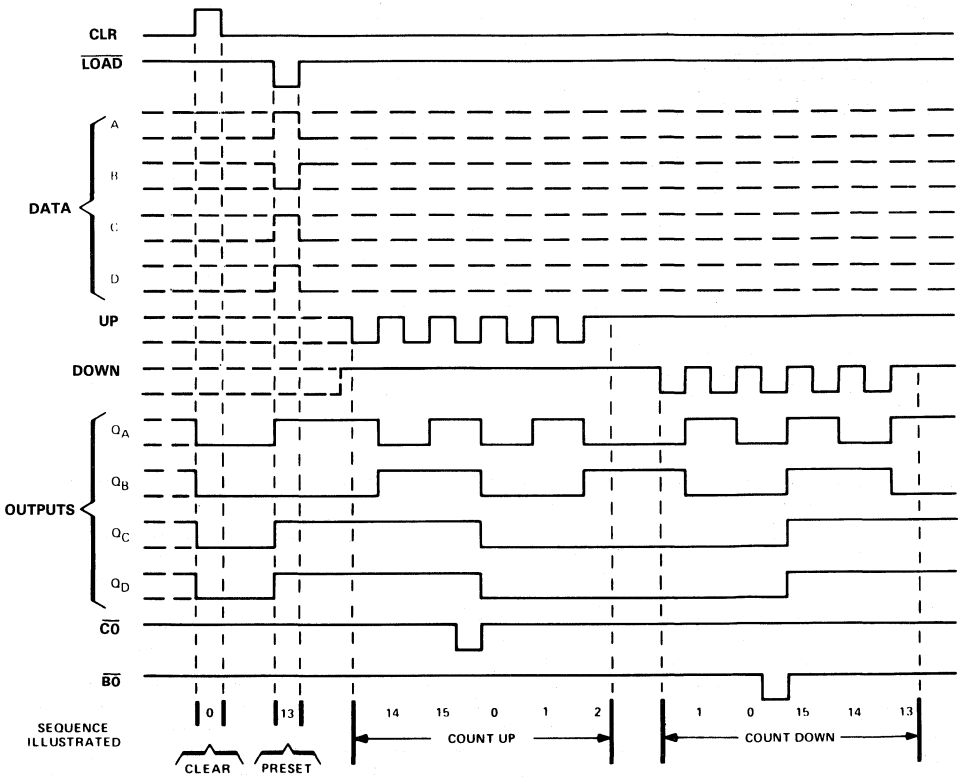
typical clear, load, and count sequences

'ALS193

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.

2



NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS192, SN54ALS193 . . . . . −55 °C to 125 °C
SN74ALS192, SN74ALS193 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

				SN54ALS192 SN54ALS193			SN74ALS192 SN74ALS193			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
I_{OH}	High-level output current					−0.4			−0.4	mA
I_{OL}	Low-level output current					4			8	mA
f_{clock}	Clock frequency	'ALS192		0		20	0		25	MHz
		'ALS193		0		25	0		30	
t_w	Pulse duration	CLR high		10			10			ns
		$\overline{LOAD}$ low		25			20			
		UP or DOWN high or low	'ALS192	25			20			ns
			'ALS193	20			16.5			
t_{su}	Setup time	Data before $\overline{LOAD}$↑		25			20			ns
		CLR inactive before UP↑ or DOWN↑		20			20			
		$\overline{LOAD}$ inactive before UP↑ or DOWN↑		20			20			
t_h	Hold time	Data after $\overline{LOAD}$↑		5			5			ns
		UP high after DOWN↑		0			0			
		DOWN high after UP↑		0			0			
T_A	Operating free-air temperature			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS192 SN54ALS193			SN74ALS192 SN74ALS193			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	UP, DOWN	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	All others					−0.1			−0.1	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		12	22		12	22	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with the clear and load inputs grounded, and all other inputs at 4.5 V.

switching characteristics (see Note 2)

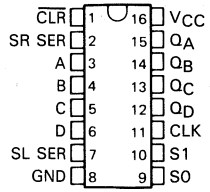
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS192 SN54ALS193		SN74ALS192 SN74ALS193		
			MIN	MAX	MIN	MAX	
f_{max}	'ALS192		20		25		MHz
	'ALS193		25		30		
t_{PLH}	Up	CO	4	19	4	16	ns
t_{PHL}			5	21	5	18	
t_{PLH}	Down	BO	4	19	4	16	ns
t_{PHL}			5	21	5	18	
t_{PLH}	Up or Down	Any Q	4	23	4	19	ns
t_{PHL}			4	20	4	17	
t_{PLH}	$\overline{LOAD}$	Any Q	8	35	8	30	ns
t_{PHL}			8	31	8	28	
t_{PHL}	CLR	Any Q	5	20	5	17	ns

NOTE 2: For load circuit and voltage waveforms, see page 1-12.

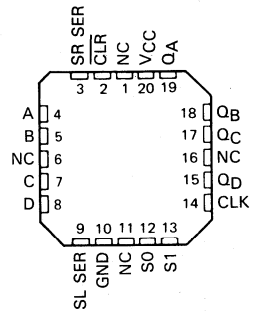
D2661, DECEMBER 1983—REVISED NOVEMBER 1984

- **Parallel-to-Serial, Serial-to-Parallel Conversions**
- **Left or Right Shifts**
- **Parallel Synchronous Loading**
- **Direct Overriding Clear**
- **Temporary Data Latching Capability**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS194 . . . J PACKAGE
SN74AS194 . . . N PACKAGE
SN74AS194 . . . D PACKAGE
(TOP VIEW)



SN54AS194 . . . FH OR FK PACKAGE
SN74AS194 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

These bidirectional shift registers feature parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Inhibit clock (temporary data latch/do nothing
Shift-right (in the direction Q_A toward Q_D)
Shift-left (in the direction Q_D toward Q_A)
Parallel (broadside) load

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift-right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial inputs. Clocking of the flip-flop is inhibited when both mode control inputs are low.

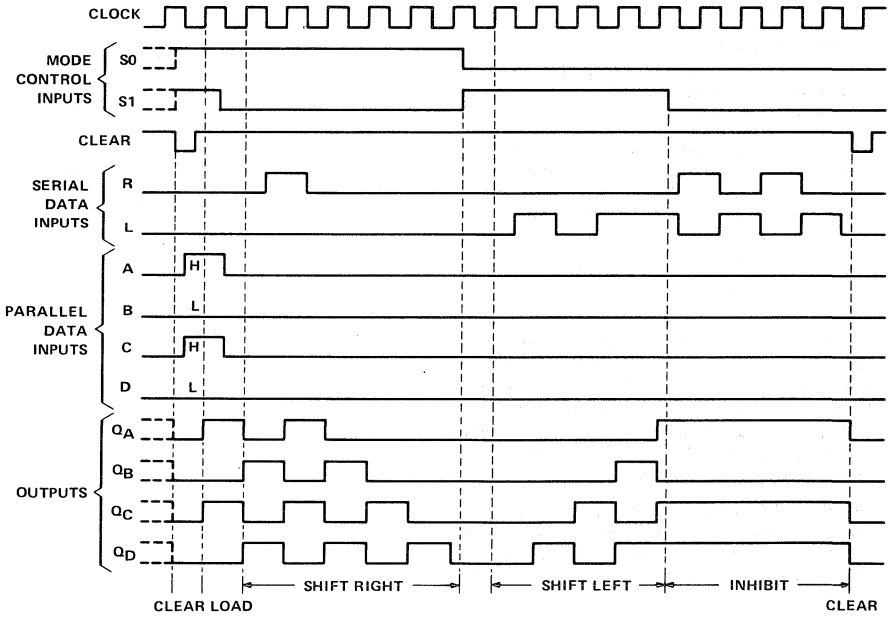
The SN54AS194 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS194 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

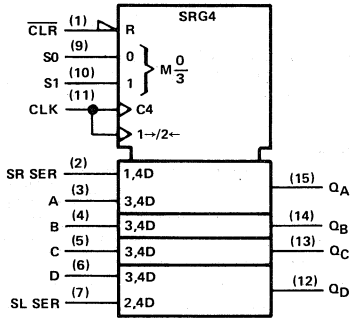
INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, respectively, before the most-recent ↑ transition of the clock.

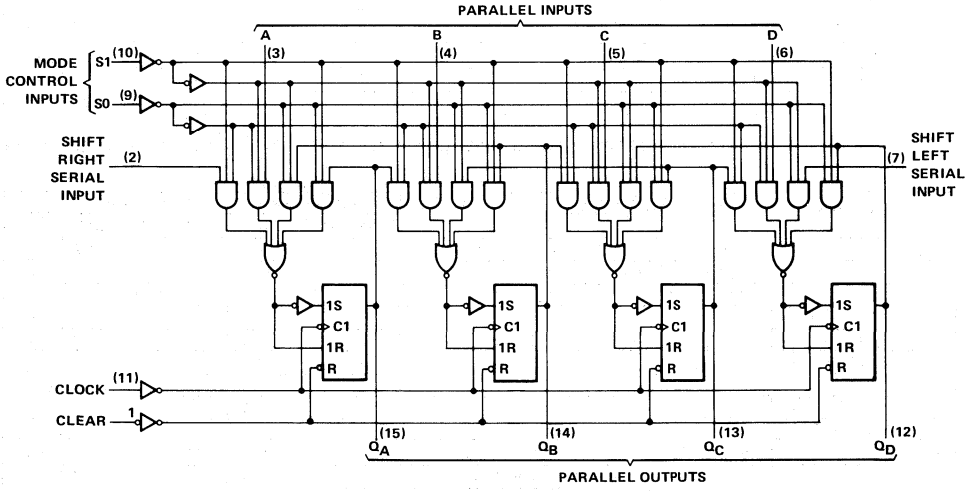
typical clear, load, right-shift, inhibit, and clear sequences



logic symbol



logic diagram (positive logic)



Pin numbers shown are for J and N package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS194 . . . . . −55°C to 125°C
SN74AS194 . . . . . 0°C to 150°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS194			SN74AS194			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0		75	0		80	MHz
t_w	Pulse duration	$\overline{CLR}$	4			4			ns
		CLK high	2			2			
		CLK low	6			6			
t_{su}	Set-up time before CLK↑	Select	9			8			ns
		Data	3.5			3			
t_{wr}	Recovery time	$\overline{CLR}$	6			6			ns
t_h	Hold time, data after CLK↑		0.5			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS194			SN74AS194			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	Data, CLK, $\overline{CLR}$	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	Mode, SL, SR					0.2			0.2	
I_{IH}	Data, CLK, $\overline{CLR}$	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	Mode, SL,SR					40			40	
I_{IL}	Data, CLK, $\overline{CLR}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	Mode, SL, SR					−1			−1	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	Outputs high		30	49		30	43	mA
			Outputs low		38	60		38	53	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS194		SN74AS194		
			MIN	MAX	MIN	MAX	
f_{max}			75		80		MHz
t_{PLH}	CLK	Any Q	2.5	8	3	7	ns
t_{PHL}			2.5	8	3	7	
t_{PHL}	$\overline{CLR}$	Any Q	3.5	13	4	12	ns

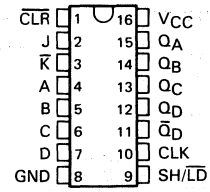
NOTE 1: For load circuit and voltage waveforms, see page 1-12

2

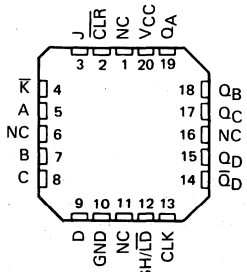
D2661, DECEMBER 1983

- **Parallel-to-Serial, Serial-to-Parallel Conversions**
- **Parallel Synchronous Loading**
- **J and $\overline{K}$ Inputs to First Stage**
- **Right-Shift Only with Complementary Outputs on Last Stage**
- **Direct Overriding Clear**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS195 . . . J PACKAGE
SN74AS195 . . . N PACKAGE
SN74AS195 . . . D PACKAGE
(TOP VIEW)



SN54AS195 . . . FH OR FK PACKAGE
SN74AS195 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

These 4-bit registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation:

Parallel (broadside) load
Shift (in the direction Q_A toward Q_D)

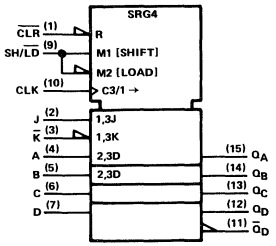
Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D-, or T-type flip-flop as shown in the function table.

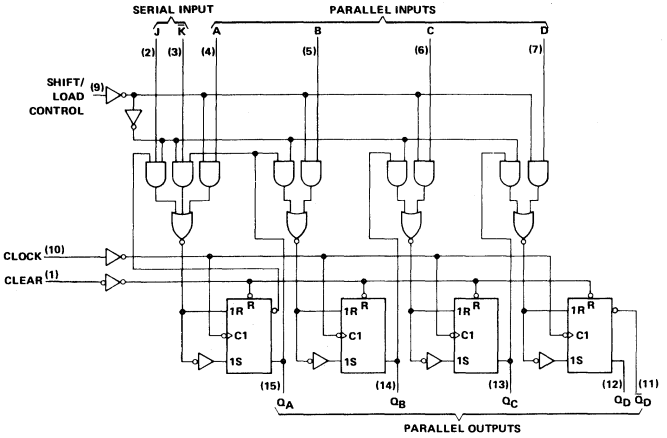
The SN54AS195 is characterized for operation over the full military range of −55°C to 125°C. The SN74AS195 is characterized for operation from 0°C to 70°C.

PRODUCT PREVIEW

logic symbol



logic diagram (positive logic)

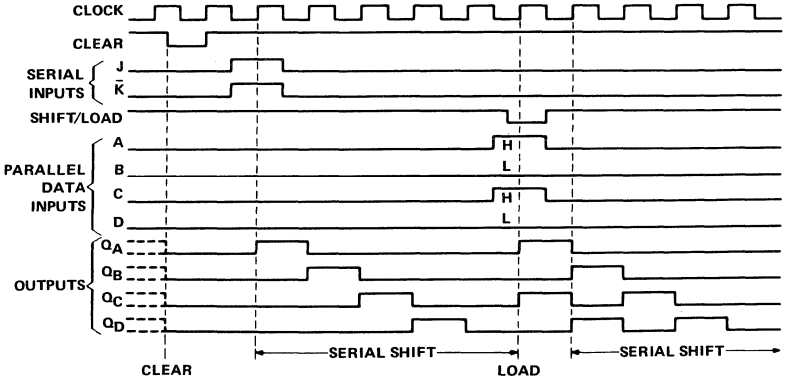


Pin numbers shown are for J and N packages.

FUNCTION TABLE

INPUTS									OUTPUTS				
CLEAR	SHIFT/LOAD	CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D	$\bar{Q}_D$
			J	$\bar{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	L
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\bar{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\bar{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\bar{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\bar{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\bar{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\bar{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\bar{Q}_{Cn}$

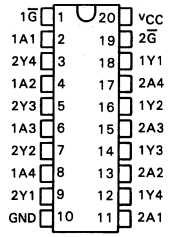
typical clear, shift, and load sequences



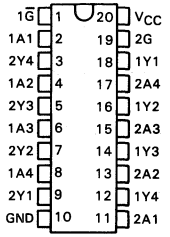
D2661, DECEMBER 1982—REVISED DECEMBER 1983

- Included among the Package Options Are 20-Pin DIPs and Small Outline (SO) and Plastic and Ceramic Chip Carriers
- 'AS230 Has True and Complementary Outputs
- 'AS231 Has Complementary G and $\overline{G}$ Inputs
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- High Capacitive Drive Capability
- Current Sinking Capability Up to 64 mA
- Dependable Texas Instruments Quality and Reliability

SN54AS230 . . . J PACKAGE
SN74AS230 . . . N PACKAGE
SN74AS230 . . . DW PACKAGE
(TOP VIEW)



SN54AS231 . . . J PACKAGE
SN74AS231 . . . N PACKAGE
SN74AS231 . . . DW PACKAGE
(TOP VIEW)



2

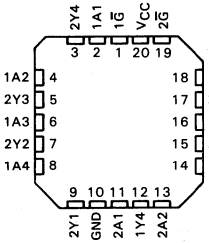
description

These octal buffers and line drivers are designed specifically to improve the performance of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs.

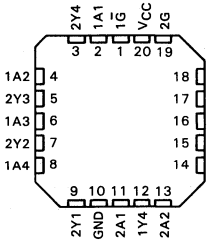
The SN74AS230 and SN74AS231 can be used to drive terminated lines down to 133 ohms.

The SN54AS230 and SN54AS231 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS230 and SN74AS231 are characterized for operation from 0°C to 70°C.

SN54AS230 . . . FH OR FK PACKAGE
SN74AS230 . . . FN PACKAGE
(TOP VIEW)

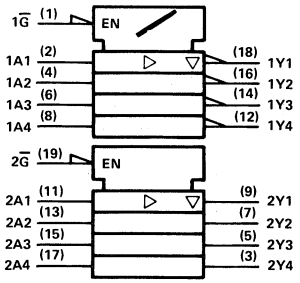


SN54AS231 . . . FH OR FK PACKAGE
SN74AS231 . . . FN PACKAGE
(TOP VIEW)

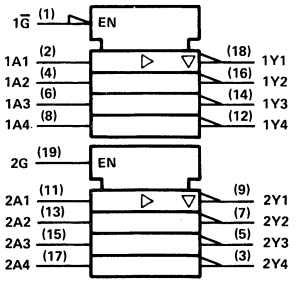


logic symbols

'AS230



'AS231



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS230, SN54AS231 . . . . . −55°C to 125°C
SN74AS230, SN74AS231 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS230 SN54AS231			SN74AS230 SN74AS231			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS230 SN54AS231			SN74AS230 SN74AS231			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.27	0.55				V
		V_{CC} = 4.5 V	I_{OL} = 64 mA					0.31	0.55	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	'AS230 2A	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	All others					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−150	−50		−150	mA
I_{CC}	'AS230	V_{CC} = 5.5 V	Outputs high		16	25		16	25	mA
			Outputs low		55	87		55	87	mA
			Outputs disabled		29	46		29	46	mA
	'AS231	V_{CC} = 5.5 V	Outputs high		12	18		12	18	mA
			Outputs low		52	82		52	82	
			Outputs disabled		25	39		25	39	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS230 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS230		SN74AS230		
			MIN	MAX	MIN	MAX	
t_{PLH}	1A	1Y	2.5	7	2.5	6.5	ns
t_{PHL}			2	6	2	5.7	
t_{PLH}	2A	2Y	2.5	9	2.5	6.2	ns
t_{PHL}			2	7	2	6.2	
t_{PZH}	$1\overline{G}$	1Y	2	7	2	6.4	ns
t_{PZL}			2	9	2	8.5	
t_{PHZ}			2	5.5	2	5	
t_{PLZ}			2	12.5	2	9.5	
t_{PZH}	$2\overline{G}$	2Y	2	10	2	9	ns
t_{PZL}			2	8	2	7.5	
t_{PHZ}			2	6.5	2	6	
t_{PLZ}			2	10.5	2	9	

'AS231 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS231		SN74AS231		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	2	7	2	6.5	ns
t_{PHL}			2	6	2	5.7	
t_{PZH}	$\overline{G}$	Y	2	7	2	6.4	ns
t_{PZL}			2	9	2	8.5	
t_{PHZ}			2	5.5	2	5	
t_{PLZ}			2	12.5	2	9.5	
t_{PZH}	G	Y	3	7	3	6	ns
t_{PZL}			3	10	3	9	
t_{PHZ}			3	6.5	3	6	
t_{PLZ}			3	13.5	3	7	

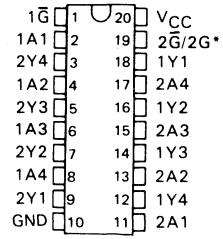
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

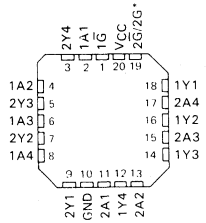
D2661, DECEMBER 1982 – REVISED DECEMBER 1984

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **P-N-P Inputs Reduce DC Loading**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . N PACKAGE
SN74ALS', SN74AS' . . . DW PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FH OR FK PACKAGE
SN74ALS', SN74AS' . . . FN PACKAGE
(TOP VIEW)



description

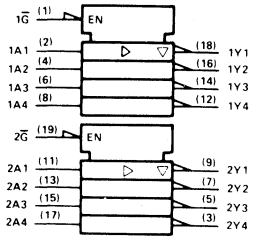
These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out and improved fan-in.

The -1 versions of the SN74ALS' parts are identical to their standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS' parts.

The SN54' family is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

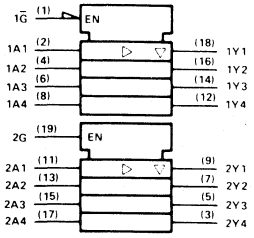
logic symbols

'ALS240A, 'AS240



Pin numbers shown are for J and N packages.

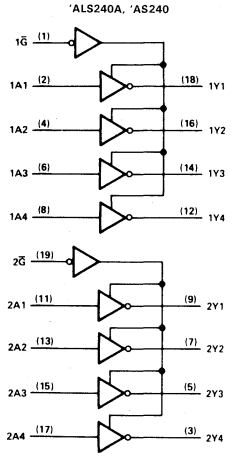
'ALS241A, 'AS241



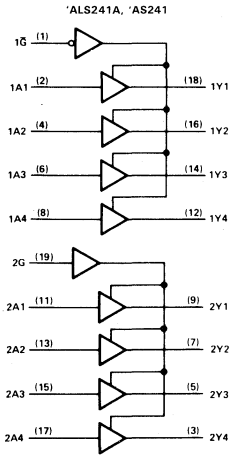
*2G̅ for 'ALS240A, 'AS240 or 2G for 'ALS241A, 'AS241

logic diagrams (positive logic)

'ALS240A, 'AS240



'ALS241A, 'AS241



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS240A, SN54ALS241A . . . . . −55°C to 125°C
SN74ALS240A, SN74ALS241A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS240A SN54ALS241A			SN74ALS240A SN74ALS241A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48 mA limit applies for the SN74ALS240-1 and SN74ALS241-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS240A SN54ALS241A			SN74ALS240A SN74ALS241A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS240A	V_{CC} = 5.5 V	Outputs high		4	11		4	11	mA
			Outputs low		13	23		13	23	
			Outputs disabled		14	25		14	25	
	'ALS241A		Outputs high		9	17		9	15	
			Outputs low		15	28		15	26	
			Outputs disabled		17	32		17	30	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS240A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54/74ALS240A			SN54ALS240A		SN74ALS240A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y		6	7.5	2	12	2	9	ns
t_{PHL}				5	7	2	11	2	9	
t_{PZH}	$\overline{G}$	Y		9	12	5	15	5	13	ns
t_{PZL}				10	13.5	5	20	5	18	
t_{PHZ}	$\overline{G}$	Y		6	8	2	12	2	10	ns
t_{PLZ}				7	9	3	18	3	12	

'ALS241A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS241A		SN74ALS241A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	14	3	11	ns
t_{PHL}			3	13	3	10	
t_{PZH}	$1\overline{G}$	Y	7	25	7	21	ns
t_{PZL}			7	25	7	21	
t_{PHZ}	$1\overline{G}$	Y	2	12	2	10	ns
t_{PLZ}			3	20	3	15	
t_{PZH}	2G	Y	7	25	7	21	ns
t_{PZL}			7	25	7	21	
t_{PHZ}	2G	Y	2	12	2	10	ns
t_{PLZ}			3	20	3	15	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS240, SN54AS241 . . . . . −55°C to 125°C
SN74AS240, SN74AS241 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS240 SN54AS241			SN74AS240 SN74AS241			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS240 SN54AS241			SN74AS240 SN74AS241			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.27	0.55				V
		V_{CC} = 4.75 V,	I_{OL} = 64 mA					0.31	0.55	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	'AS241A inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	All others					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−150	−50		−150	mA
I_{CC}	'AS240	V_{CC} = 5.5 V	Outputs high		11	17		11	17	mA
			Outputs low		51	75		51	75	
			Outputs disabled		24	38		24	38	
	'AS241		Outputs high		22	35		22	35	
			Outputs low		61	90		61	90	
			Outputs disabled		35	56		35	56	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS240 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS240		SN74AS240		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	2	7	2	6.5	ns
t_{PHL}			2	6	2	5.7	
t_{PZH}	$\overline{G}$	Y	2	7	2	6.4	ns
t_{PZL}			2	9.5	2	9	
t_{PHZ}	$\overline{G}$	Y	2	5.5	2	5	ns
t_{PLZ}			2	12.5	2	9.5	

'AS241 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS241		SN74AS241		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	2	9	2	6.2	ns
t_{PHL}			2	7	2	6.2	
t_{PZH}	$1\overline{G}$	Y	2	10	2	9	ns
t_{PZL}			2	8	2	7.5	
t_{PHZ}	$1\overline{G}$	Y	2	6.5	2	6	ns
t_{PLZ}			2	10.5	2	9	
t_{PZH}	2G	Y	3	11	3	10.5	ns
t_{PZL}			3	9.5	3	8.5	
t_{PHZ}	2G	Y	3	7	3	7	ns
t_{PLZ}			3	12	3	12	

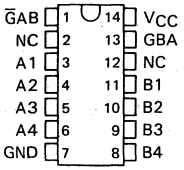
NOTE 1: For load circuit and voltage waveforms, see page 1-12

TYPES SN54ALS242A, SN54ALS243A, SN54AS242, SN54AS243
SN74ALS242A, SN74ALS243A, SN74AS242, SN74AS243
QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

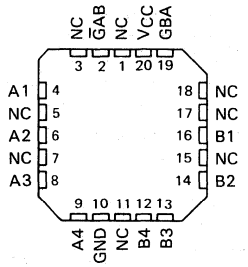
D2661, DECEMBER 1982—REVISED DECEMBER 1983

- **2-Way Asynchronous Communication Between Data Buses**
- **P-N-P Inputs Reduce Loading**
- **Dependable Texas Instruments Quality and Reliability**

SN54' . . . J PACKAGE
SN74' . . . N PACKAGE
SN74' . . . D PACKAGE
(TOP VIEW)



SN54' . . . FH OR FK PACKAGE
SN74' . . . FN PACKAGE
(TOP VIEW)



NC—No Internal connection

description

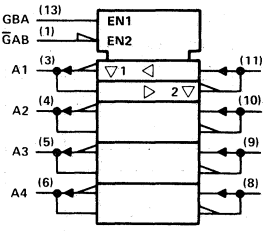
These four-data-line transceivers are designed for asynchronous two-way communications between data buses. The SN74ALS' devices can be used to drive terminated lines down to 133 ohms.

The -1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS' parts.

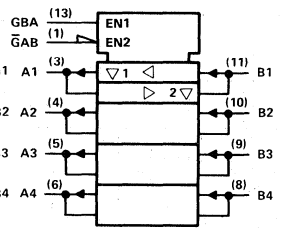
The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

logic symbol

'ALS242A, 'AS242

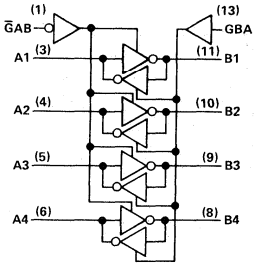


'ALS243A, 'AS243

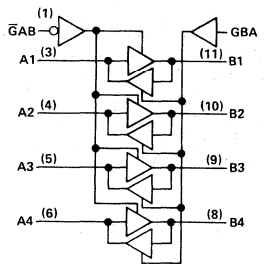


logic diagrams (positive logic)

'ALS242A, 'AS242



'ALS243A, 'AS243



Pin numbers shown are for J and N packages.

FUNCTION TABLE

INPUTS		'ALS242A	'ALS243A
$\overline{G}AB$	GBA	'AS242	'AS243
L	L	$\overline{A}$ to B	A to B
H	H	$\overline{B}$ to A	B to A
H	L	Isolation	Isolation
L	H	Latch A and B ($A=\overline{B}$)	Latch A and B ($A=B$)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS242A, SN54ALS243A . . . . . −55°C to 125°C
SN74ALS242A, SN74ALS243A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS242A SN54ALS243A			SN74ALS242A SN74ALS243A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS242A-1 and SN74ALS243A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS242A SN54ALS243A			SN74ALS242A SN74ALS243A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports§					−0.1			−0.1	
I_O¶		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS242A	V_{CC} = 5.5 V	Outputs high		10	20		10	16	mA
			Outputs low		14	26		14	21	
			Outputs disabled		15	27		15	22	
	'ALS243A		Outputs high		15	30		15	25	
			Outputs low		20	35		20	30	
			Outputs disabled		21	37		21	32	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS242A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_1 = 500 Ω, R_2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS242A		SN74AS242A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	3	15	3	11	ns
t_{PHL}			2	14	2	10	
t_{PZH}	$\overline{G}$AB	B	4	22	4	18	ns
t_{PZL}			7	25	7	21	
t_{PHZ}	$\overline{G}$AB	B	2	16	2	14	ns
t_{PLZ}			4	28	4	22	
t_{PZH}	GBA	A	4	22	4	18	ns
t_{PZL}			7	25	7	21	
t_{PHZ}	GBA	A	2	16	2	14	ns
t_{PLZ}			4	28	4	22	

'ALS243 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_1 = 500 Ω, R_2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS243A		SN74ALS243A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	4	15	4	11	ns
t_{PHL}			4	15	4	11	
t_{PZH}	$\overline{G}$AB	B	7	25	7	20	ns
t_{PZL}			7	25	7	20	
t_{PHZ}	$\overline{G}$AB	B	2	16	2	14	ns
t_{PLZ}			3	27	3	22	
t_{PZH}	GBA	A	7	25	7	20	ns
t_{PZL}			7	25	7	20	
t_{PHZ}	GBA	A	2	16	2	14	ns
t_{PLZ}			3	27	3	22	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54AS242, SN54AS243 . . . . . −55°C to 125°C
SN74AS242, SN74AS243 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS242 SN54AS243			SN74AS242 SN74AS243			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS242 SN54AS243			SN74AS242 SN74AS243			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA			0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA						0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					50			50	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	'AS242 A or B ports‡					−0.5			−0.5	
	'AS243 A or B ports‡					−1			−1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−150	−50		−150	mA
I_{CC}	'AS242	V_{CC} = 5.5 V	Outputs high		18	28		18	28	mA
			Outputs low		38	60		38	60	
			Outputs disabled		25	39		25	39	
	'AS243		Outputs high		28	44		28	44	
			Outputs low		47	74		47	74	
			Outputs disabled		35	56		35	56	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS242 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS242		SN74AS242		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	7	2	6.5	ns
t_{PHL}			2	6	2	5.7	
t_{PZH}	$\overline{G}$AB	B	2	9	2	5.5	ns
t_{PZL}			2	8.5	2	7.5	
t_{PHZ}	$\overline{G}$AB	B	2	7	2	6.5	ns
t_{PLZ}			2	12.5	2	9.5	
t_{PZH}	GAB	A	3	7	3	6	ns
t_{PZL}			3	9	3	8	
t_{PHZ}	GAB	A	3	8.5	3	6	ns
t_{PLZ}			3	13.5	3	10.5	

'AS243 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS243		SN74AS243		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	3	9	3	7.5	ns
t_{PHL}			3	8	3	6.5	
t_{PZH}	$\overline{G}$AB	B	2	10	2	9	ns
t_{PZL}			2	9	2	7.5	
t_{PHZ}	$\overline{G}$AB	B	2	7	2	6.5	ns
t_{PLZ}			2	11	2	9	
t_{PZH}	GAB	A	3	11	3	10.5	ns
t_{PZL}			3	9.5	3	8.5	
t_{PHZ}	GAB	A	3	7.5	3	7	ns
t_{PLZ}			3	14	3	11	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TYPES SN54ALS244A, SN54AS244, SN74ALS244A, SN74AS244
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982—REVISED DECEMBER 1983

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce DC Loading
- Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

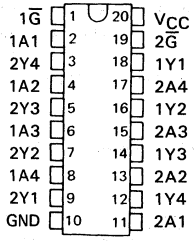
description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'ALS240A, 'ALS241A, 'AS240, and 'AS241, these devices provide the choice of selected combinations of inverting outputs, symmetrical G (active-low input control) inputs, and complementary G and G inputs.

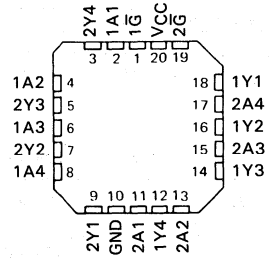
The —1 version of the SN74ALS244A is identical to the standard version except that the recommended maximum I_{OL} is increased to 48 milliamperes. There is no —1 version of the SN54ALS244A.

The SN54ALS244A and SN54AS244 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS244A and SN74AS244 are characterized for operation from 0°C to 70°C.

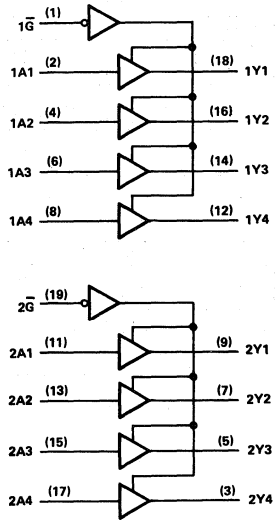
SN54ALS244A, SN54AS244 . . . J PACKAGE
SN74ALS244A, SN74AS244 . . . N PACKAGE
SN74ALS244A, SN74AS244 . . . DW PACKAGE
(TOP VIEW)



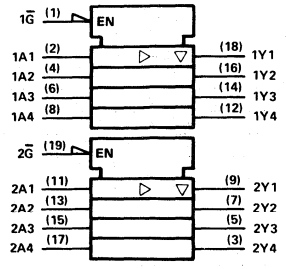
SN54ALS244A, SN54AS244 . . . FH OR FK PACKAGE
SN74ALS244A, SN74AS244 . . . FN PACKAGE
(TOP VIEW)



logic diagram (positive logic)



logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS244A . . . . . −55°C to 125°C
SN74ALS244A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS244A			SN74ALS244A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS244A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS244A			SN74ALS244A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V (I_{OL} = 48 mA for −1 version)	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V		−0.1			−0.1		mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		9	15		9	15	mA
		Outputs low		15	24		15	24	
		Outputs disabled		17	27		17	27	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS244A		SN74ALS244A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	13	3	10	ns
t_{PHL}			3	13	3	10	
t_{PZH}	$\overline{G}$	Y	7	25	7	20	ns
t_{PZL}			7	25	7	20	
t_{PHZ}	$\overline{G}$	Y	2	12	2	10	ns
t_{PLZ}			3	18	3	13	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS244 . . . . . −55 °C to 125 °C
SN74AS244 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS244			SN74AS244			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS244			SN74AS244			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA			0.55				V
		V_{CC} = 4.5 V	I_{OL} = 64 mA						0.55	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	$\overline{G}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A					−1			−1	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−150	−50		−150	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		22	34		22	34	mA
			Outputs low		60	90		60	90	
			Outputs disabled		34	54		34	54	

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS245A			SN74ALS245A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports‡					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		30	48		30	45	mA
			Outputs low		36	60		36	55	
			Outputs disabled		38	63		38	58	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

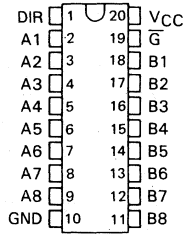
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS245A		SN74ALS245A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	3	15	3	10	ns
t_{PHL}			3	13	3	10	
t_{PZH}	$\overline{G}$	A or B	5	25	5	20	ns
t_{PZL}			5	25	5	20	
t_{PHZ}	$\overline{G}$	A or B	2	12	2	10	ns
t_{PLZ}			4	18	4	15	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

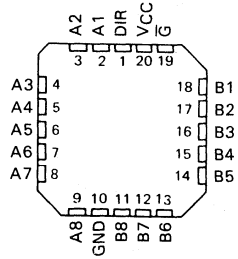
D2661, DECEMBER 1982 – REVISED AUGUST 1984

- **3-State Outputs Drive Bus Lines Directly**
- **P-N-P- Inputs Reduce DC Loading**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS245A, SN54AS245 . . . J PACKAGE
SN74ALS245A, SN74AS245 . . . N PACKAGE
SN74ALS245A, SN74AS245 . . . DW PACKAGE
(TOP VIEW)



SN54ALS245A, SN54AS245 . . . FH OR FK PACKAGE
SN74ALS245A, SN74AS245 . . . FN PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between data buses The control function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

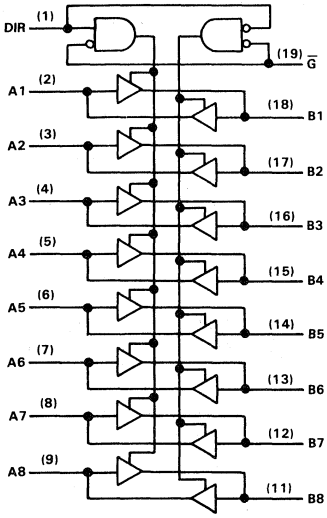
The – 1 version of the SN74ALS245A is identical to the standard version except that the recommended maximum I_{OL} is increased to 48 milliamperes. There is no – 1 version of the SN54ALS245A.

The SN54ALS245A and SN54AS245 are characterized for operation over the full military temperature range of – 55 °C to 125 °C. The SN74ALS245A and SN74AS245 are characterized for operation from 0 °C to 70 °C.

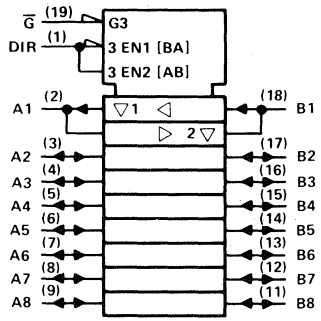
FUNCTION TABLE

ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic diagram (positive logic)



logic symbol†



Pin numbers shown are for J and N packages.

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS245A . . . . . −55°C to 125°C
SN74ALS245A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS245A			SN74ALS245A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48‡	
T_A	Operating free-air temperature	−55		125	0		70	°C

‡The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS245A-1 only.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS244		SN74AS244		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	2	9	2	6.2	ns
t_{PHL}			2	7	2	6.2	
t_{PZH}	$\overline{G}$	Y	2	10	2	9	ns
t_{PZL}			2	8	2	7.5	
t_{PHZ}	$\overline{G}$	Y	2	6.5	2	6	ns
t_{PLZ}			2	10.5	2	9	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54AS245 . . . . . −55°C to 125°C
SN74AS245 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS245			SN74AS245			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS245			SN74AS245			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.3	0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA					0.35	0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.4 V			50			20	μA
	A or B ports‡					70			70	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A or B ports‡					−0.75			−0.75	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−150	−50		−150	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		62	97		62	97	mA
			Outputs low		95	143		95	143	
			Outputs disabled		79	123		79	123	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports (Q_A through Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS245		SN74AS245		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	9.5	2	7.5	ns
t_{PHL}			2	9	2	7	
t_{PZH}	$\overline{G}$	A or B	2	11	2	9	ns
t_{PZL}			2	10.5	2	8.5	
t_{PHZ}	$\overline{G}$	A or B	2	7.5	2	5.5	ns
t_{PLZ}			2	12	2	9.5	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

- **4-Line to 1-Line Multiplexer that can Select 1 of 16 Data Inputs**
- **Applications:**
  Boolean Function Generator
  Parallel-to-Serial Converter
  Data Source Selector
- **Buffered 3-State Bus Driver Inputs Permit Multiplexing from N Lines to One Line**
- **Dependable Texas Instruments Quality and Reliability**

description

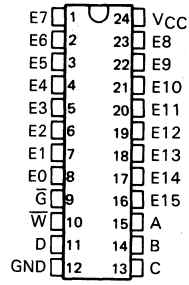
The 'AS250 provides full binary decoding to select one of sixteen data sources with an inverting $\overline{W}$ output. The selected sources are buffered with symmetrical propagation delay times. This reduces the possibility of transients occurring at the output.

A buffered enable output ($\overline{G}$) may be used for n-line-to-one-line cascading. Taking the $\overline{G}$ high will place the output in a high-impedance state. In the high-impedance state, the output neither loads nor drives the bus lines significantly.

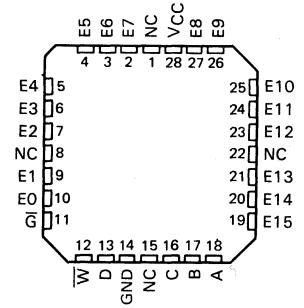
The enable ($\overline{G}$) does not affect the internal operations of the data selector/multiplexer. New data can be set up while the outputs are disabled.

The SN54AS250 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS250 is characterized for operation from 0°C to 70°C.

SN54AS250 . . . JT PACKAGE
SN74AS250 . . . NT PACKAGE
SN74AS250 . . . DW PACKAGE
(TOP VIEW)

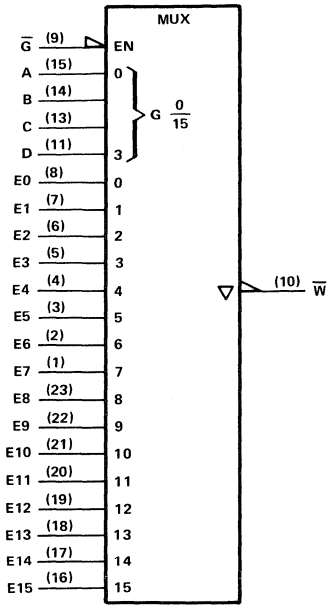


SN54AS250 . . . FH OR FK CHIP CARRIER PACKAGE
SN74AS250 . . . FN CHIP CARRIER PACKAGE
(TOP VIEW)



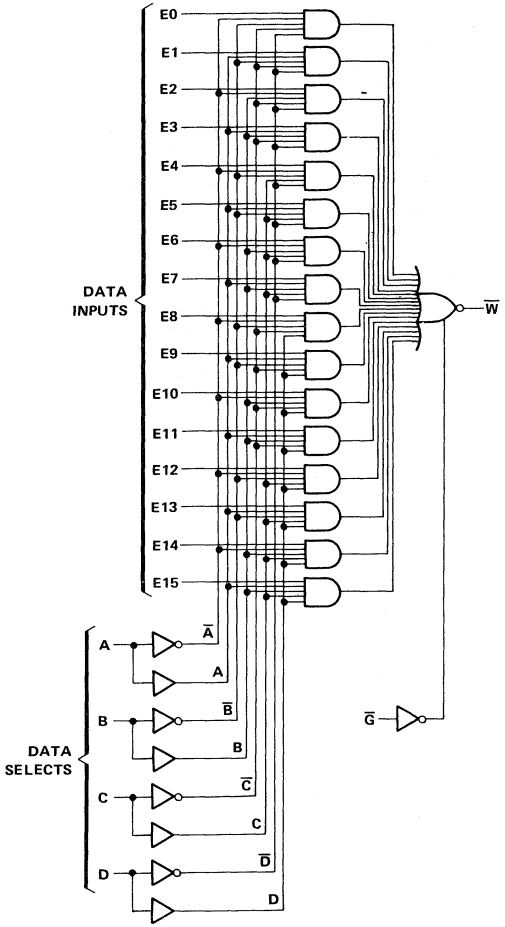
NC – No internal connection

logic symbol



Pin numbers shown are for J or N packages.

logic diagram (positive logic)



FUNCTION TABLE

INPUT						OUTPUT
$\overline{G}$	A	B	C	D	Ei	$\overline{W}$
L	L	L	L	L	E0	E0
L	H	L	L	L	E1	E1
L	L	H	L	L	E2	E2
L	H	H	L	L	E3	E3
L	L	L	H	L	E4	E4
L	H	L	H	L	E5	E5
L	L	H	H	L	E6	E6
L	H	H	H	L	E7	E7
L	L	L	L	H	E8	E8
L	H	L	L	H	E9	E9
L	L	H	L	H	E10	E10
L	H	H	L	H	E11	E11
L	L	L	H	H	E12	E12
L	H	L	H	H	E13	E13
L	L	H	H	H	E14	E14
L	H	H	H	H	E15	E15
H	X	X	X	X	X	Z

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS250 . . . . . −55°C to 125°C
SN74AS250 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS250			SN74AS250			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			32			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS250			SN74AS250			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC} −2			V_{CC} −2			V
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		26			26	42	mA
		Outputs low		31			31	50	
		Outputs disabled		30			30	48	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX					UNIT
			SN54AS250			SN74AS250		
			MIN	TYP†	MAX	MIN	MAX	
t_{PLH}	DATA	$\overline{W}$		5		3	8	ns
t_{PHL}				3.5		2	6	
t_{PLH}	SELECT	$\overline{W}$		7.5		4	13	ns
t_{PHL}				7.5		4	10	
t_{PZH}	$\overline{G}$	$\overline{W}$		4.5		2	7	ns
t_{PZL}				12		4	20	
t_{PHZ}	$\overline{G}$	$\overline{W}$		3.5		2	6	ns
t_{PLZ}				4.5		2	6	

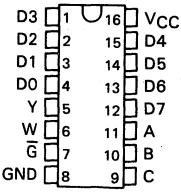
†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12

TYPES SN54ALS251, SN54AS251, SN74ALS251, SN74AS251
1 OF 8 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

D2661, APRIL 1982—REVISED DECEMBER 1983

- **Three-State Versions of 'ALS151 and 'AS151**
- **Three-State Outputs Interface Directly with System Bus**
- **Performs Parallel-to-Serial Conversion**
- **Complementary Outputs Provide True and Inverted Data**
- **Fully Compatible with Most TTL Circuits**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS251, SN54AS251 . . . J PACKAGE
SN74ALS251, SN74AS251 . . . N PACKAGE
SN74ALS251, SN74AS251 . . . D PACKAGE
(TOP VIEW)



2

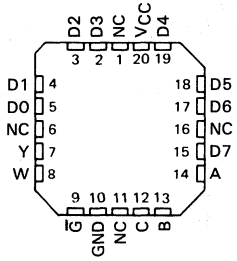
description

These data selectors/multiplexers contain full binary decoding to select one-of-eight data sources and feature strobe-controlled complementary three-state outputs.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state), the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Both outputs are controlled by the strobe ($\overline{G}$). The outputs are disabled when $\overline{G}$ is high.

The SN54ALS251 and SN54AS251 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS251 and SN74AS251 are characterized for operation from 0 °C to 70 °C.

SN54ALS251, SN54AS251 . . . FH OR FK PACKAGE
SN74ALS251, SN74AS251 . . . FN PACKAGE
(TOP VIEW)



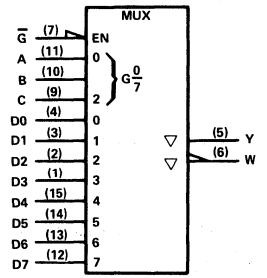
NC — No internal connection.

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	$\overline{G}$	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

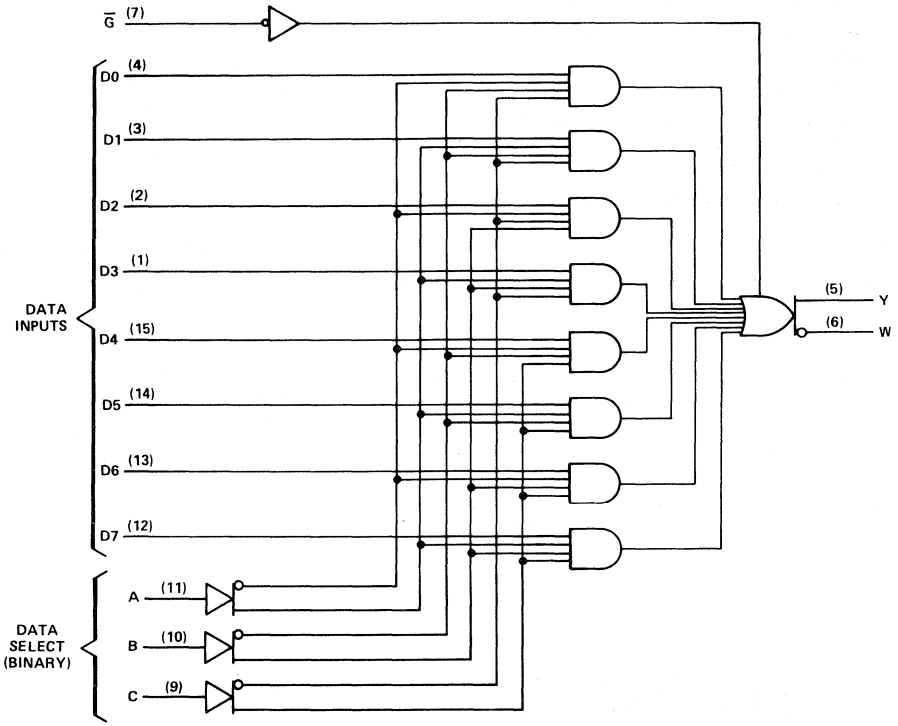
D0, D1 . . . D7 = the level of the respective D input

logic symbol



Pin numbers shown are for J and N packages.

logic diagram (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS251, SN54AS251 . . . . . −55 °C to 125 °C
SN74ALS251, SN74AS251 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS251			SN74ALS251			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS251			SN74ALS251			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	Enabled	V_{CC} = 5.5 V,	Inputs at Gnd.		7	10		7	10	mA
	Disabled	V_{CC} = 5.5 V,	Inputs at 4.5 V		9.4	14		9.4	14	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS251		SN74ALS251		
			MIN	MAX	MIN	MAX	
t_{PLH}	A, B or C	Y	5	21	5	18	ns
t_{PHL}			8	28	8	24	
t_{PLH}	A, B or C	W	8	28	8	24	ns
t_{PHL}			7	26	7	23	
t_{PLH}	Any D	Y	2	12	2	10	ns
t_{PHL}			3	18	3	15	
t_{PLH}	Any D	W	3	18	3	15	ns
t_{PHL}			3	18	3	15	
t_{PZH}	$\overline{G}$	Y	3	18	3	15	ns
t_{PZL}			3	18	3	15	
t_{PZH}	$\overline{G}$	W	3	18	3	15	ns
t_{PZL}			3	18	3	15	
t_{PHZ}	$\overline{G}$	Y	2	12	2	10	ns
t_{PLZ}			1	12	1	10	
t_{PHZ}	$\overline{G}$	W	2	12	2	10	ns
t_{PLZ}			1	12	1	10	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

recommended operating conditions

		SN54AS251			SN74AS251			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			32			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS251			SN74AS251			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−50			−50	μA
I_I	A, B, C	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	All other					0.1			0.1	
I_{IH}	A, B, C	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All other					20			20	
I_{IL}	A, B, C	V_{CC} = 5.5 V,	V_I = 0.4 V		−0.6			−0.6		mA
	All other				−0.3			−0.3		
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,			28			28		mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS251			SN74AS251			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A, B,or C	Y		5			5		ns
t_{PHL}				5			5		
t_{PLH}	A, B, or C	W		4.5			4.5		ns
t_{PHL}				4.5			4.5		
t_{PLH}	Any D	Y		3			3		ns
t_{PHL}				4			4		
t_{PLH}	Any D	W		3			3		ns
t_{PHL}				2.5			2.5		
t_{PZH}	$\overline{G}$	Y		5			5		ns
t_{PZL}				6			6		
t_{PZH}	$\overline{G}$	W		5			5		ns
t_{PZL}				6			6		
t_{PHZ}	$\overline{G}$	Y		3			3		ns
t_{PLZ}				4			4		
t_{PHZ}	$\overline{G}$	W		3			3		ns
t_{PLZ}				4			4		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

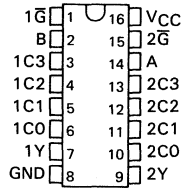
Additional information on these products can be obtained from the factory as it becomes available.

TYPES SN54ALS253, SN54AS253, SN74ALS253, SN74AS253
DUAL 1 OF 4 DATA SELECTORS/MULTIPLEXERS
WITH 3-STATE OUTPUTS

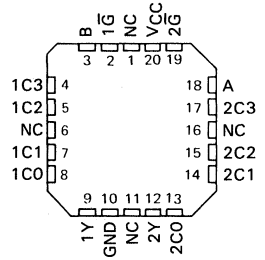
D2661, APRIL 1982—REVISED DECEMBER 1983

- **Three-State Versions of 'ALS153 and 'AS153**
- **Permits Multiplexing from N Lines to 1 Line**
- **Performs Parallel-to-Serial Conversion**
- **Fully Compatible with Most TTL Circuits**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS253, SN54AS253 . . . J PACKAGE
SN74ALS253, SN74AS253 . . . N PACKAGE
SN74ALS253, SN74AS253 . . . D PACKAGE
(TOP VIEW)



SN54ALS253, SN54AS253 . . . FH OR FK PACKAGE
SN74ALS253, SN74AS253 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe ($\overline{G}$). The output is disabled when its strobe is high.

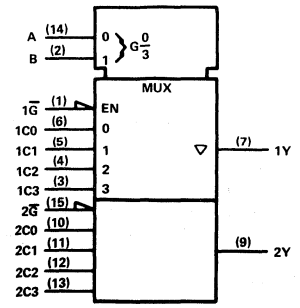
The SN54ALS253 and SN54AS253 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS253 and SN74AS253 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

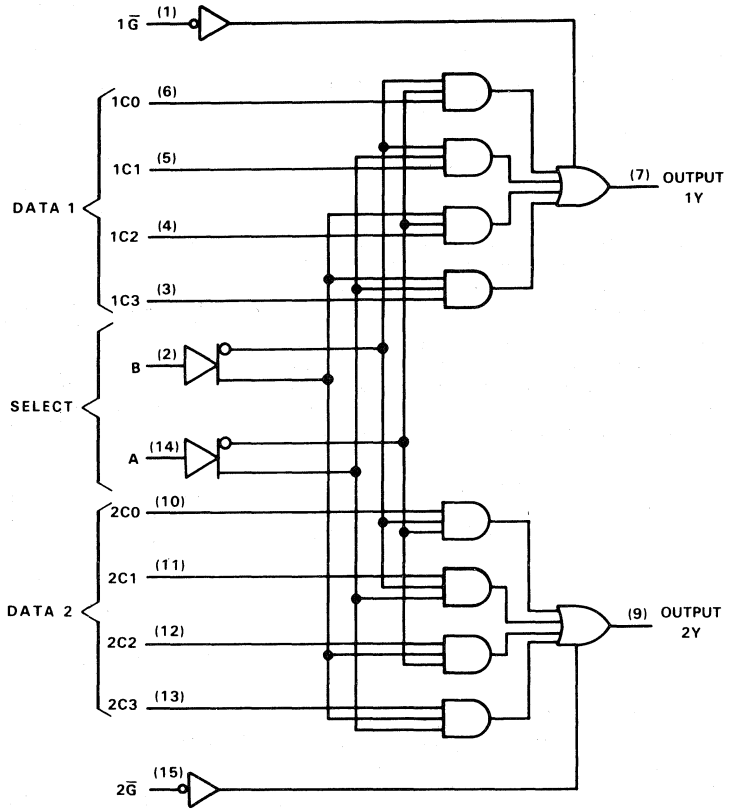
Address inputs A and B are common to both sections.

logic symbol



Pin numbers shown are for J and N packages.

logic diagram (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS253, SN54AS253 . . . . . −55 °C to 125 °C
SN74ALS253, SN74AS253 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS253			SN74ALS253			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS253			SN74ALS253			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs enabled		6.5	12		6.5	12	mA
		Outputs disabled		7.5	14		7.5	14	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS253		SN74ALS253		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Any Y	5	25	5	21	ns
t_{PHL}			5	25	5	21	
t_{PLH}	Data (Any C)	Any Y	2	12	2	10	ns
t_{PHL}			3	17	3	14	
t_{PZH}	$\overline{G}$	Any Y	3	17	3	14	ns
t_{PZL}			4	19	4	16	
t_{PHZ}	$\overline{G}$	Any Y	2	12	2	10	ns
t_{PLZ}			2	16	2	14	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

recommended operating conditions

		SN54AS253			SN74AS253			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			32			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS253			SN74AS253			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I	A, B	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	A, B	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All others					20			20	
I_{IL}	A, B	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	All others					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		18	29		18	29	mA
			Outputs low		20	32		20	32	
			Outputs disabled		21	33		21	33	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

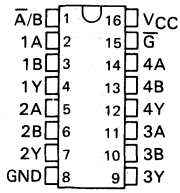
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS253		SN74AS253		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	4	14.5	4	13.5	ns
t_{PHL}			4	12	4	11.5	
t_{PLH}	Data (Any C)	Y	3	8.5	3	7.5	ns
t_{PHL}			3	8.5	3	8	
t_{PZH}	G	Any Y	4	13	4	12.5	ns
t_{PZL}			4	12	4	11.5	
t_{PHZ}	G	Any Y	2	6.5	2	6	ns
t_{PLZ}			2	8	2	7	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

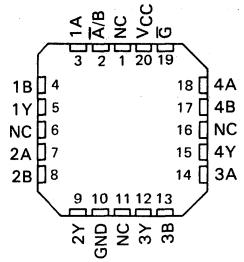
D2661, APRIL 1982—REVISED DECEMBER 1983

- **Three-State Outputs Interface Directly with System Bus**
- **Provides Bus Interface from Multiple Sources in High-Performance Systems**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . N PACKAGE
SN74ALS', SN74AS' . . . D PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FH OR FK PACKAGE
SN74ALS', SN74AS' . . . FN PACKAGE
(TOP VIEW)

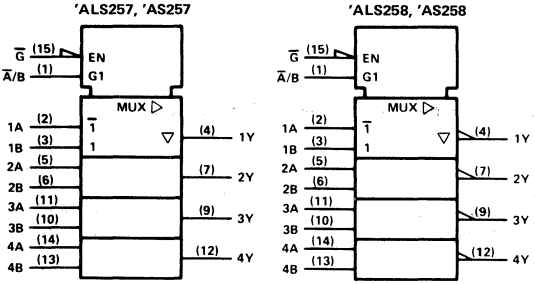


description

These devices are designed to multiplex signals from four-bit data sources to four-output data lines in bus-organized systems. The 3-state outputs will not load the data lines when the output control pin ($\overline{G}$) is at a high-logic level.

The SN54' family is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74' family is characterized for operation from 0 °C to 70 °C.

logic symbols



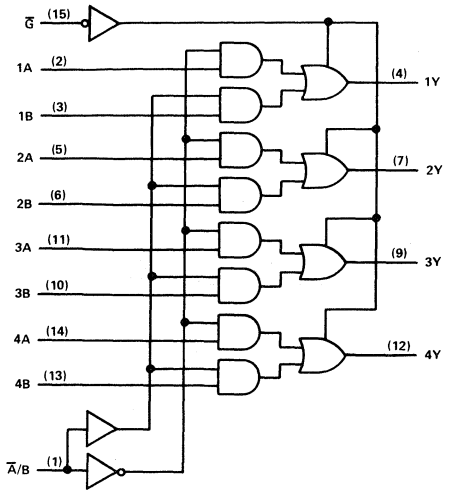
Pin numbers shown are for J and N packages.

FUNCTION TABLE

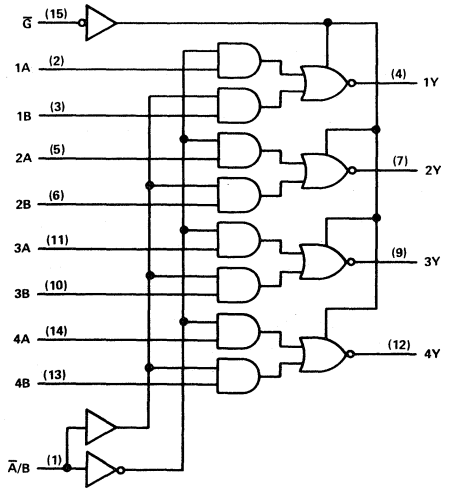
INPUTS				OUTPUT Y	
OUTPUT CONTROL $\overline{G}$	SELECT $\overline{A}/B$	DATA A	DATA B	'ALS257 'AS257	'ALS258 'AS258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

logic diagrams (positive logic)

'ALS257, 'AS257



'ALS258, 'AS258



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS', SN54AS' . . . . . −55°C to 125°C
SN74ALS', SN74AS' . . . . . 0°C to 70°
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS257 SN54ALS258			SN74ALS257 SN74ALS258			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS257 SN54ALS258			SN74ALS257 SN74ALS258			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS257	V_{CC} = 5.5 V	Outputs high		3	6		3	6	mA
			Outputs low		8	12		8	12	
			Outputs disabled		9	14		9	14	
	'ALS258	V_{CC} = 5.5 V	Outputs high		2.5	4		2.5	4	
			Outputs low		7	11		7	11	
			Outputs disabled		8	13		8	13	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS257 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS257		SN74ALS257		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Any Y	2	12	2	10	ns
t_{PHL}			3	14	3	12	
t_{PLH}	$\overline{A}$/B	Any Y	7	21	7	18	ns
t_{PHL}			6	25	6	22	
t_{PZH}	$\overline{G}$	Any Y	4	20	4	16	ns
t_{PZL}			5	22	5	18	
t_{PHZ}	$\overline{G}$	Any Y	2	12	2	10	ns
t_{PLZ}			4	18	4	15	

'ALS258 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS258		SN74ALS258		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Any Y	2	10	2	8	ns
t_{PHL}			2	9	2	7	
t_{PLH}	$\overline{A}$/B	Any Y	5	28	5	25	ns
t_{PHL}			8	23	8	20	
t_{PZH}	$\overline{G}$	Any Y	5	20	5	18	ns
t_{PZL}			5	20	5	18	
t_{PHZ}	$\overline{G}$	Any Y	2	12	2	10	ns
t_{PLZ}			5	20	5	18	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

recommended operating conditions

		SN54AS257 SN54AS258			SN74AS257 SN74AS258			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			32			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS257 SN54AS258			SN74AS257 SN74AS258			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I	A, B or $\overline{G}$	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	$\overline{A}$/B					0.2			0.2	
I_{IH}	A, B, or $\overline{G}$	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	$\overline{A}$/B					40			40	
I_{IL}	A, B, or $\overline{G}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	$\overline{A}$/B					−1			−1	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS257	V_{CC} = 5.5 V	Outputs high		12.1	19.7		12.1	19.7	mA
			Outputs low		19	30.6		19	30.6	
			Outputs disabled		19.7	31.9		19.7	31.9	
	'AS258	V_{CC} = 5.5 V	Outputs high		8.4	13.5		8.4	13.5	
			Outputs low		15.2	24.6		15.2	24.6	
			Outputs disabled		15.5	25.2		15.5	25.2	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS257 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS257		SN74AS257		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Any Y	1	6.5	1	5.5	ns
t_{PHL}			1	7	1	6	
t_{PLH}	$\overline{A}$/B	Any Y	2	12	2	11	ns
t_{PHL}			2	10.5	2	10	
t_{PZH}	$\overline{G}$	Any Y	2	8.5	2	7.5	ns
t_{PZL}			2	10.5	2	9.5	
t_{PHZ}	$\overline{G}$	Any Y	1.5	8	1.5	6.5	ns
t_{PLZ}			2	8	2	7	

'AS258 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS258		SN74AS258		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Any Y	1	5.5	1	5	ns
t_{PHL}			1	5	1	4	
t_{PLH}	$\overline{A}$/B	Any Y	2	11	2	9.5	ns
t_{PHL}			2	11	2	10	
t_{PZH}	$\overline{G}$	Any Y	2	8.5	2	8	ns
t_{PZL}			2	11	2	10	
t_{PHZ}	$\overline{G}$	Any Y	1.5	7	1.5	6	ns
t_{PLZ}			2	8.5	2	6.5	

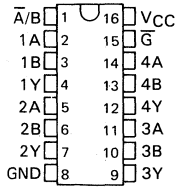
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

QUADRUPLE 1 OF 2 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

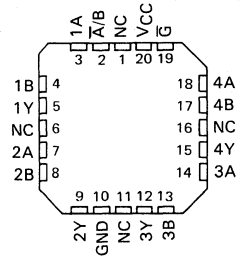
D2661, APRIL 1982 – REVISED JUNE 1984

- **Three-State Outputs Interface Directly with System Bus**
- **Provides Bus Interface from Multiple Sources in High-Performance Systems**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . N PACKAGE
SN74ALS', SN74AS' . . . D PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FH OR FK PACKAGE
SN74ALS', SN74AS' . . . FN PACKAGE
(TOP VIEW)

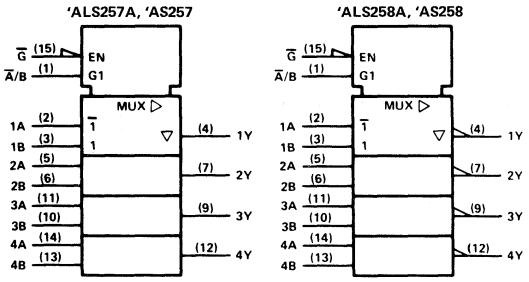


description

These devices are designed to multiplex signals from four-bit data sources to four-output data lines in bus-organized systems. The 3-state outputs will not load the data lines when the output control pin ($\overline{G}$) is at a high-logic level.

The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

logic symbols



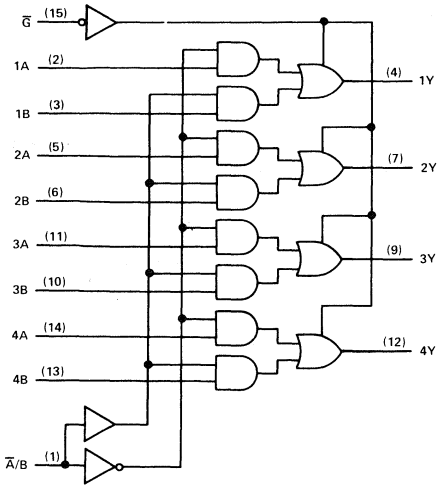
Pin numbers shown are for J and N packages.

FUNCTION TABLE

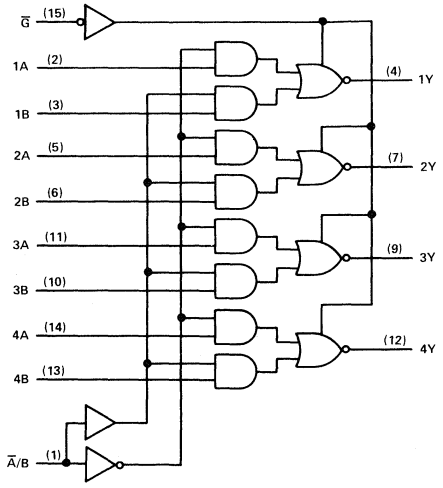
INPUTS				OUTPUT Y	
OUTPUT CONTROL $\overline{G}$	SELECT $\overline{A}$/B	DATA A	DATA B	'ALS257A 'AS257	'ALS258A 'AS258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

logic diagrams (positive logic)

'ALS257A, 'AS257



'ALS258A, 'AS258



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS', SN54AS' . . . . . −55°C to 125°C
SN74ALS', SN74AS' . . . . . 0°C to 70°
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS257A SN54ALS258A			SN74ALS257A SN74ALS258A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS257A SN54ALS258A			SN74ALS257A SN74ALS258A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS257A	V_{CC} = 5.5 V	Outputs high		3	6		3	6	mA
			Outputs low		8	13		8	13	
			Outputs disabled		9	14		9	14	
	'ALS258A	V_{CC} = 5.5 V	Outputs high		2.5	4		2.5	4	
			Outputs low		7	11		7	11	
			Outputs disabled		8	13		8	13	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS257A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS257A		SN74ALS257A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Any Y	2	13	2	11	ns
t_{PHL}			2	13	2	11	
t_{PLH}	$\overline{A}$/B	Any Y	5	21	5	18	ns
t_{PHL}			5	28	5	25	
t_{PZH}	$\overline{G}$	Any Y	3	19	3	16	ns
t_{PZL}			5	22	5	18	
t_{PHZ}	$\overline{G}$	Any Y	2	12	2	10	ns
t_{PLZ}			4	20	4	15	

'ALS258A switching characteristics (see Note 1)

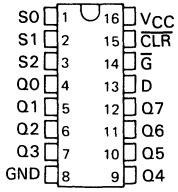
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS258A		SN74ALS258A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Any Y	2	10	2	8	ns
t_{PHL}			2	10	2	8	
t_{PLH}	$\overline{A}$/B	Any Y	3	25	3	22	ns
t_{PHL}			7	25	7	22	
t_{PZH}	$\overline{G}$	Any Y	5	19	5	16	ns
t_{PZL}			5	20	5	17	
t_{PHZ}	$\overline{G}$	Any Y	2	12	2	10	ns
t_{PLZ}			5	21	5	18	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

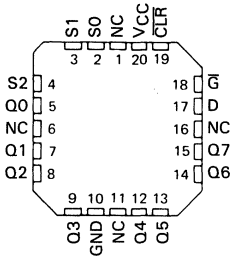
D2661, DECEMBER 1982

- 8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion with Storage
- Asynchronous Parallel Clear
- Active High Decoder
- Enable/Disable Input Simplifies Expansion
- Expandable for N-Bit Applications
- Four Distinct Functional Modes
- Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS259 . . . J PACKAGE
SN74ALS259 . . . N PACKAGE
SN74ALS259 . . . D PACKAGE
(TOP VIEW)



SN54ALS259 . . . FH OR FK PACKAGE
SN74ALS259 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

These 8-bit addressable latches are designed for general purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

Four distinct modes of operation are selectable by controlling the clear ($\overline{CLR}$) and enable ($\overline{G}$) inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch. The addressed latch will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, enable $\overline{G}$ should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

The SN54ALS259 will be characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS259 will be characterized for operation from 0°C to 70°C.

FUNCTION TABLE

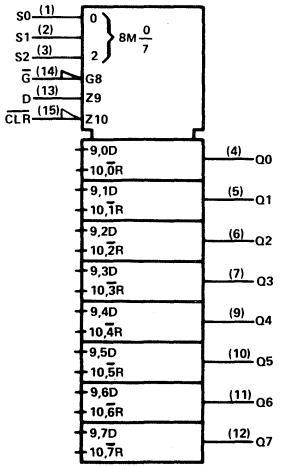
INPUTS $\overline{CLR}$	INPUTS $\overline{G}$	OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
H	L	D	Q_{iO}	Addressable Latch
H	H	Q_{iO}	Q_{iO}	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear

D = the level at the data input.
Q_{iO} = the level of Q_i (i = 0, 1, ...7, as appropriate) before the indicated steady-state input conditions were established.

LATCH SELECTION TABLE

SELECT INPUTS S2	S1	S0	LATCH ADDRESSED
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

logic symbol



Pin numbers shown are for J and N packages.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS

D2824, DECEMBER 1983

- **Performs Look-Ahead Carry Across n-Bit Counters**
- **Accommodates Active-High or Active-Low Carry**
- **Improves Cascaded Counters System Performance**
- **Dependable Texas Instruments Quality and Reliability**

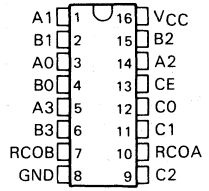
description

This look-ahead generator was designed specifically to perform a carry-anticipate across any number of n-bit counters,thus increasing system clock frequency. A carry enable CE, and carry outputs RCOA and RCOB are provided for n-bit cascading.

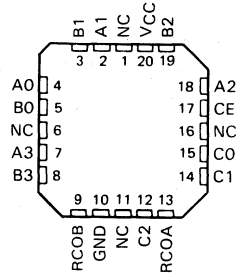
The counter can be used with either active-high-carry or active-low-carry counters. For active-high-carry counters, CE is active high, the A set of inputs and output RCOA are used, and the B set of inputs are connected to a low logic level. For active-low-carry counters, CE is active low, the B set of inputs and output RCOB are used, and the A set of inputs are connected to a high logic level. See Figures 1 and 2 for typical applications.

The SN54AS264 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS264 is characterized for operation in the temperature range of 0°C to 70°C.

SN54AS264 . . . J PACKAGE
SN74AS264 . . . N PACKAGE
SN74AS264 . . . D PACKAGE
(TOP VIEW)



SN54AS264 . . . FH OR FK PACKAGE
SN74AS264 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

positive logic equations

ACTIVE-HIGH-CARRY COUNTERS
(CE is high, all B inputs are low)

$C0 = A0$
$C1 = A0 \cdot A1$
$C2 = A0 \cdot A1 \cdot A2$
$RCOA = A0 \cdot A1 \cdot A2 \cdot A3$
RCOB is high

ACTIVE-LOW-CARRY COUNTERS
(CE is low, all A inputs are high)

$C0 = \overline{B0}$
$C1 = \overline{B0 \cdot B1}$
$C2 = \overline{B0 \cdot B1 \cdot B2}$
$RCOA = \overline{B1 \cdot B2 \cdot B3}$
$RCOB = \overline{B0 \cdot B1 \cdot B2 \cdot B3}$

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

FUNCTION TABLE FOR C0 OUTPUT

INPUTS			OUTPUT
A0	B0	CE	C0
H	H	X	H
H	X	H	H
L	X	X	L
X	L	L	L

FUNCTION TABLE FOR C1 OUTPUT

INPUTS					OUTPUT
A1	A0	B1	B0	CE	C1
H	X	H	X	X	H
H	H	X	H	X	H
H	H	X	X	H	H
L	X	X	X	X	L
X	L	L	X	X	L
X	X	L	L	L	L

FUNCTION TABLE FOR C2 OUTPUT

INPUTS							OUTPUT
A2	A1	A0	B2	B1	B0	CE	C2
H	X	X	H	X	X	X	H
H	H	X	X	H	X	X	H
H	H	H	X	X	H	X	H
H	H	H	X	X	X	H	H
L	X	X	X	X	X	X	L
X	L	X	L	X	X	X	L
X	X	L	L	L	X	X	L
X	X	X	L	L	L	L	L

FUNCTION TABLE FOR RCOA OUTPUT

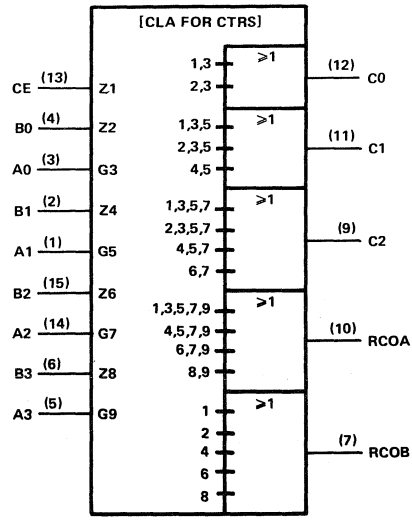
INPUTS							OUTPUT
A3	A2	A1	A0	B3	B2	B1	CE	RCOA
H	X	X	X	H	X	X	X	H
H	H	X	X	X	H	X	X	H
H	H	H	X	X	X	H	X	H
H	H	H	H	X	X	X	H	H
L	X	X	X	X	X	X	X	L
X	L	X	X	L	X	X	X	L
X	X	L	X	L	L	X	X	L
X	X	X	L	L	L	L	X	L
X	X	X	X	L	L	L	L	L

FUNCTION TABLE FOR RCOB OUTPUT

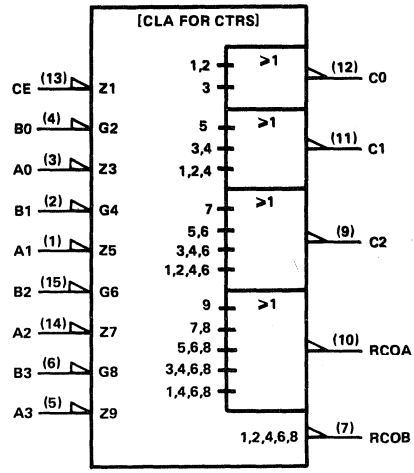
INPUTS					OUTPUT
B3	B2	B1	B0	CE	RCOB
H	X	X	X	X	H
X	H	X	X	X	H
X	X	H	X	X	H
X	X	X	H	X	H
X	X	X	X	H	H
L	L	L	L	L	L

logic symbols

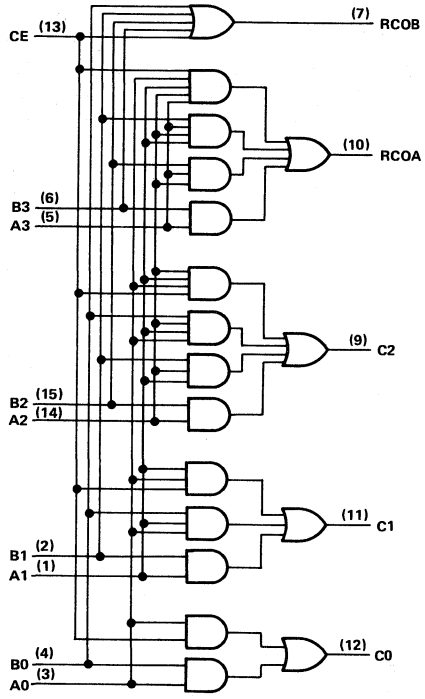
ACTIVE-HIGH INPUTS



ACTIVE-LOW INPUTS



logic diagram (positive logic)



absolute maximum ratings over free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS264 . . . . . −55°C to 125°C
SN74AS264 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS264			SN74AS264			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS264			SN74AS264			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I	CE	V_{CC} = 5.5 V,	V_I = 7 V			500			500	μA
	A0, A2					700			700	
	A1					800			800	
	A3, B0, B1					400			400	
	B2					300			300	
	B3					200			200	
I_{IH}	CE	V_{CC} = 5.5 V,	V_I = 2.7 V			100			100	μA
	A0, A2					140			140	
	A1					160			160	
	A3, B0, B1					80			80	
	B2					60			60	
	B3					40			40	
I_{IL}	CE	V_{CC} = 5.5 V,	V_I = 0.4 V			−2.5			−2.5	mA
	A0					−3.5			−3.5	
	A1, A2					−4			−4	
	A3, B0, B1					−2			−2	
	B2					−1			−1	
	B3					−1.5			−1.5	
I_O‡		V_{CC} = 5.5 V	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}		V_{CC} = 5.5 V			26			26		mA
I_{CCL}					28			28		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 50 Ω, T_A = MIN to MAX						UNIT
			SN54AS264			SN74AS264			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	CE	C0, C1, C2		6			6		ns
t_{PHL}				5			5		
t_{PLH}	An or Bn	C0, C1, C2		5			5		ns
t_{PHL}				5			5		
t_{PLH}	An, Bn, or CE	RCOA		5			5		ns
t_{PHL}				5			5		
t_{PLH}	Bn or CE	RCOB		5			5		ns
t_{PHL}				5			5		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TYPICAL APPLICATION INFORMATION

The circuit shown in Figure 1 illustrates how the 'AS624 can implement look-ahead carry for the active-high-carry 'AS163, while Figure 2 shows the look-ahead carry for the active-low-carry 'AS169.

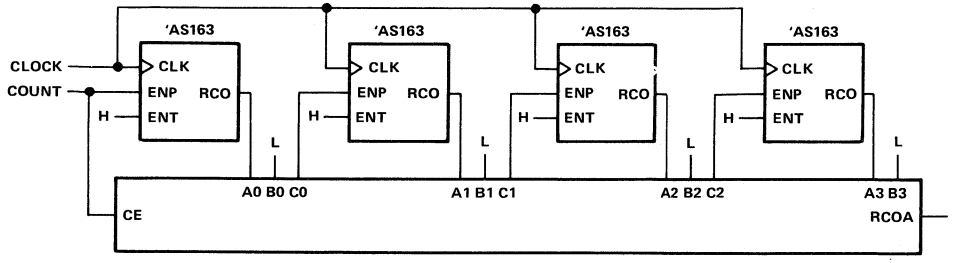


FIGURE 1–ACTIVE-HIGH-CARRY

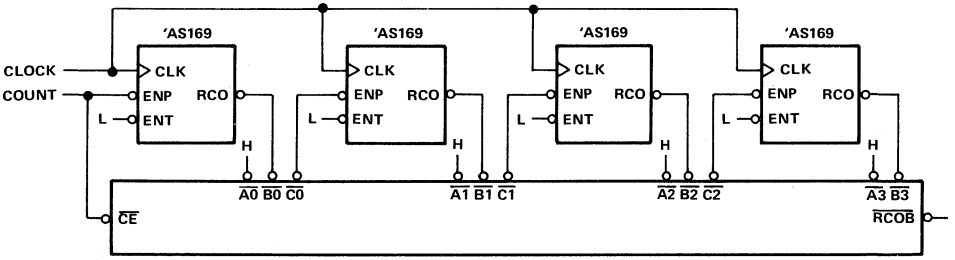
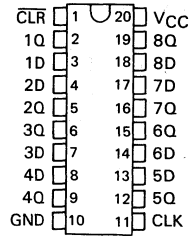


FIGURE 2–ACTIVE-LOW-CARRY

D2661, APRIL 1982—REVISED DECEMBER 1983

- Contains Eight Flip-Flops with Single-Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications Include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators
- Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS273 . . . J PACKAGE
SN74ALS273 . . . N PACKAGE
SN74ALS273 . . . DW PACKAGE
(TOP VIEW)



2

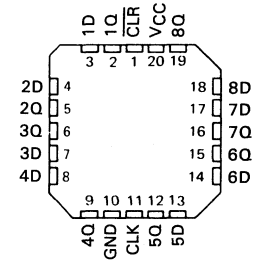
description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

The SN54ALS273 is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS273 is characterized for operation from 0 °C to 70 °C.

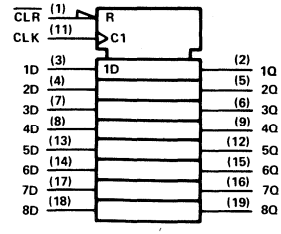
SN54ALS273 . . . FH OR FK PACKAGE
SN74ALS273 . . . FN PACKAGE
(TOP VIEW)



FUNCTION TABLE
(EACH FLIP-FLOP)

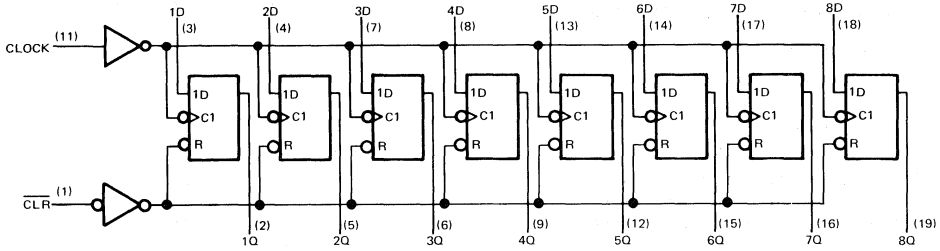
INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

logic symbol



Pin numbers shown are for J and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS273 . . . . . −55 °C to 125 °C
SN74ALS273 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54ALS273			SN74ALS273			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency		0		30	0		35	MHz
t_w	Pulse duration	$\overline{CLR}$ low	10			10			ns
		CLK high	16.5			14			
		CLK low	16.5			14			
t_{su}	Setup time before CLK↑	Data	10			10			ns
		Clear inactive state	15			15			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS273			SN74ALS273			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V			11	20		11	20	mA
I_{CCL}	V_{CC} = 5.5 V			19	29		19	29	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

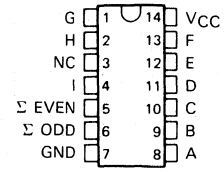
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS273		SN74ALS273		
			MIN	MAX	MIN	MAX	
f_{max}			30		35		MHz
t_{PHL}	$\overline{CLR}$	Any Q	4	21	4	18	ns
t_{PLH}	CLR	Any Q	2	16	2	12	ns
t_{PHL}			3	17	3	15	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D2661, DECEMBER 1982—REVISED NOVEMBER 1984

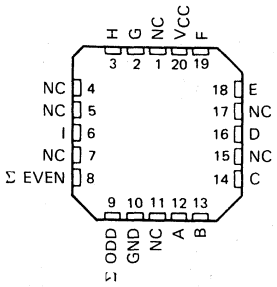
- Generates Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bits Parity
- Can Be Used to Upgrade Existing Systems using MSI Parity Circuits
- Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS280, SN54AS280 . . . J PACKAGE
SN74ALS280, SN74AS280 . . . N PACKAGE
SN74ALS280, SN74AS280 . . . D PACKAGE
(TOP VIEW)



2

SN54ALS280, SN54AS280 . . . FH OR FK PACKAGE
SN74ALS280, SN74AS280 . . . FN PACKAGE
(TOP VIEW)

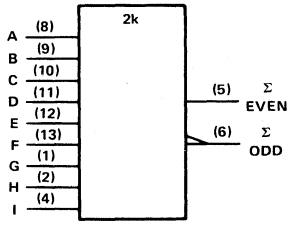


NC—No internal connection

FUNCTION TABLE

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0,2,4,6,8	H	L
1,3,5,7,9	L	H

logic symbol



Pin numbers shown are for J and N packages.

description

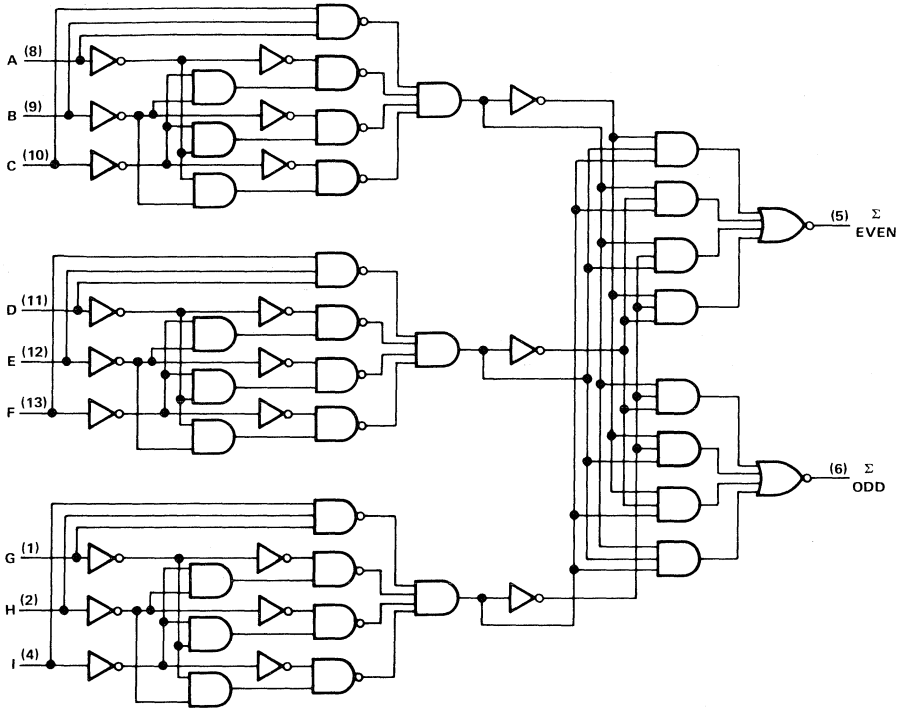
These universal, monolithic, nine-bit parity generators/checkers utilize Advanced Schottky high-performance circuitry and feature odd and even outputs to facilitate operation of either odd or even parity application. The word-length capability is easily expanded by cascading.

These devices can be used to upgrade the performance of most systems utilizing the '180 parity generator/checker. Although the 'ALS280 and 'AS280 are implemented without expander inputs, the corresponding function is provided by the availability of an input at pin 4 and the absence of any internal connection at pin 3. This permits the 'ALS280 and 'AS280 to be substituted for the '180 in existing designs to produce an identical function even if the devices are mixed with existing '180's.

All 'AS280 inputs are buffered to lower the drive requirements.

The SN54' Family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' Family is characterized for operation from 0°C to 70°C.

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS280 . . . . . −55°C to 125°C
SN74ALS280 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS280			SN74ALS280			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS280			SN74ALS280			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−2			−2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			9			9		mA

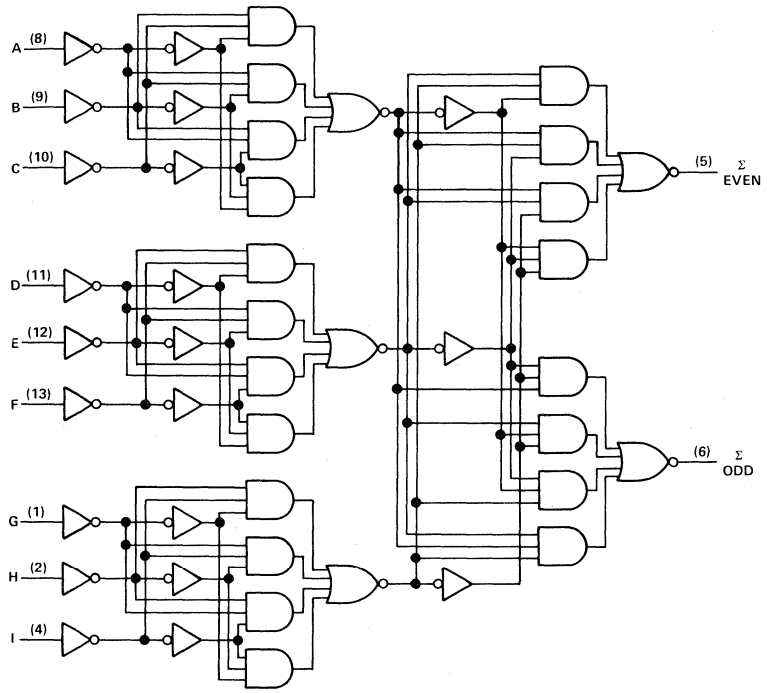
†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX			UNIT
			SN54/74ALS280			SN54ALS280		SN74ALS280	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Σ Even		14						ns
t_{PHL}				14						
t_{PLH}	Any	Σ Odd		14						ns
t_{PHL}				14						

NOTE 1: For load circuit and voltage waveforms, see page 1-12

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS280 . . . . . −55°C to 125°C
SN74AS280 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS280			SN74AS280			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS280			SN74AS280			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			25	40		25	35	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

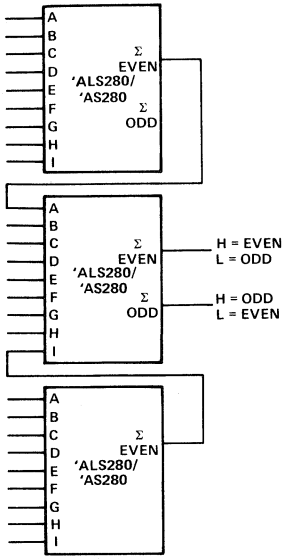
switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54/74AS280			SN54AS280		SN74AS280		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Σ Even		8.5	10.8	3	13	3	12	ns
t_{PHL}				7.5	10	3	12.5	3	11	
t_{PLH}	Any	Σ Odd		7.5	10.8	3	13	3	12	ns
t_{PHL}				8	10.5	3	12.5	3	11.5	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

TYPICAL APPLICATION DATA

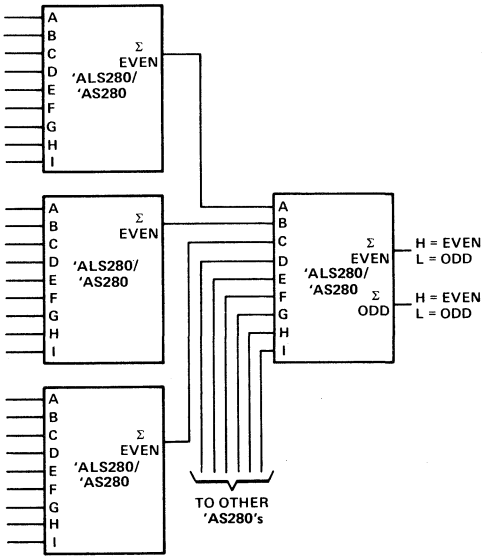
25-LINE PARITY/GENERATOR CHECKER



Three 'ALS280/'AS280 can be used to implement a 25-line parity generator/checker.

As an alternative, the outputs of two or three parity generators/checkers can be decoded with a 2-input ('S86 or 'LS86) or 3-input ('S135) exclusive-OR gate for 18- or 27-line parity applications.

81-LINE PARITY/GENERATOR CHECKER

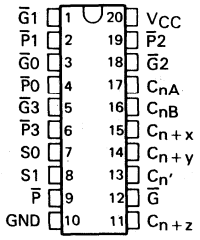


Longer word lengths can be implemented by cascading 'ALS280/'AS280. As shown here, parity can be generated for word lengths up to 81 bits.

D2811, DECEMBER 1983

- **Selectable Carry Inputs Version of the Popular 'S182 Allows Double Precision Carry**
- **Offers Carry Functions in a Compatible Form for Direct Connection to the ALU**
- **Cascadable to Perform Look-Ahead Across n-Bit Adders**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS282 . . . J PACKAGE
SN74AS282 . . . N PACKAGE
SN74AS282 . . . DW PACKAGE
(TOP VIEW)



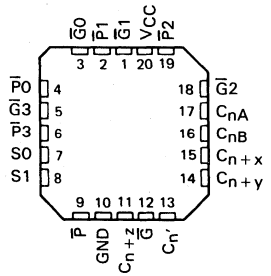
2

PIN DESIGNATIONS

ALTERNATIVE DESIGNATIONS†		FUNCTION
$\overline{G}0$, $\overline{G}1$, $\overline{G}2$, $\overline{G}3$	G0, G1, G2, G3	Carry Generate Inputs
$\overline{P}0$, $\overline{P}1$, $\overline{P}2$, $\overline{P}3$	P0, P1, P2, P3	Carry Propagate Inputs
C_{nA}, C_{nB}	$\overline{C}_{nA}$, $\overline{C}_{nB}$	Carry Inputs
$C_{n'}$	$\overline{C}_{n'}$	Selected Carry
C_{n+x}, C_{n+y}, C_{n+z}	$\overline{C}_{n+x}$, $\overline{C}_{n+y}$, $\overline{C}_{n+z}$	Carry Outputs
$\overline{G}$	Y	Carry Generate Outputs
$\overline{P}$	X	Carry Propagate Outputs
S0, S1		Carry Select Inputs
V_{CC}		Supply Voltage
GND		Ground

† Interpretations are illustrated in connection with the Function Tables for the 'AS181A and 'AS881A.

SN54AS282 . . . FH OR FK PACKAGE
SN74AS282 . . . FN PACKAGE
(TOP VIEW)



description

The 'AS282 look-ahead carry generator is capable of anticipating a carry across four binary adders or group of adders. They are cascadable to perform full look-ahead across n-bit adders. The 'AS282 is functionally the same as the SN54AS182/SN74AS182 except that the carry input (C_n) is selected from C_{nA}, C_{nB}, and their complements $\overline{C}_{nA}$ and $\overline{C}_{nB}$. The logic equations are written in terms of the selected carry C_n. This signal is also available as an output at $C_{n'}$.

When used in conjunction with the 'AS181A, 'AS881A, or 'AS888 arithmetic logic unit (ALU), this generator provides high-speed carry look-ahead capability for any word length. The 'AS282 generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry across sections of four look-ahead circuits may be employed to anticipated carry across sections of four look-ahead packages up to n-bits. The method of cascading 'AS282 circuits to perform multi-level look-ahead is illustrated under typical application data.

logic equations

$$C_{n+x} = G0 + P0\ C_n$$
$$C_{n+y} = G1 + P1\ G0 + P1\ P0\ C_n$$
$$C_{n+z} = G2 + P2\ G1 + P2\ P1\ G0 + P2\ P1\ P0\ C_n$$
$$\overline{G} = \overline{G3 + P3\ G2 + P3\ P2\ G1 + P3\ P2\ P1\ G0}$$
$$\overline{P} = \overline{P3\ P2\ P1\ P0}$$

or

$$\overline{C}_{n+x} = \overline{Y0\ (X0 + C_n)}$$
$$\overline{C}_{n+y} = \overline{Y1\ [X1 + Y0\ (X0 + C_n)]}$$
$$\overline{C}_{n+z} = \overline{Y2\ \{X2 + Y1\ [X1 + Y0\ (X0 + C_n)]\}}$$
$$Y = Y3\ (X3 + Y2)\ (X3 + X2 + Y1)\ (X3 + X2 + X1 + Y0)$$
$$X = X3 + X2 + X1 + X0$$

FUNCTION TABLE FOR $\overline{G}$ OUTPUT

INPUTS							OUTPUT
$\overline{G}3$	$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All other combinations							H

FUNCTION TABLE FOR $\overline{P}$ OUTPUT

INPUTS				OUTPUT
$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	$\overline{P}$
L	L	L	L	L
All other combinations				H

FUNCTION TABLE FOR C_n' OUTPUT

INPUTS		OUTPUT
S1	S0	C_n'
L	L	C_{nA}
L	H	$\overline{C}_{nA}$
H	L	C_{nB}
H	H	$\overline{C}_{nB}$

FUNCTION TABLE FOR C_{n+x} OUTPUT

INPUTS			OUTPUT
$\overline{G}0$	$\overline{P}0$	Cn'	C_{n+x}
L	X	X	H
X	L	H	H
All other combinations			L

FUNCTION TABLE C_{n+y} OUTPUT

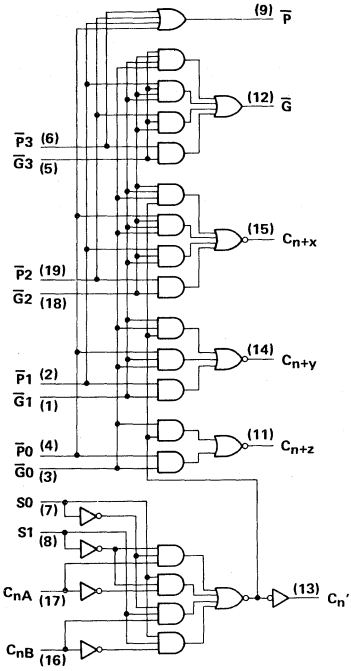
INPUTS					OUTPUT
$\overline{G}1$	$\overline{G}0$	$\overline{P}1$	$\overline{P}0$	C_n'	C_{n+y}
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

FUNCTION TABLE FOR C_{n+z} OUTPUT

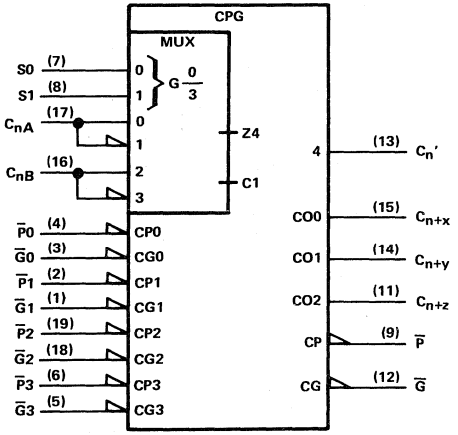
INPUTS							OUTPUT
$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	C_n'	C_{n+z}
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All other combinations							L

H = high-level, L = low level, X = irrelevant.
Any inputs not shown in a given table are irrelevant with respect to that output.

logic diagram (positive logic)



logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS282 . . . . . −55°C to 125°C
SN74AS282 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS282			SN74AS282			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS282			SN74AS282			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I	C_{nA}, C_{nB}	V_{CC} = 5.5 V,	V_I = 7 V			200			200	µA
	S0, S1, $\overline{P}$3					200			200	
	$\overline{P}$2					300			300	
	$\overline{P}$0, $\overline{P}$1, $\overline{G}$3					400			400	
	$\overline{G}$0, $\overline{G}$2					700			700	
	$\overline{G}$1					800			800	
I_{IH}	C_{nA}, C_{nB}	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	µA
	S0, S1, $\overline{P}$3					40			40	
	$\overline{P}$2					60			60	
	$\overline{P}$0, $\overline{P}$1, $\overline{G}$3					80			80	
	$\overline{G}$0, $\overline{G}$2					140			140	
	$\overline{G}$1					160			160	
I_{IL}	C_{nA}, C_{nB}	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	S0, S1, $\overline{P}$3					−1			−1	
	$\overline{P}$2					−1.5			−1.5	
	$\overline{P}$0, $\overline{P}$1, $\overline{G}$3					−2			−2	
	$\overline{G}$0, $\overline{G}$2					−3.5			−3.5	
	$\overline{G}$1					−4			−4	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}		V_{CC} = 5.5 V			22			22		mA
I_{CCL}					26			26		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS282			SN74AS282			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	S0, S1, C_{nA}, or C_{nB}	$C_{n'}$		6			6		ns
t_{PHL}				6			6		
t_{PLH}	S0, S1, C_{nA}, or C_{nB}	C_{n+x}, C_{n+y}, C_{n+z}		6			6		ns
t_{PHL}				6			6		
t_{PLH}	$\overline{P}$ or $\overline{G}$	C_{n+x}, C_{n+y}, C_{n+z}		5			5		ns
t_{PHL}				5			5		
t_{PLH}	$\overline{P}$ or $\overline{G}$	$\overline{G}$		6			6		ns
t_{PHL}				5			5		
t_{PLH}	$\overline{P}$	$\overline{P}$		5			5		ns
t_{PHL}				5			5		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TYPICAL APPLICATION DATA

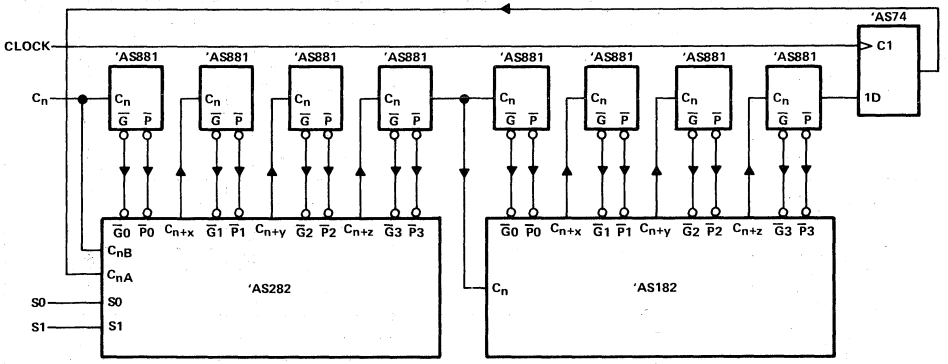
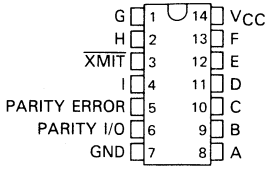


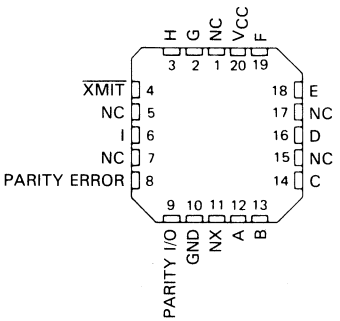
FIGURE 1–32-BIT LOOK-AHEAD CARRY WITH DOUBLE-PRECISION CARRY IN 'AS282 AND 'AS182

- **Generates Either Odd or Even Parity for Nine Data Lines**
- **Cascadable for n-Bits Parity**
- **Direct Bus Connection for Parity Generation or for Checking by Using the Parity I/O Port**
- **Glitch-Free Bus During Power Up/Down**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS286 . . . J PACKAGE
SN74AS286 . . . N PACKAGE
SN74AS286 . . . D PACKAGE
(TOP VIEW)



SN54AS286 . . . FH OR FK PACKAGE
SN74AS286 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

The SN54AS286 and SN74AS286 universal nine-bit parity generators/checkers feature a local output for parity checking and a 48-milliampere bus-driving parity I/O port for parity generation/checking. The word-length capability is easily expanded by cascading.

The $\overline{\text{XMIT}}$ control input is implemented specifically to accommodate cascading. When $\overline{\text{XMIT}}$ is low the parity tree is disabled and PE will remain at a high logic level regardless of the input levels. When $\overline{\text{XMIT}}$ is high the parity tree is enabled. The Parity Error output will indicate a parity error when either an even number of inputs (A through I) are high and Parity I/O is forced to a low logic level, or when an odd number of inputs are high and Parity I/O is forced to a high logic level.

The I/O control circuitry was designed so that the I/O port will remain in the high-impedance state during power-up or power-down to prevent bus glitches.

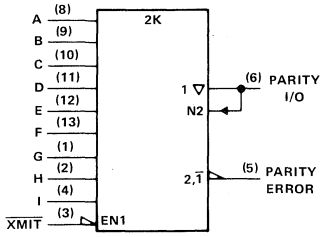
The SN54AS286 is characterized for operation over the full military range of −55°C to 125°C. The SN74AS286 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

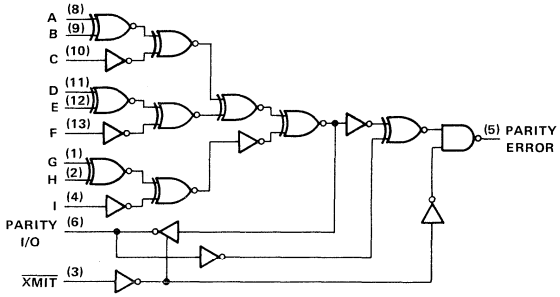
NUMBER OF INPUTS (A THRU I) THAT ARE HIGH	$\overline{XMIT}$	PARITY I/O	PARITY ERROR
0, 2, 4, 6, 8	l	H	H
1, 3, 5, 7, 9	l	L	H
0, 2, 4, 6, 8	h	h	H
	h	l	L
1, 3, 5, 7, 9	h	h	L
	h	l	H

h — high input level
H — high output level
l — low input level
L — low output level

logic symbol



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS286 . . . . . −55°C to 125°C
SN74AS286 . . . . . 0°C to 70°C
Storage temperature . . . . . −65°C to 140°C

recommended operating conditions

			SN54AS286			SN74AS286			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	Parity error			−2			−2	mA
		Parity I/O			−12			−15	
I_{OL}	Low-level output current	Parity error			20			20	mA
		Parity I/O			32			48	
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS286			SN74AS286			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	Parity I/O	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	2.9		2.4	3		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.5			
V_{OL}	Parity error	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
	Parity I/O	V_{CC} = 4.5 V,	I_{OL} = 32 mA			0.5				
		V_{CC} = 4.5 V,	I_{OL} = 48 mA						0.5	
I_I	Parity I/O	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
	All other inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	
I_{IH}	Parity I/O‡	V_{CC} = 5.5 V,	V_I = 2.7 V			50			50	μA
	All other inputs					20			20	
I_{IL}	Parity I/O‡	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	All other inputs					−0.5			−0.5	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	Transmit	V_{CC} = 5.5 V			30	43		30	43	mA
	Receive				35	50		35	50	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS286		SN74AS286		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any A thru I	Parity I/O	3	17	3	15	ns
t_{PHL}			3	15	3	14	
t_{PLH}	Any A thru I	Parity error	3	20	3	16.5	ns
t_{PHL}			3	18	3	16.5	
t_{PLH}	Parity I/O	Parity error	3	10	3	9	ns
t_{PHL}			3	10	3	9	
t_{PZH}	$\overline{XMIT}$	Parity I/O	3	14	3	13	ns
t_{PZL}			3	17	3	16	
t_{PHZ}			3	13	3	11.5	
t_{PLZ}			3	11	3	10	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

TYPICAL APPLICATION DATA

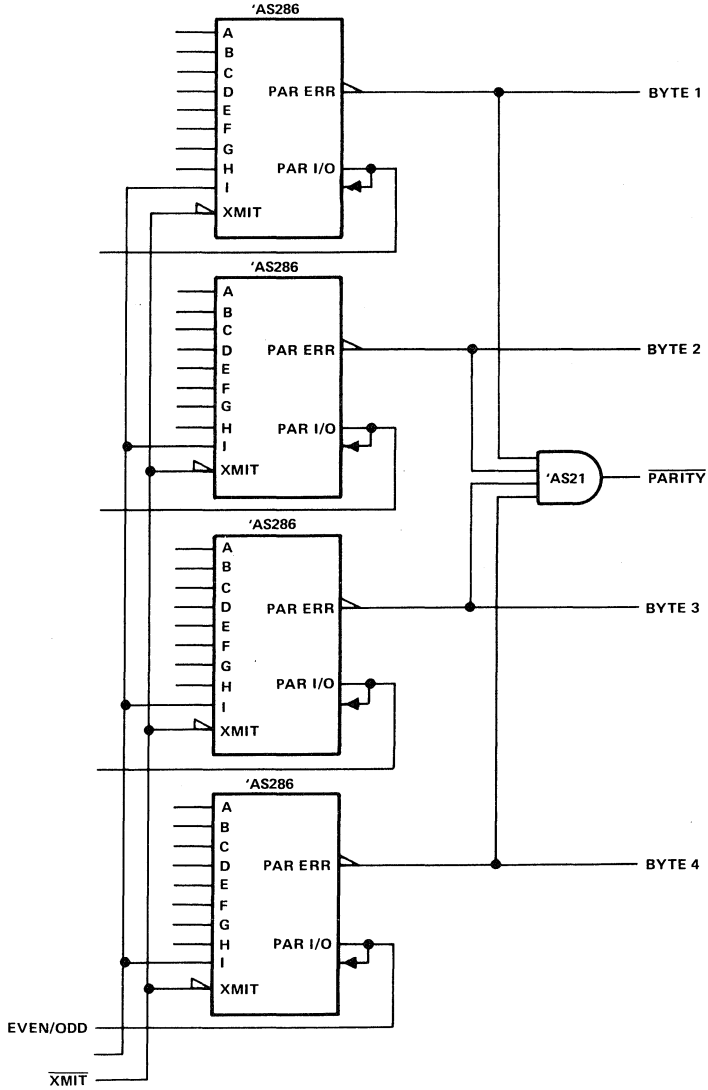


FIGURE 1–32-BIT PARITY GENERATOR/CHECKER

Figure 1 shows a 32-bit parity generator/checker with output polarity-switching, parity error detection, and parity on every byte.

TYPICAL APPLICATION DATA

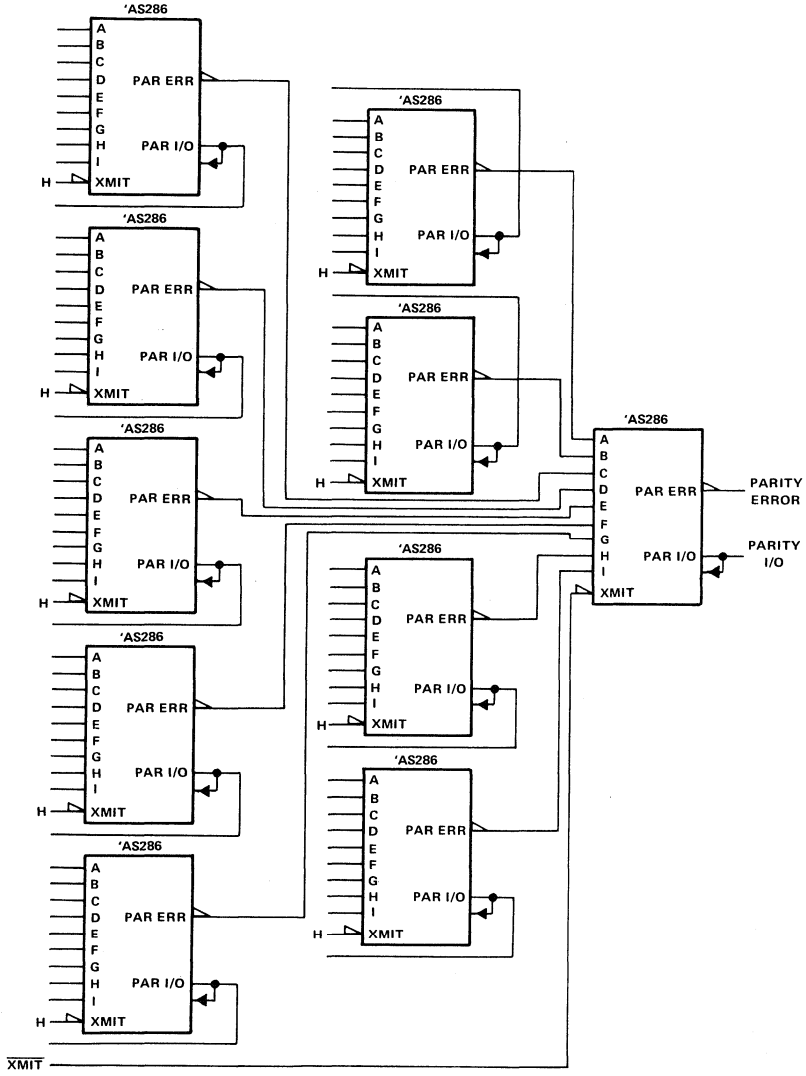


FIGURE 2–90-BIT PARITY GENERATOR/CHECKER WITH PARITY ERROR DETECTION

In Figure 2, a 90-bit parity generator/checker with the $\overline{\text{XMIT}}$ on the last stage is available for use with parity detection.

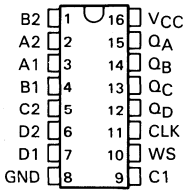
D2661, DECEMBER 1983 — REVISED FEBRUARY 1984

- **Selects One of Two 4-Bit Data Sources and Stores Data Synchronously with System Clock**
- **Applications:**
  Dual Source for Operands and Constants in Arithmetic Processor; Can Release Processor Register Files for Acquiring New Data

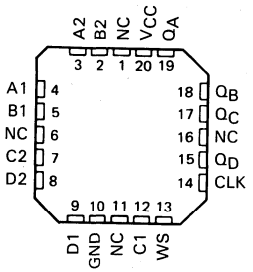
  Implements Separate Registers Capable of Parallel Exchange of Contents, yet Retains External Load Capability

  Has Universal-Type Register for Implementing Various Shift Patterns; even Has Compound Left-Right Capability
- **Dependable Texas Instruments Quality and Reliability**

SN54AS298 . . . J PACKAGE
SN74AS298 . . . N PACKAGE
SN74AS298 . . . D PACKAGE
(TOP VIEW)



SN54AS298 . . . FH OR FK PACKAGE
SN74AS298 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

This quadruple two-input multiplexer with storage provides essentially the equivalent functional capabilities of two separate MSI functions (SN54AS157/SN74AS157 and SN54AS175/SN74AS175) in a single 16-pin package.

When the word-select (WS) input is low, Word 1 (A1, B1, C1, D1 is applied to the flip-flops. A high input to the word-select (WS) will cause the selection of Word 2 (A2, B2, C2, D2). The selected word is clocked to the output terminals on the negative-going edge of the clock pulse.

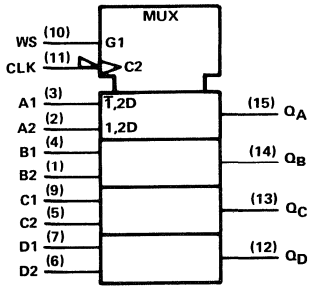
The SN54AS298 is characterized for operation over the full military range of −55°C to 125°C. The SN74AS298 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

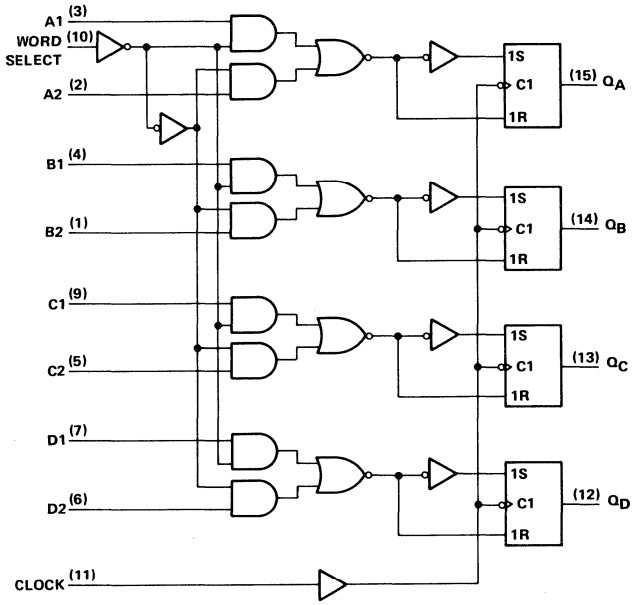
INPUTS		OUTPUTS			
WORD SELECT	CLOCK	Q_A	Q_B	Q_C	Q_D
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	H	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↓ = transition from high to low level
a1, a2, etc. = the level of steady-state input at A1, A2, etc.
Q_{A0}, Q_{B0}, etc. = the level of Q_A, Q_B, etc. entered on the most-recent ↓ transition of the clock input.

logic symbol



logic diagram (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS298 . . . . . −55°C to 125°C
SN74AS298 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS298			SN74AS298			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0		100	0		100	MHz
t_w	Pulse duration, CLK high or low		5			5			ns
t_{su}	Setup time before CLK ↓	Data	4.5			4.5			ns
		Word Select	13			13			
t_h	Hold time after CLK ↓	Data	3.5			3.5			ns
		Word Select	1			1			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS298			SN74AS298			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1			−1	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	WS	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All other					20			20	
I_{IL}	WS	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.75			−0.75	mA
	All other					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}		V_{CC} = 5.5 V			21	33		21	33	mA
I_{CCL}		V_{CC} = 5.5 V			22	36		22	36	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characterisitcs (see Note 1)

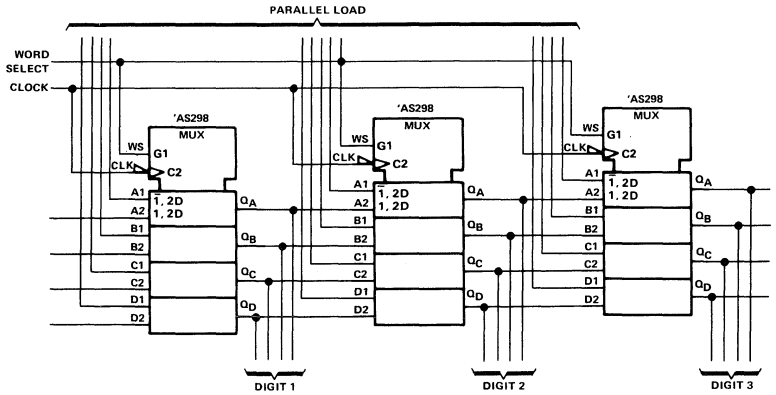
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS298		SN74AS298		
			MIN	MAX	MIN	MAX	
f_{max}			100		100		MHz
t_{PLH}	CLK	Q	2	16	2	9	ns
t_{PHL}			1	12	1	11	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

TYPICAL APPLICATION DATA

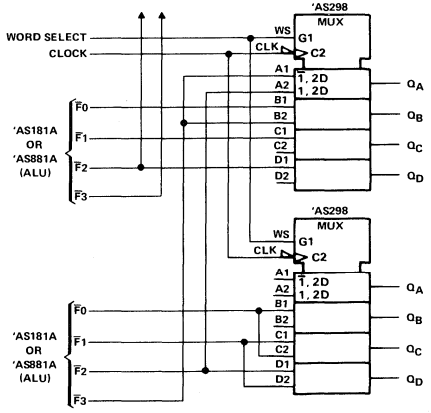
This versatile multiplexer/register can be connected to operate as a shift register that can shift N-places in a single clock pulse.

The following figure illustrates a BCD shift register that will shift an entire 4-bit BCD digit in one clock pulse.



When the word-select input is high and the registers are clocked, the contents of register 1 is transferred (shifted) to register 2, etc. In effect, the BCD digits are shifted one position. In addition, this application retains a parallel-load capability which means that new BCD data can be entered in the entire register with one clock pulse. This arrangement can be modified to perform the shifting of binary data for any number of bit locations.

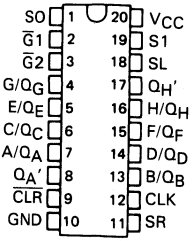
Another function that can be implemented with the 'AS298 is a register that can be designed specifically for supporting multiplier or division operations. The example below is a one-place/two-place shift register.



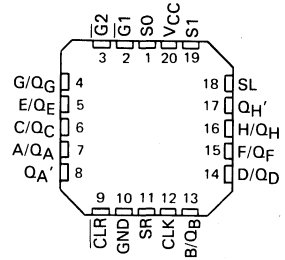
When word select is low and the register is clocked, the outputs of the arithmetic/logic units (ALUs) are shifted one place. When word select is high and the registers are clocked, the data is shifted two places.

- **Multiplexed I/O Ports Provides Improved Bit Density**
- **Four Modes of Operation: Hold (Store), Shift Right, Shift Left, and Load Data**
- **Operates with Outputs Enabled or at High Impedance**
- **3-State Outputs Drive Bus Lines Directly**
- **Can Be Cascaded for N-Bit Word Lengths**
- **'ALS299 and AS299 Have Direct Overriding Clear**
- **'ALS323 and AS323 Have Synchronous Clear**
- **Application:**
  Stacked or Push-Down Registers, Buffer Storage, and Accumulator Registers
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . N PACKAGE
SN74ALS', SN74AS' . . . DW PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FH OR FK PACKAGE
SN74ALS', SN74AS' . . . FN PACKAGE
(TOP VIEW)



description

These eight-bit universal registers feature multiplexed I/O ports to achieve full eight-bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines SO and S1 high. This places the three-state outputs in a high-impedance state and permits data that is applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs asynchronously on 'ALS299, 'AS299 and synchronously on 'ALS323, 'AS323 when $\overline{CLR}$ is low. Taking either of the output controls, $\overline{G}1$ or $\overline{G}2$, high disables the outputs but this has no effect on clearing, shifting, or storage of data.

The SN54' family is characterized for operation over the full military range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

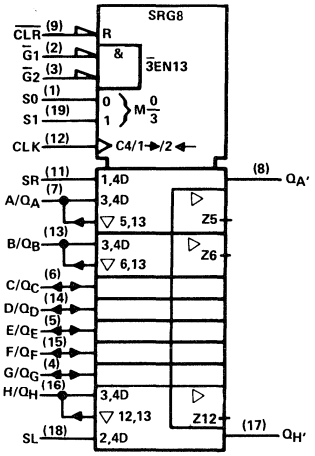
FUNCTION TABLE

MODE	INPUTS								I/O PORTS								OUTPUTS	
	$\overline{CLR}$	S1	S0	OUTPUT CONTROL $\overline{G1}$	OUTPUT CONTROL $\overline{G2}$	CLK	SL	SR	A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	Q_A'	Q_H'
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
('ALS299)	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
('AS299)	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
Clear	L	X	L	L	L	↑	X	X	L	L	L	L	L	L	L	L	L	L
('ALS323)	L	L	X	L	L	↑	X	X	L	L	L	L	L	L	L	L	L	L
('AS323)	L	H	H	X	X	↑	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

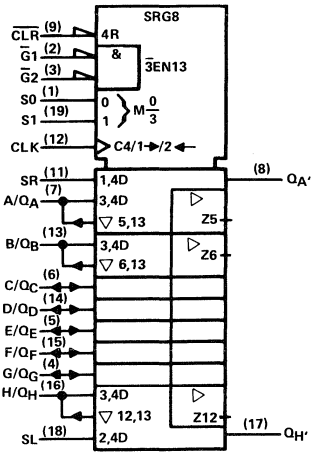
When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

logic symbols

'ALS299, 'AS299



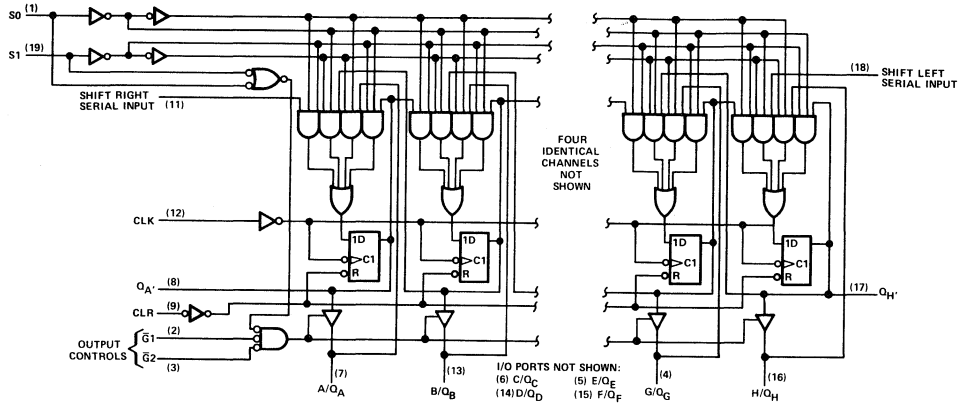
'ALS323, 'AS323



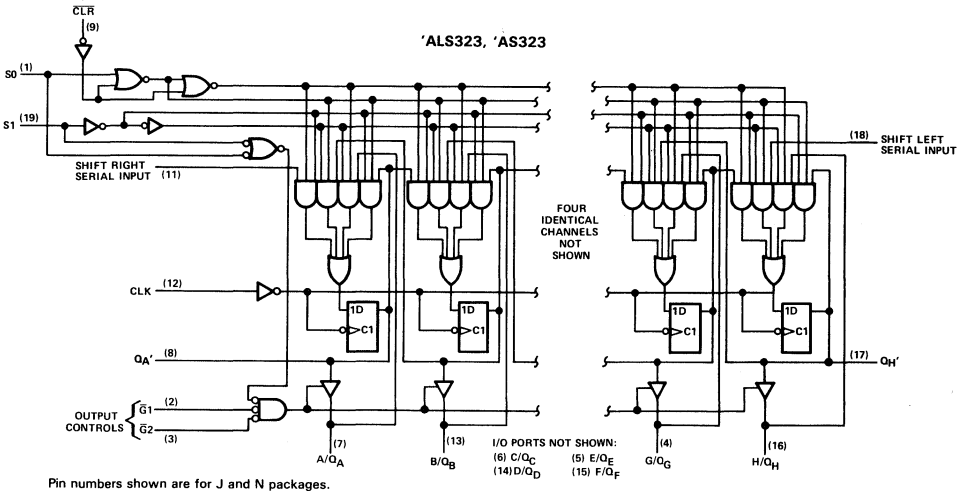
Pin numbers shown are for J and N packages.

logic diagrams (positive logic)

'ALS299, 'AS299



'ALS323, 'AS323



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS', SN54AS' . . . . . −55°C to 125°C
SN74ALS', SN74AS' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

				SN54ALS299 SN54ALS323			SN74ALS299 SN74ALS323			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
I_{OH}	High-level output current	$Q_{A'}$ or $Q_{H'}$				−0.4			−0.4	mA
		Q_A thru Q_H				−1			−2.6	
I_{OL}	Low-level output current	$Q_{A'}$ or $Q_{H'}$				4			8	mA
		Q_A thru Q_H				12			24	
f_{clock}	Clock frequency (at 50% duty cycle)			0		25	0		30	MHz
t_w	Pulse duration	CLK high or low		20			16.5			ns
		$\overline{CLR}$ low ('ALS299)		10		10				
t_{su}	Setup time before CLK↑	Select		25			20			ns
		Serial or Parallel data	High level	18			16			
			Low level	7			6			
		$\overline{CLR}$ inactive ('ALS299)		15			15			
		$\overline{CLR}$ active ('ALS323)		25			20			
		$\overline{CLR}$ inactive ('ALS323)		18			16			
t_h	Hold time after CLK↑	Select		0			0			ns
		Serial or parallel data		0			0			
T_A	Operating free-air temperature			−55		125	0		70°	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS299 SN54ALS323			SN74ALS299 SN74ALS323			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	Q_A thru Q_H	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	$Q_{A'}$ or $Q_{H'}$	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
	Q_A thru Q_H	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	A thru H	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
	Any other	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	
I_{IH}‡		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}‡	S0, S1, SR, SL	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	All others					−0.1			−0.1	
I_O§	$Q_{A'}$, $Q_{H'}$	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
	Q_A thru Q_H			−30		−112	−30		−112	
I_{CC}		V_{CC} = 5.5 V	Outputs high		15	28		15	28	mA
			Outputs low		22	38		22	38	
			Outputs disabled		23	40		23	40	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡For I/O ports (Q_A through Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS299 SN54ALS323		SN74ALS299 SN74ALS323		
			MIN	MAX	MIN	MAX	
f_{max}			25		30		MHz
t_{PLH}	CLK	Q_A thru Q_H	4	15	4	13	ns
t_{PHL}			7	25	7	19	
t_{PLH}	CLK	Q_A' or Q_H'	5	20	5	15	
t_{PHL}			8	21	8	18	
t_{PHL}	$\overline{CLR}$ ('ALS299 only)	Q_A thru Q_H	6	29	6	22	ns
		Q_A' or Q_H'	6	29	6	22	
t_{PZH}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H	6	21	6	16	ns
t_{PZL}			8	26	8	22	
t_{PZH}	S0, S1	Q_A thru Q_H	7	21	7	17	ns
t_{PZL}			8	26	8	22	
t_{PHZ}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H	1	10	1	8	ns
t_{PLZ}			5	23	5	15	
t_{PHZ}	S0, S1	Q_A thru Q_H	1	16	1	12	ns
t_{PLZ}			8	30	8	25	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

recommended operating conditions

				SN54AS299 SN54AS323			SN74AS299 SN74AS323			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level output voltage					0.8			0.8	V
I_{OH}	High-level output current	Q_A' or Q_H'				−2			−2	mA
		Q_A thru Q_H				−12			−15	
I_{OL}	Low-level output current	Q_A' or Q_H'				20			20	mA
		Q_A thru Q_H				32			48	
f_{clock}	Clock frequency (at 50% duty cycle)									MHz
t_w	Pulse duration	CLK high or low								ns
		$\overline{CLR}$ low ('AS299)								
t_{su}	Setup time before CLK↑	Select								ns
		Serial or Parallel data	High level							
			Low level							
		$\overline{CLR}$ inactive ('AS299)								
		$\overline{CLR}$ active ('AS323)								
		$\overline{CLR}$ inactive ('AS323)								
t_h	Hold time after CLK↑	Select								ns
		Serial or parallel data								
T_A	Operating free-air temperature			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS299 SN54AS323			SN74AS299 SN74AS323			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	Q_A thru Q_H	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.2		
V_{OL}	Q_A' or Q_H'	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	V
	Q_A thru Q_H	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	A thru H	V_{CC} = 5.5 V,	V_I = 5.5 V							mA
	Any other	V_{CC} = 5.5 V,	V_I = 7 V							
I_{IH}‡		V_{CC} = 5.5 V,	V_I = 2.7 V							μA
I_{IL}‡		V_{CC} = 5.5 V,	V_I = 0.4 V							mA
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high							mA
			Outputs low							
			Outputs disabled		95			95		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡For I/O ports (Q_A through Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

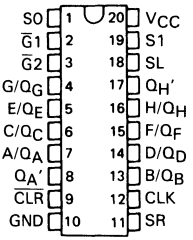
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS299 SN54AS323			SN74AS299 SN74AS323			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}									MHz
t_{PLH}	CLK	Q_A thru Q_H		10			10		ns
t_{PHL}				10			10		
t_{PLH}	CLK	Q_A' or Q_H'		10			10		
t_{PHL}				10			10		
t_{PHL}	$\overline{CLR}$	Q_A thru Q_H		12			12		ns
		Q_A' or Q_H'		12			12		
t_{PZH}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H		10			10		ns
t_{PZL}				10			10		
t_{PZH}	S0, S1	Q_A thru Q_H		10			10		ns
t_{PZL}				10			10		
t_{PHZ}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H		7			7		ns
t_{PLZ}				7			7		
t_{PHZ}	S0, S1	Q_A thru Q_H		7			7		ns
t_{PLZ}				7			7		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

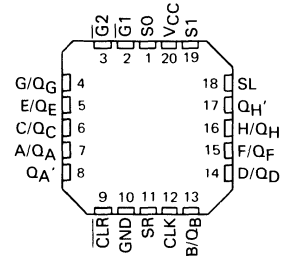
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- Multiplexed I/O Ports Provides Improved Bit Density
- Four Modes of Operation: Hold (Store), Shift Right, Shift Left, and Load Data
- Operates with Outputs Enabled or at High Impedance
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for N-Bit Word Lengths
- 'ALS323 and 'AS323 Have Synchronous Clear
- Application:
  Stacked or Push-Down Registers, Buffer Storage, and Accumulator Registers
- Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . N PACKAGE
SN74ALS', SN74AS' . . . DW PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FH OR FK PACKAGE
SN74ALS', SN74AS' . . . FN PACKAGE
(TOP VIEW)



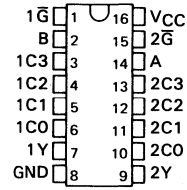
For complete information on the SN54ALS323, SN54AS323, SN74ALS323, SN74AS323, see page 2-299.

TYPES SN54ALS352, SN54AS352, SN74ALS352, SN74AS352
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

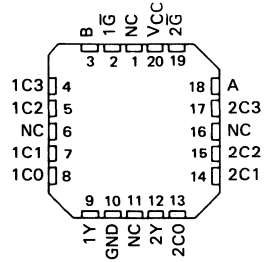
D2661, APRIL 1982—REVISED DECEMBER 1983

- **Inverting Versions of 'ALS153 and 'AS153**
- **Permits Multiplexing from N Lines to 1 Line**
- **Performs Parallel-to-Serial Conversion**
- **Strobe (Enable) Line Provided for Cascading (N Lines to n Lines)**
- **Typical 'ALS352 Power per Multiplexer . . . 16 mW**
- **Typical 'AS352 Average Propagation Delay Times**
  - **Data Input to Output . . . 2.7 ns**
  - **Strobe Input to Output . . . 4.5 ns**
  - **Select Input to Output . . . 4.5 ns**
- **Fully Compatible with Most TTL Circuits**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS352, SN54AS352 . . . J PACKAGE
SN74ALS352, SN74AS352 . . . N PACKAGE
SN74ALS352, SN74AS352 . . . D PACKAGE
(TOP VIEW)



SN54ALS352, SN54AS352 . . . FH OR FK PACKAGE
SN74ALS352, SN74AS352 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs ($\overline{G}$) are provided for each of the two four-line sections.

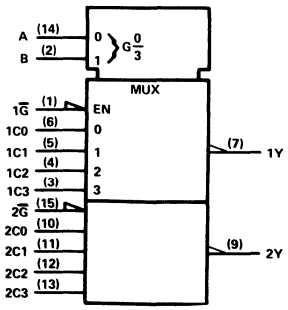
The SN54ALS352 and SN54AS352 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS352 and SN74AS352 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	H
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

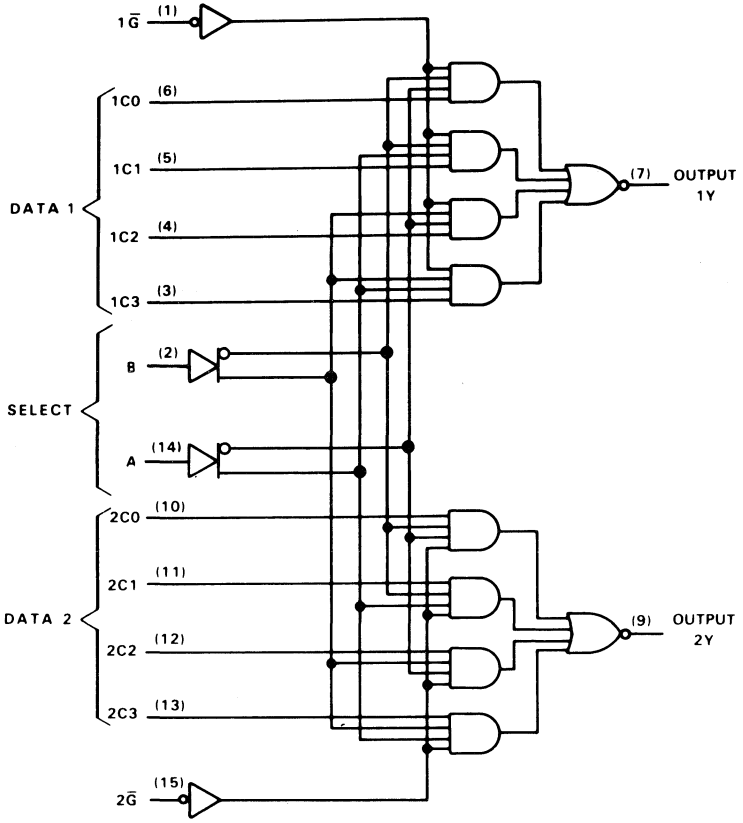
Select inputs A and B are common to both sections.

logic symbol



Pin numbers shown are for J and N packages.

logic diagram (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS352, SN54AS352 . . . . . −55 °C to 125 °C
SN74ALS352, SN74AS352 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS352			SN74ALS352			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS352			SN74ALS352			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V,	See Note 1		6.5	10		6.5	10	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with data and select inputs at 4.5 V, and G inputs grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS352		SN74ALS352		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	5	28	5	24	ns
t_{PHL}			5	24	5	21	
t_{PLH}	Data (Any C)	Y	3	21	3	18	ns
t_{PHL}			2	15	2	13	
t_{PLH}	$\overline{G}$	Y	4	22	4	18	ns
t_{PHL}			4	24	4	20	

NOTE 2: For load circuit and voltage waveforms, see page 1-12.

recommended operating conditions

		SN54AS352			SN74AS352			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			32			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS352			SN74AS352			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	A, B	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	A, B	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All others					20			20	
I_{IL}	A, B	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	All others					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		15.5	25		15.5	25	mA
			Outputs low		17.5	28		17.5	28	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

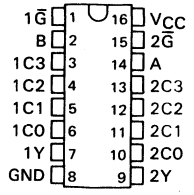
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS352		SN74AS352		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	4	12.5	4	11	ns
t_{PHL}			4	14	4	13	
t_{PLH}	Data (Any C)	Y	2	7.5	2	6.5	ns
t_{PHL}			2	7	2	6	
t_{PLH}	$\overline{G}$	Y	3	8	3	7	ns
t_{PHL}			4	13.5	4	12	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D2661, APRIL 1982—REVISED DECEMBER 1983

- **Inverting Versions of 'ALS253 and 'AS253**
- **Permits Multiplexing from N Lines to 1 Line**
- **Performs Parallel-to-Serial Conversion**
- **Typical 'ALS353 Power per Multiplexer . . . 20 mW**
- **Fully Compatible with Most TTL Circuits**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS353, SN54AS353 . . . J PACKAGE
SN74ALS353, SN74AS353 . . . N PACKAGE
SN74ALS353, SN74AS353 . . . D PACKAGE
(TOP VIEW)



2

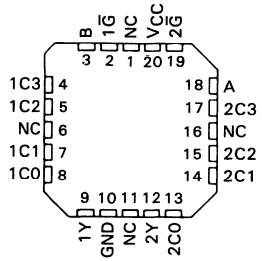
description

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs ($\overline{G}$) are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe ($\overline{G}$). The output is disabled when its strobe is high.

The SN54ALS353 and SN54AS353 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS353 and SN74AS353 are characterized for operation from 0°C to 70°C.

SN54ALS353, SN54AS353 . . . FH OR FK PACKAGE
SN74ALS353, SN74AS353 . . . FN PACKAGE
(TOP VIEW)



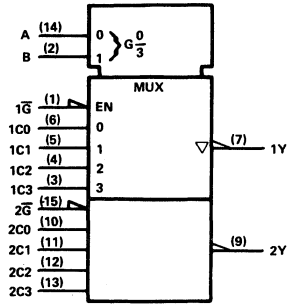
NC—No internal connection

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

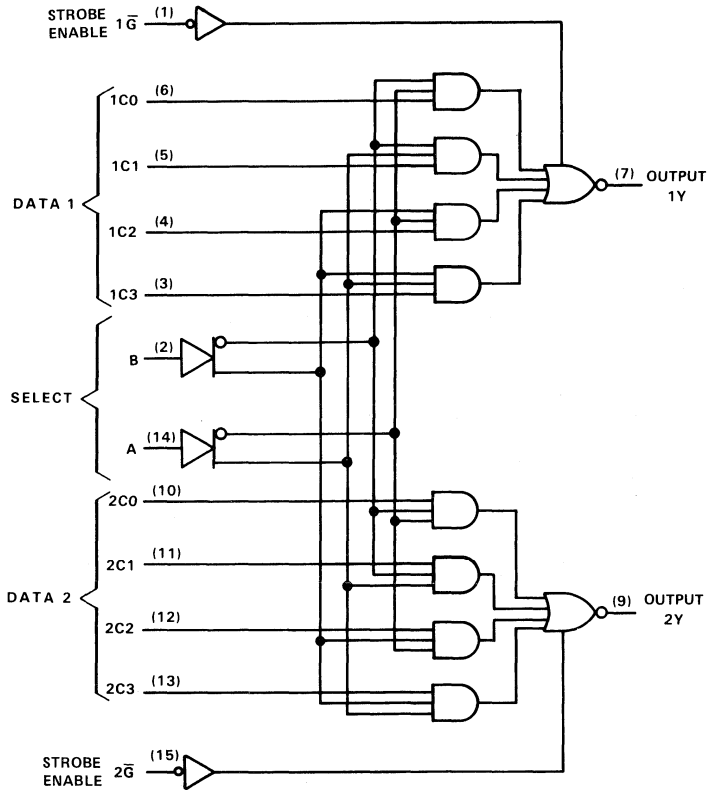
Select inputs A and B are common to both sections.

logic symbol



Pin numbers shown are for J and N packages

logic diagram (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS353, SN54AS353 . . . . . −55 °C to 125 °C
SN74ALS353, SN74AS353 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS353			SN74ALS353			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS353			SN74ALS353			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V,			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	disabled	V_{CC} = 5.5 V	All inputs, at 4.5 V		8	13		8	13	mA
	enabled		All inputs at Gnd		7	12		7	12	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS353		SN74ALS353		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	5	28	5	24	ns
t_{PHL}			5	24	5	21	
t_{PLH}	Data (Any C)	Y	4	21	4	18	ns
t_{PHL}			3	15	3	13	
t_{PZH}	$\overline{G}$	Y	3	15	3	13	ns
t_{PZL}			3	19	2	16	
t_{PHZ}	$\overline{G}$	Y	2	12	2	10	ns
t_{PLZ}			2	16	2	14	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

recommended operating conditions

		SN54AS353			SN74AS353			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			32			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS353			SN74AS353			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V,			−50			−50	μA
I_I	A, B	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	A, B	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All others					20			20	
I_{IL}	A, B	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	All others					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		15	24		15	24	mA
			Outputs low		19	31		19	31	
			Outputs disabled		18	30		18	30	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS353		SN74AS353		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	3	10	3	9	ns
t_{PHL}			4	14	4	12	
t_{PLH}	Data (Any C)	Y	3	8.5	3	7.5	ns
t_{PHL}			2	6.5	2	6	
t_{PZH}	Strobe	Y	3	8.5	3	7.5	ns
t_{PZL}			4	12	4	11	
t_{PHZ}	Strobe	Y	2	6.5	2	5.5	ns
t_{PLZ}			3	9	3	7.5	

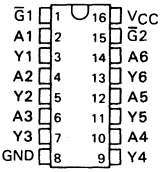
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D2661, DECEMBER 1982 – REVISED DECEMBER 1983

- **3-State Outputs Drive Bus Lines Or Buffer Memory Address Registers**
- **Choice of True or Inverting Outputs**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

'ALS365, 'ALS367	True Outputs
'ALS366, 'ALS368	Inverting Outputs

SN54ALS365, SN54ALS366 . . . J PACKAGE
SN74ALS365, SN74ALS366 . . . N PACKAGE
SN74ALS365, SN74ALS366 . . . D PACKAGE
(TOP VIEW)



2

description

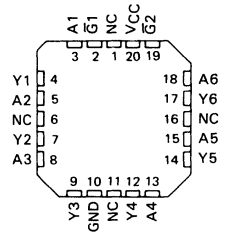
These Hex buffers and line drivers are designed specifically to improve both the performance and density of three state memory address drivers, clock drivers, and bus oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low control) inputs.

These devices feature high fan-out, and improved fan-in. The SN74ALS365 through SN74ALS368 can be used to drive terminated lines down to 133 ohms.

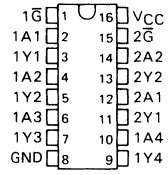
The -1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS' parts.

The SN54' family is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74' family is characterized for operation from 0 °C to 70 °C.

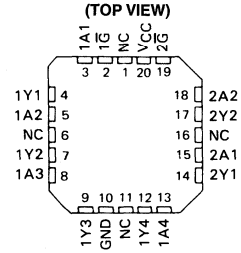
SN54ALS365, SN54ALS366 . . . FH OR FK PACKAGE
SN74ALS365, SN74ALS366 . . . FN PACKAGE
(TOP VIEW)



SN54ALS367, SN54ALS368 . . . J PACKAGE
SN74ALS367, SN74ALS368 . . . N PACKAGE
SN74ALS367, SN74ALS368 . . . D PACKAGE
(TOP VIEW)

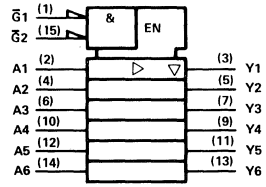


SN54ALS367, SN54ALS368 . . . FH OR FK PACKAGE
SN74ALS367, SN74ALS368 . . . FN PACKAGE
(TOP VIEW)

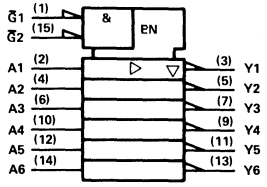


logic symbols

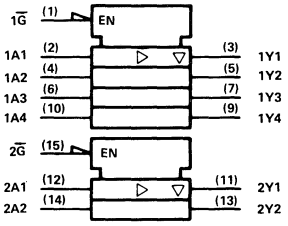
'ALS365



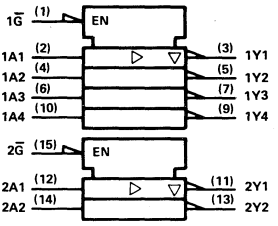
'ALS366



'ALS367

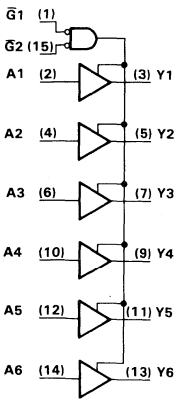


'ALS368

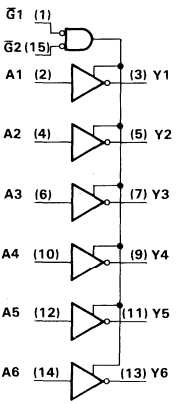


logic diagrams (positive logic)

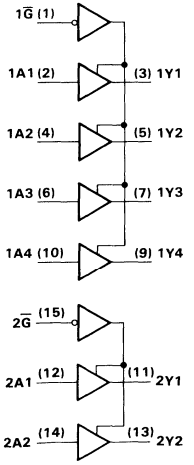
'ALS365



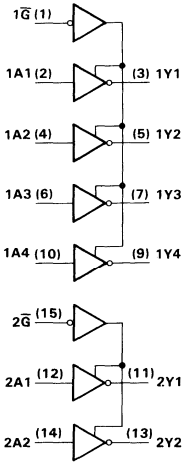
'ALS366



'ALS367



'ALS368



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS365 thru SN54ALS368 . . . . . −55°C to 125°C
SN74ALS365 thru SN74ALS368 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS365 THRU SN54ALS368			SN74ALS365 THRU SN74ALS368			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS365-1 thru SN74ALS368-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS365 THRU SN54ALS368			SN74ALS365 THRU SN74ALS368			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA				−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V, I_{OH} = −0.4 mA		V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V, I_{OH} = −3 mA		2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V, I_{OH} = −12 mA		2						
		V_{CC} = 4.5 V, I_{OH} = −15 mA					2			
V_{OL}		V_{CC} = 4.5 V, I_{OL} = 12 mA			0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 versions)						0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V, V_O = 2.7 V				20			20	μA
I_{OZL}		V_{CC} = 5.5 V, V_O = 0.4 V				−20			−20	μA
I_I		V_{CC} = 5.5 V, V_I = 7 V				0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V, V_I = 2.7 V				20			20	μA
I_{IL}		V_{CC} = 5.5 V, V_I = 0.4 V				−0.1			−0.1	mA
I_O§		V_{CC} = 5.5 V, V_O = 2.25 V		−30		−112	−30		−112	mA
I_{CC}	'ALS365 'ALS367	V_{CC} = 5.5 V	Outputs high		7			7		mA
			Outputs low		12			12		
			Outputs disabled		13			13		
	'ALS366 'ALS368		Outputs high		3			3		
			Outputs low		10			10		
			Outputs disabled		11			11		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS365, 'ALS367 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS365 SN54ALS367			SN74ALS365 SN74ALS367			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y		7			7		ns
t_{PHL}				7			7		
t_{PZH}	$\overline{G}$	Y		14			14		ns
t_{PZL}				14			14		
t_{PHZ}	$\overline{G}$	Y		5			5		ns
t_{PLZ}				8			8		

'ALS366, 'ALS368 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS366 SN54ALS368			SN74ALS366 SN74ALS368			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y		6			6		ns
t_{PHL}				5			5		
t_{PZH}	$\overline{G}$	Y		10			10		ns
t_{PZL}				17			17		
t_{PHZ}	$\overline{G}$	Y		6			6		ns
t_{PLZ}				6			6		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

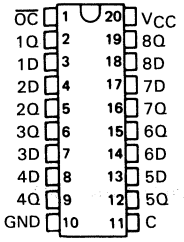
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TYPES SN54ALS373, SN54AS373, SN74ALS373, SN74AS373
OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

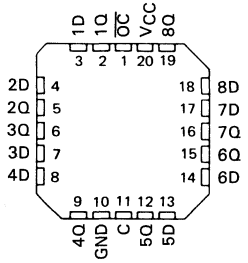
D2661, APRIL 1982—REVISED DECEMBER 1983

- 8 Latches in a Single Package
- 3-State Bus-Driving True Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- P-N-P Inputs Reduce D-C Loading on Data Lines
- Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS373, SN54AS373 . . . J PACKAGE
SN74ALS373, SN74AS373 . . . N PACKAGE
SN74ALS373, SN74AS373 . . . DW PACKAGE
(TOP VIEW)



SN54ALS373, SN54AS373 . . . FH OR FK PACKAGE
SN74ALS373, SN74AS373 . . . FN PACKAGE
(TOP VIEW)



description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'ALS373 and 'AS373 are transparent D-type latches. While the enable (C) is high the Q outputs will follow the data (D) inputs. When the enable is taken low, the Q outputs will be latched at the levels that were set up at the D inputs.

A buffered output-control input ($\overline{OC}$) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

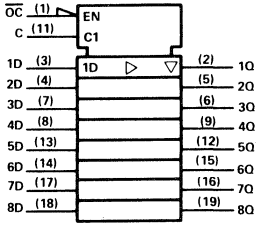
The output control $\overline{OC}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN54ALS373 and SN54AS373 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS373 and SN74AS373 are characterized for operation from 0 °C to 70 °C.

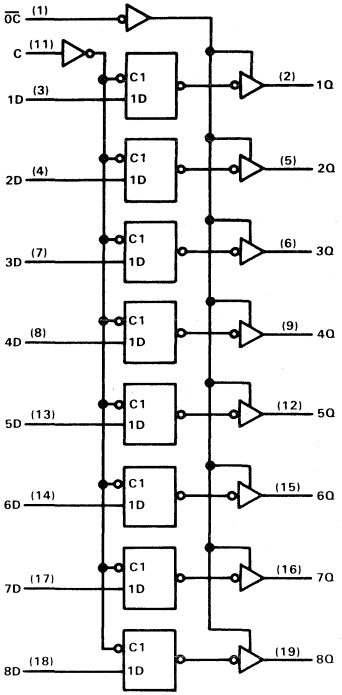
FUNCTION TABLE (EACH LATCH)

INPUTS			OUTPUT
$\overline{OC}$	ENABLE C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol



logic diagram (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS373, SN54AS373 . . . . . −55 °C to 125 °C
SN74ALS373, SN74AS373 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS373			SN74ALS373			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
t_w	Pulse duration, enable C high	10			10			ns
t_{su}	Setup time, data before enable C↓	10			10			ns
t_h	Hold time, data after enable C↓	7			7			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS373			SN74ALS373			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		9	16		9	16	mA
		Outputs low		16	25		16	25	
		Outputs disabled		17	27		17	27	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

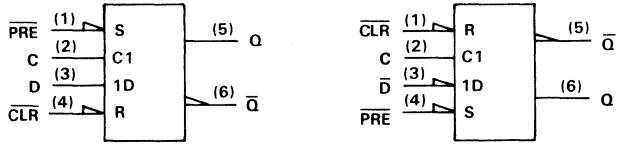
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS373		SN74ALS373		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	2	14	2	12	ns
t_{PHL}			4	19	4	16	
t_{PLH}	C	Any Q	6	26	6	22	ns
t_{PHL}			7	27	7	23	
t_{PZH}	$\overline{OC}$	Any Q	5	24	5	20	ns
t_{PZL}			6	22	6	18	
t_{PHZ}	$\overline{OC}$	Any Q	2	16	2	12	ns
t_{PLZ}			2	12	2	10	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D latch signal conventions

It is TI practice to name the outputs and other inputs of a D-type latch and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active low.

In some applications it may be advantageous to redesignate the data input $\overline{D}$. In that case all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.



Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (⊵) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 ($\overline{Q}$) is still in phase with the data input $\overline{D}$, but now both are considered active-low.

recommended operating conditions

		SN54AS373			SN74AS373			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	
I_{OL}	Low-level output current			32			48	mA
t_w	Pulse duration, enable C high	5.5			4.5			ns
t_{su}	Setup time, data before enable C↓	2			2			ns
t_h	Hold time, data after enable C↓	3			3			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS373			SN74AS373			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.27	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.32	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V		−0.02	−0.5		−0.02	−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		55	90		55	90	mA
		Outputs low		55	85		55	85	
		Outputs disabled		65	100		65	100	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

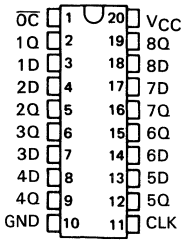
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS373		SN74AS373		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	3.5	8	3.5	6	ns
t_{PHL}			3.5	7	3.5	6	
t_{PLH}	C	Any Q	6.5	14	6.5	11.5	ns
t_{PHL}			5	8	5	7.5	
t_{PZH}	$\overline{OC}$	Any Q	2	7.5	2	6.5	ns
t_{PZL}			4.5	10.5	4.5	9.5	
t_{PHZ}	$\overline{OC}$	Any Q	3	7.5	3	6.5	ns
t_{PLZ}			3	8	3	7	

NOTE 1: For load circuits and voltage waveforms, see page 1-12.

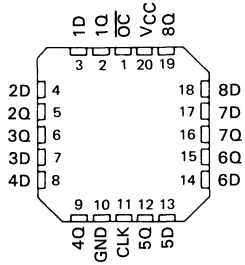
D2661, APRIL 1982—REVISED DECEMBER 1983

- D-Type Flip-Flops In a Single Package
- 3-State Bus-Driving True Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS374, SN54AS374 . . . J PACKAGE
SN74ALS374, SN74AS374 . . . N PACKAGE
SN74ALS374, SN74AS374 . . . DW PACKAGE
(TOP VIEW)



SN54ALS374, SN54AS374 . . . FH OR FK PACKAGE
SN74ALS374, SN74AS374 . . . FN PACKAGE
(TOP VIEW)



description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 'ALS374 and 'AS374 are edge-triggered D-type flip-flops. On the positive transition of the clock the Q outputs will be set to the logic levels that were set up at the D inputs.

A buffered output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

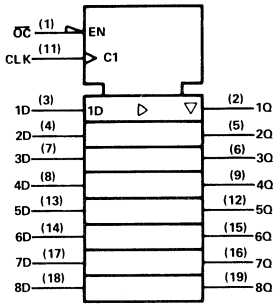
The output control ($\overline{OC}$) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS374 and SN54AS374 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS374 and SN74AS374 are characterized for operation from 0 °C to 70 °C.

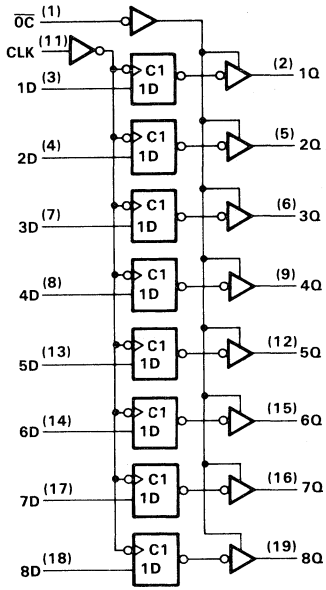
FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol



logic diagram (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS374, SN54AS374 . . . . . −55 °C to 125 °C
SN74ALS374, SN74AS374 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54ALS374			SN74ALS374			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	high-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency		0		30	0		35	MHz
t_w	Pulse duration	CLK high	16.5			14			ns
		CLK low	16.5			14			
t_{su}	Setup time, data before CLK↑		10			10			ns
t_h	Hold time, data after CLK↑		4			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS374			SN74ALS374			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		11	19		11	19	mA
		Outputs low		19	28		19	28	
		Outputs disabled		20	31		20	31	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

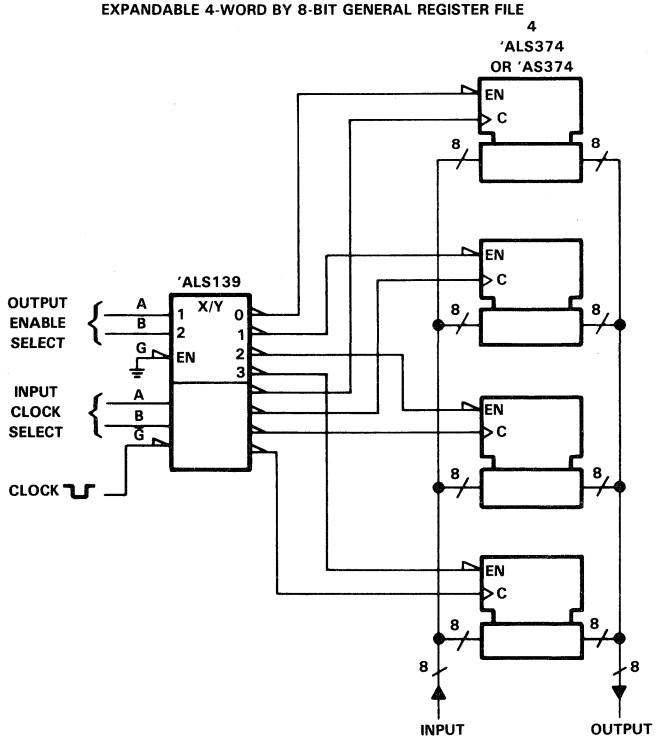
switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS374		SN74ALS374		
			MIN	MAX	MIN	MAX	
f_{max}			30		35		MHz
t_{PLH}	CLK	Q	3	15	3	12	ns
t_{PHL}			5	18	5	16	
t_{PZH}	$\overline{OC}$	Q	5	19	5	17	ns
t_{PZL}			7	20	7	18	
t_{PHZ}	$\overline{OC}$	Q	2	12	2	10	ns
t_{PLZ}			3	24	3	18	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TYPICAL APPLICATION DATA

EXPANDABLE 4-WORD BY 8-BIT GENERAL REGISTER FILE



recommended operating conditions

			SN54AS374			SN74AS374			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				32			48	mA
f_{clock}	Clock frequency		0		100	0		125	MHz
t_w	Pulse duration	CLK high	5.5			4			ns
		CLK low	5			3			
t_{su}	Setup time data before CLK↑		3			2			ns
t_h	Hold time, data after CLK↑		3			2			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS374			SN74AS374			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.29	0.5				V
		V_{CC} = 4.5 V	I_{OL} = 48 mA					0.34	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	OC, CLK	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	Data					−3			−2	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		77	120		77	120	mA
			Outputs low		84	128		84	128	
			Outputs disabled		84	128		84	128	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

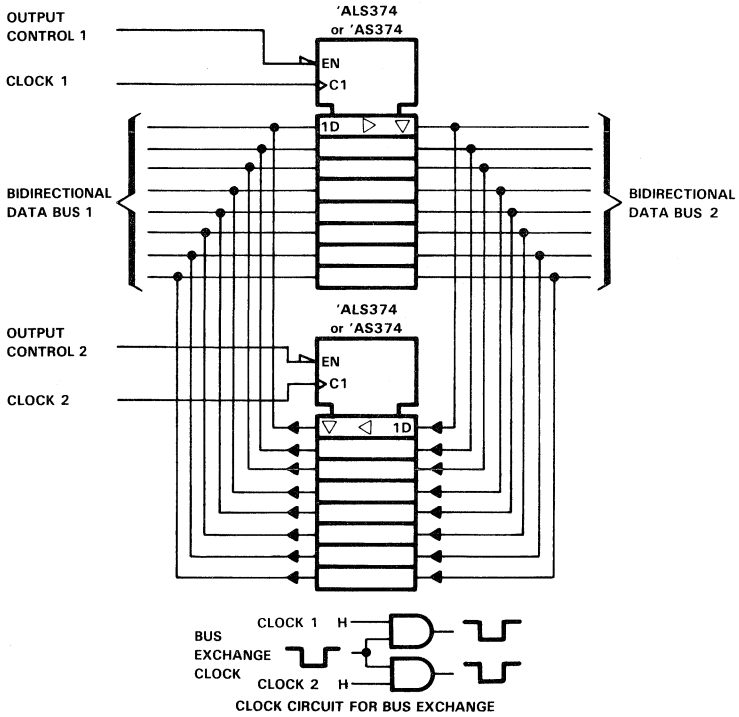
switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS374		SN74AS374		
			MIN	MAX	MIN	MAX	
f_{max}			100		125		MHz
t_{PLH}	CLK	Q	3	11	3	8	ns
t_{PHL}			4	11.5	4	9	
t_{PZH}	$\overline{OC}$	Q	2	7	2	6	ns
t_{PZL}			3	11	3	10	
t_{PHZ}	$\overline{OC}$	Q	2	7	2	6	ns
t_{PLZ}			2	7	2	6	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TYPICAL APPLICATION DATA

BIDIRECTIONAL BUS DRIVER

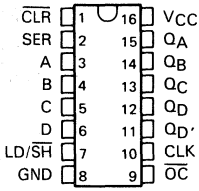


CLOCK CIRCUIT FOR BUS EXCHANGE

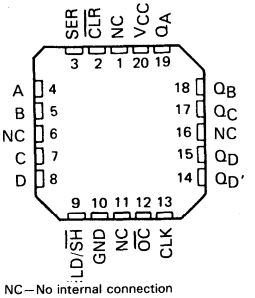
D2661, DECEMBER 1983

- **Cascadable, 4-Bit, Three-State Parallel-to-Serial,Serial-to-Parallel Conversations**
- **Parallel Synchronous Loading**
- **Direct Overriding Clear**
- **Applications:**
  - **N-Bit Serial-to-Parallel Converter**
  - **N-Bit Parallel-to-Serial Converter**
  - **N-Bit Storage Register**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS395 . . . J PACKAGE
SN74AS395 . . . N PACKAGE
SN74AS395 . . . D PACKAGE
(TOP VIEW)



SN54AS395 . . . FH OR FK PACKAGE
SN74AS395 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

These 4-bit registers feature parallel inputs, parallel outputs, cascadable output, and clock, serial load/shift, output control, and direct overriding clear inputs.

Shifting is accomplished when the load/shift control is low. Parallel loading is accomplished by applying the four bits of data and taking the load/shift control input high. The data are loaded into the associated flip-flops and appear at the outputs after the high-to-low transition of the clock input. During parallel loading, the entry of serial data is inhibited.

When the output control is low, the normal logic levels of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently of the level of the clock by a high logic level at the output control input. The outputs then present a high impedance and neither load nor drive the bus line; however, sequential operation of the registers is not affected. During the high-impedance mode, the output at $Q_{D'}$ is still available for cascading.

The SN54AS395 is characterized for operation over the full military range of −55°C to 125°C. The SN74AS395 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS								3-STATE OUTPUTS				CASCADE OUTPUT
CLEAR	LOAD/SHIFT CONTROL	CLOCK	SERIAL	PARALLEL A	PARALLEL B	PARALLEL B	PARALLEL B	Q_A	Q_B	Q_C	Q_D	$Q_{D'}$
L	X	X	X	X	X	X	X	L	L	L	L	L
H	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{D0}
H	H	↓	X	a	b	c	d	a	b	c	d	d
H	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{D0}
H	L	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}
H	L	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}

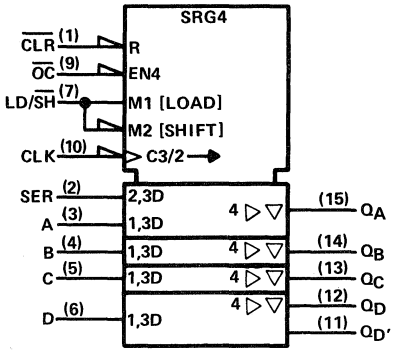
When the output control is high, the 3-state outputs are disabled to the high-impedance state; however, sequential operation of the registers and the output at $Q_{D'}$ are not affected.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

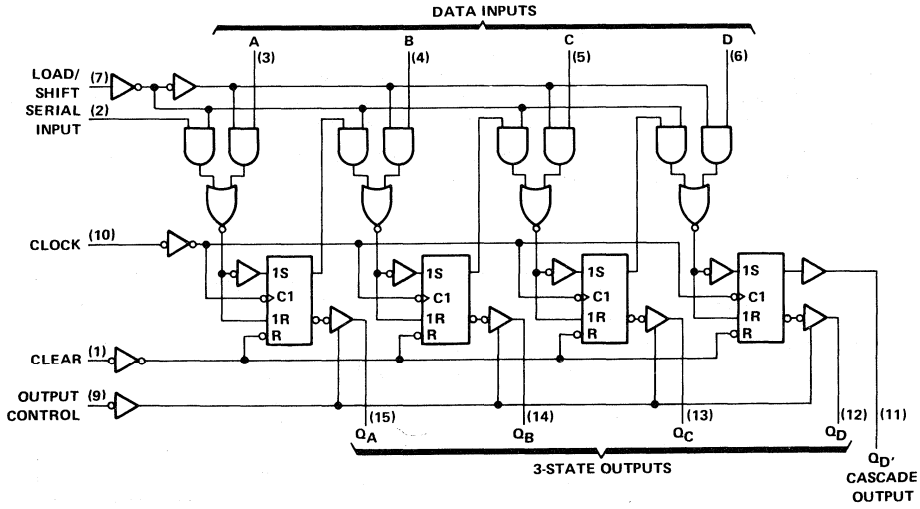
TEXAS INSTRUMENTS

logic symbol



Pin numbers shown are for J and N packages.

logic diagram (positive logic)



Pin numbers shown are for J and N packages.

TYPES SN54ALS465A THRU SN54ALS468A, SN74ALS465A THRU SN74ALS468A
OCTAL BUFFERS WITH 3-STATE OUTPUTS

D2661, APRIL 1982—REVISED DECEMBER 1983

- **Mechanically and Functionally Interchangeable with DM71/81LS97 and DM71/81LS98**
- **P-N-P Inputs Reduce Bus Loading**
- **3-State Outputs Rated at I_{OL} of 12 mA and 24 mA for SN54ALS' and SN74ALS', Respectively**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

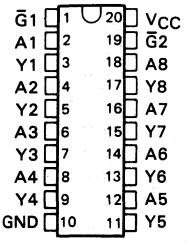
DEVICE	DATA PATH
'ALS465A	True
'ALS466A	Inverting
'ALS467A	True
'ALS468A	Inverting

description

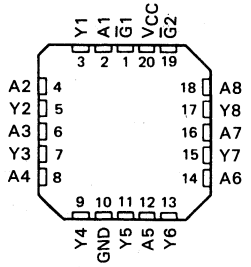
These octal buffers utilize the latest advanced low-power Schottky technology. The 'ALS465A and 'ALS466A have a two-input active-low AND enable gate controlling all eight data buffers. The 'ALS467A and 'ALS468A have two separate active-low enable inputs each controlling four data buffers. In each case, a high level on any $\overline{G}$ places the affected outputs at high impedance.

The SN54ALS465A, SN54ALS466A, SN54ALS467A, and SN54ALS468A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS465A, SN74ALS466A, SN74ALS467A, and SN74ALS468A are characterized for operation from 0°C to 70°C.

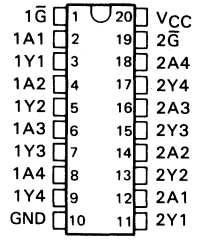
SN54ALS465A, SN54ALS466A . . . J PACKAGE
SN74ALS465A, SN74ALS466A . . . N PACKAGE
SN74ALS465A, SN74ALS466A . . . DW PACKAGE
(TOP VIEW)



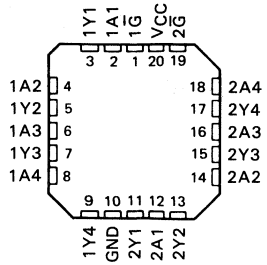
SN54ALS465A, SN54ALS466A . . . FH OR FK PACKAGE
SN74ALS465A, SN74ALS466A . . . FN PACKAGE
(TOP VIEW)



SN54ALS467A, SN54ALS468A . . . J PACKAGE
SN74ALS467A, SN74ALS468A . . . N PACKAGE
SN74ALS467A, SN74ALS468A . . . DW PACKAGE
(TOP VIEW)

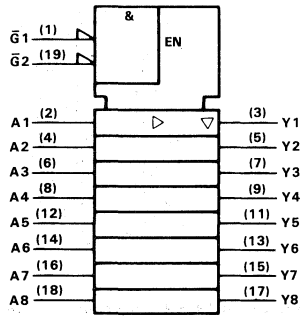


SN54ALS467A, SN54ALS468A . . . FH OR FK PACKAGE
SN74ALS467A, SN74ALS468A . . . FN PACKAGE
(TOP VIEW)

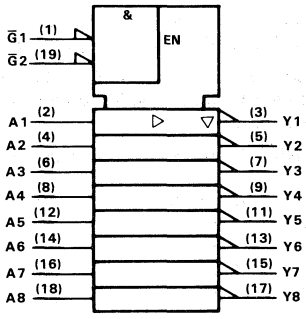


logic symbols

'ALS465A

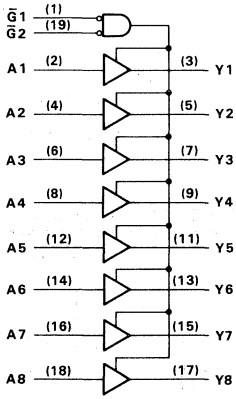


'ALS466A

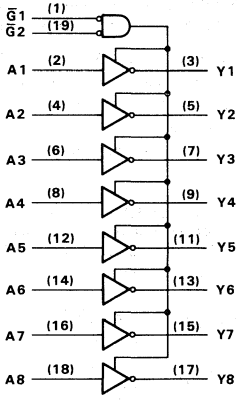


logic diagrams (positive logic)

'ALS465A



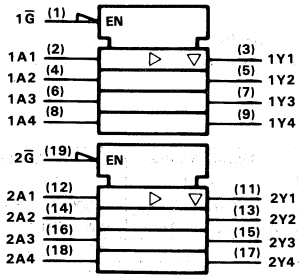
'ALS466A



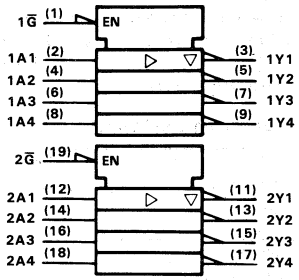
Pin numbers shown are for J and N packages.

logic symbols

'ALS467A

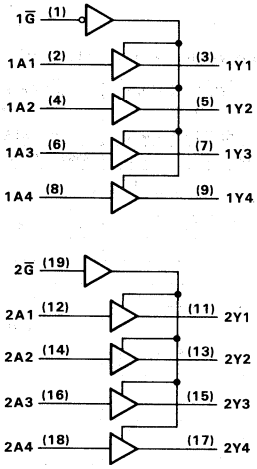


'ALS468A

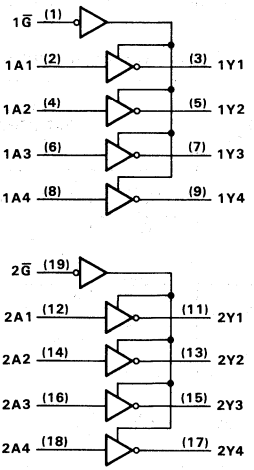


logic diagrams (positive logic)

'ALS467A



'ALS468A



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS465A THRU SN54ALS468A . . . . . −55°C to 125°C
SN74ALS465A THRU SN74ALS468A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS465A THRU SN54ALS468A			SN74ALS465A THRU SN74ALS468A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limit applies only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48 mA limit applies for SN74ALS465A-1, SN74ALS466A-1, SN74ALS467A-1, and SN74ALS468A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS465A THRU SN54ALS468A			SN74ALS465A THRU SN74ALS468A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS465A 'ALS467A	V_{CC} = 5.5 V	Outputs high		11	21		11	16	mA
			Outputs low		19	33		19	28	
			Outputs disabled		23	38		23	33	
	'ALS466A 'ALS468A	V_{CC} = 5.5 V	Outputs high		7	15		7	10	mA
			Outputs low		16	29		16	24	
			Outputs disabled		19	32		19	27	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS465A, 'ALS467A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS465A SN54ALS467A		SN74ALS465A SN74ALS467A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	2	16	2	13	ns
t_{PHL}			4	15	4	12	
t_{PZH}	$\overline{G}$	Any Y	4	27	4	23	ns
t_{PZL}			5	30	5	25	
t_{PHZ}	$\overline{G}$	Any Y	2	12	2	10	ns
t_{PLZ}			3	21	3	18	

'ALS466A, 'ALS468A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS466A SN54ALS468A		SN74ALS466A SN74ALS468A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	14	3	12	ns
t_{PHL}			2	11	2	9	
t_{PZH}	$\overline{G}$	Any Y	4	21	4	16	ns
t_{PZL}			7	25	7	23	
t_{PHZ}	$\overline{G}$	Any Y	2	12	2	10	ns
t_{PLZ}			2	20	2	17	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TYPES SN54ALS518 THRU SN54ALS522, SN74ALS518 THRU SN74ALS522
8-BIT IDENTITY COMPARATORS

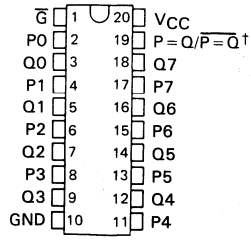
D2661, JUNE 1982—REVISED DECEMBER 1983

- **Compares Two 8-Bit Words**
- **Choice of Totem-Pole or Open-Collector Outputs**
- **'ALS518, 'ALS520, and 'ALS522 Have 20-kΩ Pull-up Resistors on Q Inputs**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

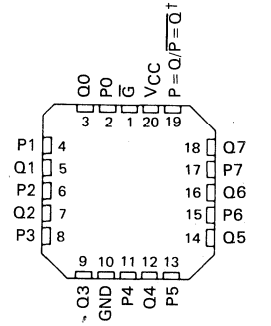
TYPE	INPUT PULL-UP RESISTOR	OUTPUT FUNCTION AND CONFIGURATION
'ALS518	Yes	P = Q open-collector
'ALS519	No	P = Q open-collector
'ALS520	Yes	$\overline{P=Q}$ totem-pole
'ALS521†	No	$\overline{P=Q}$ totem-pole
'ALS522	Yes	$\overline{P=Q}$ open-collector

†'ALS521 is identical to 'ALS688

SN54ALS' . . . J PACKAGE
SN74ALS' . . . N PACKAGE
SN74ALS' . . . DW PACKAGE
(TOP VIEW)



SN54ALS' . . . FH OR FK PACKAGE
SN74ALS' . . . FN PACKAGE
(TOP VIEW)



†P = Q for 'ALS518 and 'ALS519, and $\overline{P=Q}$ for 'ALS520, 'ALS521, and 'ALS522.

description

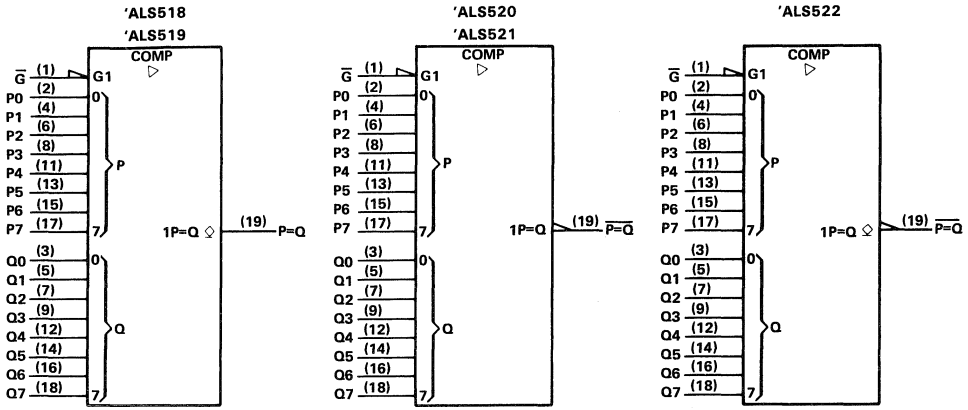
These identity comparators perfrom comparisons on two eight-bit binary or BCD words. The 'ALS518 and 'ALS519 provide P = Q outputs, while the 'ALS520, 'ALS521, and 'ALS522 provide $\overline{P=Q}$ outputs. The 'ALS518, 'ALS519, and 'ALS522 have open-collector outputs. The 'ALS518, 'ALS520, and 'ALS522 feature 20-kΩ pull-up termination resistors on the Q inputs for analog or switch data.

The SN54ALS518 through SN54ALS522 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS518 through SN74ALS522 are characterized for operation from 0°C to 70°C.

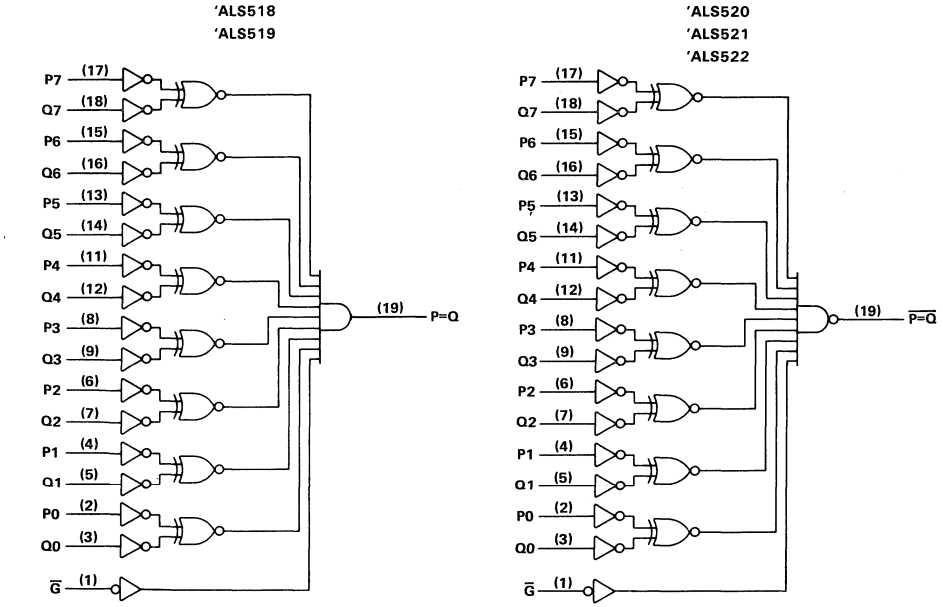
FUNCTION TABLE

INPUTS		OUTPUTS	
DATA P, Q	ENABLE G	P = Q	$\overline{P=Q}$
P = Q	L	H	L
P > Q	L	L	H
P < Q	L	L	H
X	H	L	H

logic symbols



logic diagrams (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: Q inputs of 'ALS518, 'ALS522 . . . . . V_{CC} + 0.5 V or 5.5 V, whichever is less
All other inputs . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS518, SN54ALS519, SN54ALS522 . . . . . −55°C to 125°C
SN74ALS518, SN74ALS519, SN74ALS522 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

2

recommended operating conditions

		SN54ALS518 SN54ALS519 SN54ALS522			SN74ALS518 SN74ALS519 SN74ALS522			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS518 SN54ALS519 SN54ALS522			SN74ALS518 SN74ALS519 SN74ALS522			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	'ALS518, 'ALS522 Q inputs	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
	All other inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	
I_{IH}	'ALS518, 'ALS522 Q inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			−0.2			−0.2	mA
	All other inputs					20			20	μA
I_{IL}	'ALS518, 'ALS522 Q inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.6			−0.6	mA
	All other inputs					−0.1			−0.1	
I_{CC}	'ALS518	V_{CC} = 5.5 V,	See Note 1		11	17		11	17	mA
	'ALS519				11	17		11	17	
	'ALS522				11	17		11	17	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: I_{CC} is measured with $\overline{G}$ grounded, P and Q at 4.5 V.

'ALS518, 'ALS519 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS518 SN54ALS519		SN74ALS518 SN74ALS519		
			MIN	MAX	MIN	MAX	
t_{PLH}	P or Q	P=Q	15	37	15	33	ns
t_{PHL}			3	18	3	15	
t_{PLH}	$\overline{G}$	P=Q	15	37	15	33	ns
t_{PHL}			3	18	3	15	

'ALS522 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS522		SN74ALS522		
			MIN	MAX	MIN	MAX	
t_{PLH}	P or Q	$\overline{P=Q}$	10	30	10	25	ns
t_{PHL}			5	25	5	23	
t_{PLH}	$\overline{G}$	$\overline{P=Q}$	8	30	8	25	ns
t_{PHL}			8	30	8	23	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: Q inputs of 'ALS520 . . . . . V_{CC} + 0.5 V or 5.5 V, whichever is less
All other inputs . . . . . 7 V
Operating free-air temperature range: SN54ALS520, SN54ALS521 . . . . . −55°C to 125°C
SN74ALS520, SN74ALS521 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS520 SN54ALS521			SN74ALS520 SN74ALS521			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS520 SN54ALS521			SN74ALS520 SN74ALS521			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_I	'ALS520 Q inputs	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
	All other inputs	V_{CC} = 5.5 V	V_I = 7 V			0.1			0.1	
I_{IH}	'ALS520 Q inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			−0.2			−0.2	mA
	All other inputs					20			20	μA
I_{IL}	'ALS520 Q inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.6			−0.6	mA
	All other inputs					−0.1			−0.1	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS520	V_{CC} = 5.5 V,	See Note 1		12	19		12	19	mA
	'ALS521				12	19		12	19	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with $\overline{G}$ grounded and P and Q inputs at 4.5 V.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS520 SN54ALS521		SN74ALS520 SN74ALS521		
			MIN	MAX	MIN	MAX	
t_{PLH}	P or Q	$\overline{P=Q}$	3	16	3	12	ns
t_{PHL}			5	25	5	20	
t_{PLH}	$\overline{G}$	$\overline{P=Q}$	2	15	2	12	ns
t_{PHL}			5	23	5	22	

NOTE 1. For load circuit and voltage waveforms, see page 1-12.

- Can Be Programmed and Verified on Most Incoming Test Equipment
- Reduces Board and Package Size for Similar Fixed Comparator Functions
- High-Speed Address Recognition
- Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

Programming Capabilities

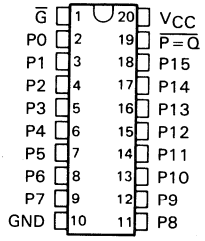
'ALS526 — Fuse Programmable 16-Bit Identity Comparator

'ALS527 — Fuse Programmable 8-Bit Identity Comparator and 4-Bit Comparator

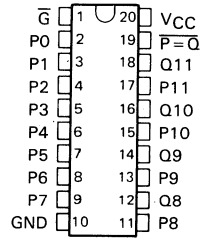
'ALS528 — Fuse Programmable 12-Bit Identity Comparator

2

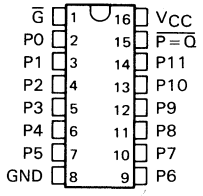
SN54ALS526 . . . J PACKAGE
SN74ALS526 . . . N PACKAGE
SN74ALS526 . . . DW PACKAGE
(TOP VIEW)



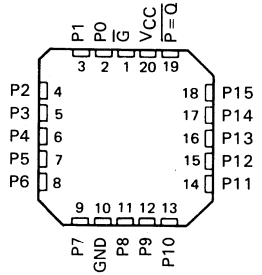
SN54ALS527 . . . J PACKAGE
SN74ALS527 . . . N PACKAGE
SN74ALS527 . . . DW PACKAGE
(TOP VIEW)



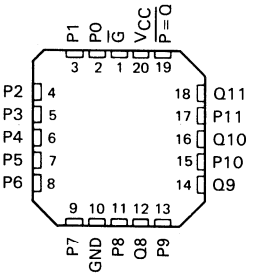
SN54ALS528 . . . J PACKAGE
SN74ALS528 . . . N PACKAGE
SN74ALS528 . . . D PACKAGE
(TOP VIEW)



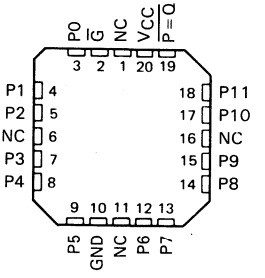
SN54ALS526 . . . FH OR FK PACKAGE
SN74ALS526 . . . FN PACKAGE
(TOP VIEW)



SN54ALS527 . . . FH OR FK PACKAGE
SN74ALS527 . . . FN PACKAGE
(TOP VIEW)



SN54ALS528 . . . FH OR FK PACKAGE
SN74ALS528 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

The 'ALS526 and 'ALS528 are fuse-programmable identity comparators designed for easy programming in fixed-comparator applications. The 'ALS526 compares a 16-bit data word against a preprogrammed 16-bit data word while the 'ALS528 compares a 12-bit data word against a preprogrammed 12-bit data word. The $\overline{P=Q}$ output will go low when the applied data word (P inputs) matches the preprogrammed data word (Q represents the preprogrammed data word). Programming is easily accomplished on the bench or with conventional automatic test equipment. Special equipment such as PROM-programmers are not required.

The 'ALS527 is a combination of an 8-bit fuse-programmable comparator and a conventional 4-bit comparator. For the $\overline{P=Q}$ output to go low, the applied data word P0 through P7 must match the preprogrammed data word Q0 through Q7, and the applied data word P8 through P11 must match the applied data word Q8 through Q11.

The SN54ALS526, SN54ALS527, and SN54ALS528 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS526, SN74ALS527, and SN74ALS528 are characterized for operation from 0°C to 70°C.

programming details

Before any fuses are blown, the inputs are programmed to recognize a low logic level. Therefore, only the bits that are to be programmed to recognize a high logic level require a fuse to be blown. A fuse is easily blown by applying 12 volts (V_{IHH}) to the desired P input pin and also to the $\overline{G}$ input. This permanently programs the pin to recognize a high. Only one input pin should be programmed at a time.

verification details

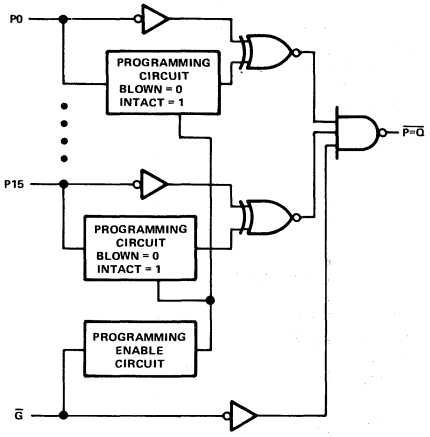
Before the device is programmed, all of the fuses are intact. In this condition, the $\overline{P=Q}$ output should go low only if lows are applied to all the P inputs. On the 'ALS527, the same is true for the P0 and P7 inputs, but in addition, the P8 through P11 inputs must match the Q8 through Q11 inputs.

It is possible to check the fuse circuitry before actually blowing it in the following manner. By placing a high (V_{IH}) at the desired P input pin while leaving a low on the $\overline{G}$ input, the $\overline{P=Q}$ output should be high. If the P input is then taken to V_{IHH}, the $\overline{P=Q}$ output should go low assuming all other P inputs are at a high level (V_{IH}).

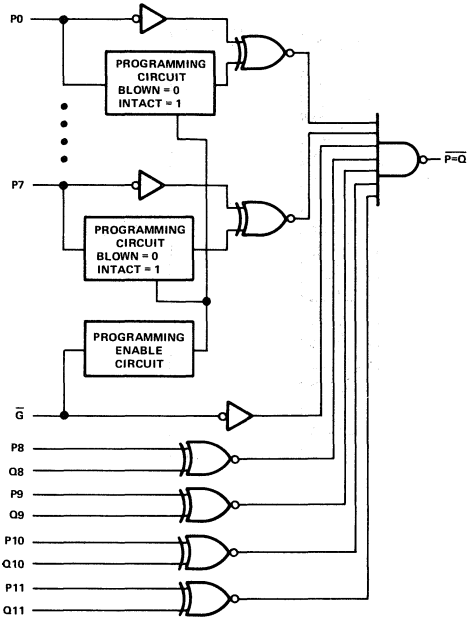
In this condition, the fuse will not be blown as long as $\overline{G}$ is at V_{IL}. When $\overline{G}$ is taken to V_{IHH}, the fuse will be blown and the input will be permanently programmed to recognize a high logic level. The timing diagram in Figure 1 shows the recommended programming sequence. After all desired input pins have been programmed, it is easy to verify the device by applying the programmed data word and checking to be sure that the $\overline{P=Q}$ output is low.

logic diagrams (positive logic)

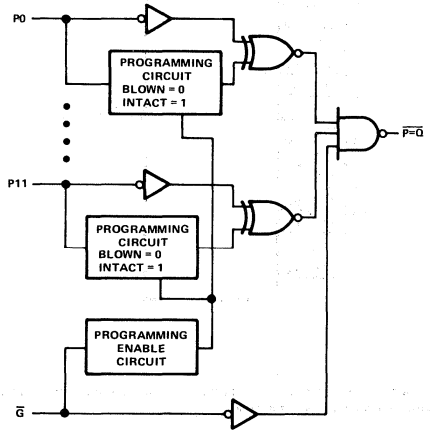
'ALS526



'ALS527



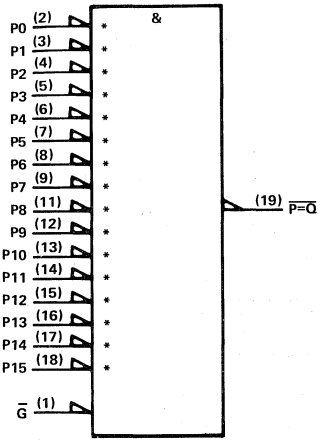
'ALS528



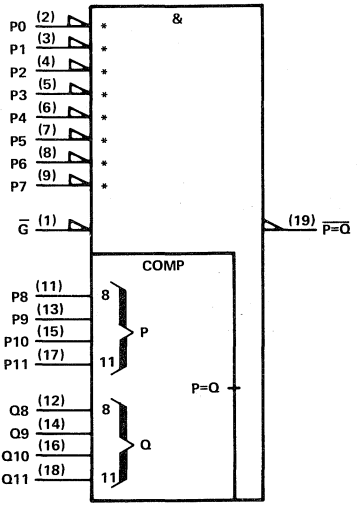
Pin numbers shown are for J and N packages.

logic symbols

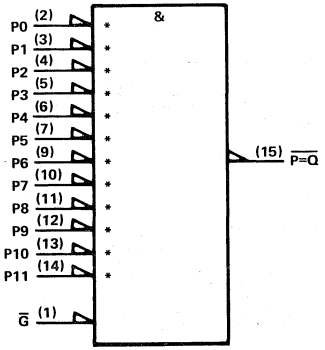
'ALS526



'ALS527



'ALS528



*These inputs can be programmed to be active high. The asterisk is not a part of the symbol. For a correct symbol for the programmed device, delete the polarity symbol ( ) at any input whose programming fuse has been blown.

Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: SN54ALS' . . . . . −55°C to 125°C
SN74ALS' . . . . . 0°CC to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

		SN54ALS'			SN74ALS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		5.5	2		5.5	V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS'			SN74ALS'			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	2.9		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.36	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_{IL} = 0.4 V			−0.2			−0.2	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−130	−30		−130	mA
I_{CC}	'ALS526	V_{CC} = 5.5 V, All inputs at 4.5 V			16	27		16	27	mA
	'ALS527				15	24		15	24	
	'ALS528				13	21		13	21	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximtes one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 2)

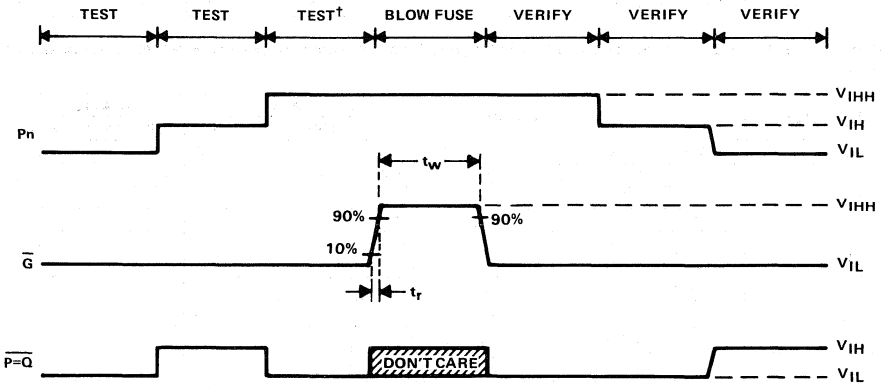
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS'		SN74ALS'		
			MIN	MAX	MIN	MAX	
t_{PLH}	P or Q	$\overline{P=Q}$	3	18	3	15	ns
t_{PHL}			2	15	2	12	
t_{PLH}	$\overline{G}$	$\overline{P=Q}$	2	18	2	15	ns
t_{PHL}			2	15	2	12	

NOTE 2: For load circuit and voltage waveforms, see page 1-12

programming parameters

PARAMETER			MIN	MAX	UNIT
V_{IH}	High-level input voltage		2	5.5	V
V_{IL}	Low-level input voltage			0.8	V
V_{IHH}	Program-pulse input voltage		11.5	12.5	V
V_{CC}	Supply voltage		6.5	7.5	V
I_{IHH}	Program-pulse input current	Pn ($\overline{G}$ low)		10	mA
		$\overline{G}$		1.24	
I_{CCHH}	Supply current with V_{IHH} applied	'ALS526		31	mA
		'ALS527		29	
		'ALS528		26	
t_w	Pulse duration, program		10	50	μs
t_r	Rise time, program voltage			10	μs

programming waveforms



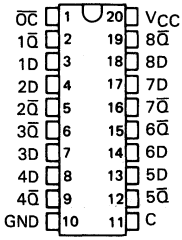
†This test is only true if all other P inputs are at V_{IH}.

TYPES SN54ALS533, SN54AS533, SN74ALS533, SN74AS533
OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

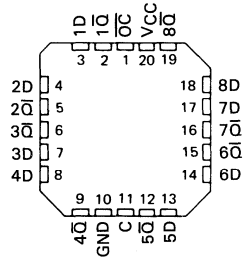
D2661, APRIL 1982—REVISED DECEMBER 1983

- **8-Latches In a Single Package**
- **3-State Bus-Driving Inverting Outputs**
- **Full Parallel Access for Loading**
- **Buffered Control Inputs**
- **P-N-P Inputs Reduce D-C Loading on Data Lines**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS533, SN54AS533 . . . J PACKAGE
SN74ALS533, SN74AS533 . . . N PACKAGE
SN74ALS533, SN74AS533 . . . DW PACKAGE
(TOP VIEW)



SN54ALS533, SN54AS533 . . . FH OR FK PACKAGE
SN74ALS533, SN74AS533 . . . FN PACKAGE
(TOP VIEW)



description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'ALS533 and 'AS533 are transparent D-type latches. While the enable (C) is high, the $\overline{Q}$ outputs will follow the complements of the D inputs. When the enable is taken low, the $\overline{Q}$ outputs will be latched at the inverses of the levels that were set up at the D inputs. The 'ALS533 and 'AS533 are functionally equivalent to the 'ALS373 and 'AS373 except for having inverted outputs.

A buffered output-control ($\overline{OC}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

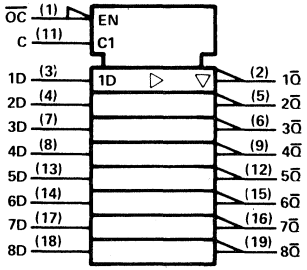
The output control does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN54ALS533 and SN54AS533 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS533 and SN74AS533 are characterized for operation from 0°C to 70°C.

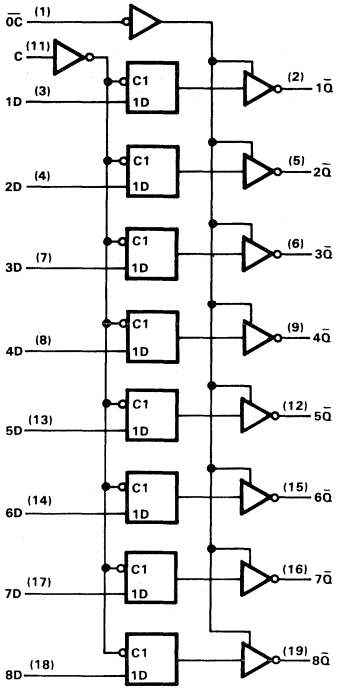
FUNCTION TABLE (EACH LATCH)

INPUTS			OUTPUT
$\overline{OC}$	ENABLE C	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

logic symbol



logic diagram (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS533, SN54AS533 . . . . . −55 °C to 125 °C
SN74ALS533, SN74AS533 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS533			SN74ALS533			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
t_w	Pulse duration, enable C high	15			15			ns
t_{su}	Setup time, data before enable C↓	15			15			ns
t_h	Hold time, data after enable C↓	7			7			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS533			SN74ALS533			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		10	17		10	17	mA
		Outputs low		17	26		17	26	
		Outputs disabled		18.5	28		18.5	28	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

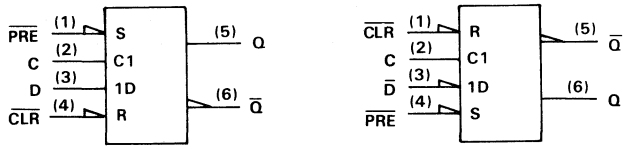
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS533		SN74ALS533		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$	4	24	4	19	ns
t_{PHL}			4	14	4	13	
t_{PLH}	C	Any $\overline{Q}$	5	28	5	23	ns
t_{PHL}			4	21	4	18	
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$	4	19	4	17	ns
t_{PZL}			4	20	4	18	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$	2	12	2	10	ns
t_{PLZ}			3	22	3	16	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D latch signal conventions

It is TI practice to name the outputs and other inputs of a D-type latch and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active low.

In some applications it may be advantageous to redesignate the data input $\overline{D}$. In that case all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.



Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (⊵) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 ($\overline{Q}$) is still in phase with the data input $\overline{D}$, but now both are considered active-low.

recommended operating conditions

		SN54AS533			SN74AS533			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			32			48	mA
t_w	Pulse duration, enable C high	3			2			ns
t_{su}	Setup time, data before enable C↓	2			2			ns
t_h	Hold time, data after enable C↓	3			3			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS533			SN74AS533			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.29	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.34	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−50			50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V		−0.02	−0.5		−0.02	−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		62	100		62	100	mA
		Outputs low		64	100		64	100	
		Outputs disabled		71	110		71	110	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS533		SN74AS533		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$	4	10	4	7.5	ns
t_{PHL}			4	8	4	7	
t_{PLH}	C	Any $\overline{Q}$	5	11	5	9	ns
t_{PHL}			4.5	8.5	4.5	8	
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$	2	7.5	2	6.5	ns
t_{PZL}			4.5	10.5	4.5	9.5	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$	3	7.5	3	6.5	ns
t_{PLZ}			3	8	3	7	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TYPES SN54ALS534, SN54AS534, SN74ALS534, SN74AS534
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

D2661, APRIL 1982—REVISED DECEMBER 1983

- **3-State Bus-Driving Inverting Outputs**
- **Buffered Control Inputs**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

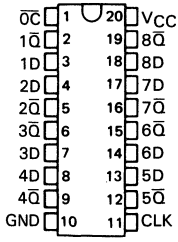
The eight flip-flops of the 'ALS534 and 'AS534 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the complement of the logic states that were set up at the D inputs. The 'ALS534 and 'AS534 are functionally equivalent to the 'ALS374 and 'AS374 except for having inverted outputs.

A buffered output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

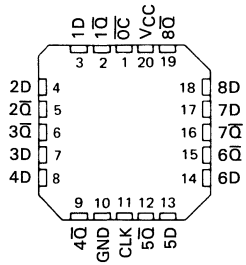
The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN54ALS534 and SN54AS534 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS534 and SN74AS534 are characterized for operation from 0°C to 70°C.

SN54ALS534, SN54AS534 . . . J PACKAGE
SN74ALS534, SN74AS534 . . . N PACKAGE
SN74ALS534, SN74AS534 . . . DW PACKAGE
(TOP VIEW)



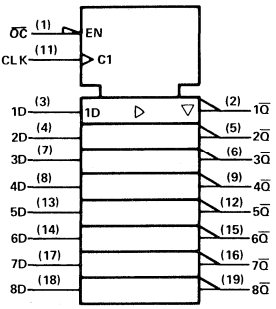
SN54ALS534, SN54AS534 . . . FH OR FK PACKAGE
SN74ALS534, SN74AS534 . . . FN PACKAGE
(TOP VIEW)



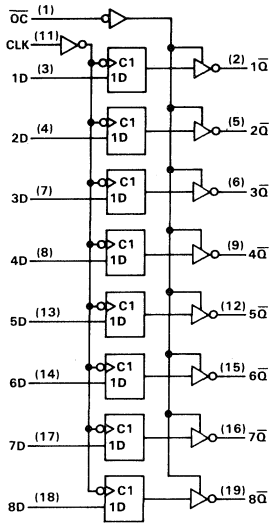
FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

logic symbol



logic diagram (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS534, SN54AS534 . . . . . −55 °C to 125 °C
SN74ALS534, SN74AS534 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54ALS534			SN74ALS534			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency		0		30	0		35	MHz
t_w	Pulse duration	CLK high	16.5			14			ns
		CLK low	16.5			14			
t_{su}	Setup time, data before CLK↑		10			10			ns
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS534			SN74ALS534			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	CLK, $\overline{OC}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	D					−0.2			−0.2	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		11	19		11	19	mA
			Outputs low		19	28		19	28	
			Outputs disabled		10	31		20	31	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

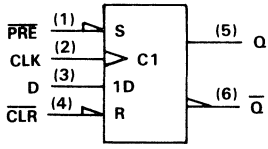
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS534		SN74ALS534		
			MIN	MAX	MIN	MAX	
f_{max}			30		35		MHz
t_{PLH}	CLK	Any $\overline{Q}$	3	15	3	12	ns
t_{PHL}			5	18	5	16	
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$	5	19	5	17	ns
t_{PZL}			7	20	7	18	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$	2	12	2	10	ns
t_{PLZ}			2	16	2	14	

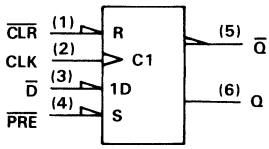
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D flip-flop signal conventions

It is TI practice to name the outputs and other inputs of a D-type flip-flop and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active low.

In some applications it may be advantageous to redesignate the data input $\overline{D}$. In that case all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.





Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (▷) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 ($\overline{Q}$) is still in phase with the data input $\overline{D}$, but now both are considered active-low.

recommended operating conditions

			SN54AS534			SN74AS534			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				32			48	mA
f_{clock}	Clock frequency		0		100	0		125	MHz
t_w	Pulse duration	CLK high	5.5			4			ns
		CLK low	5			3			
t_{su}	Setup time, data before CLK↑		3			2			ns
t_h	Hold time, data after CLK↑		3			2			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS534			SN74AS534			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.29	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.34	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	$\overline{OC}$, CLK	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	D					−3			−2	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC} mA		V_{CC} = 5.5 V	Outputs high		77	120		77	120	mA
			Outputs low		84	128		84	128	
			Outputs disabled		84	128		84	128	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS534		SN74AS534		
			MIN	MAX	MIN	MAX	
f_{max}			100		125		MHz
t_{PLH}	CLK	Any $\overline{Q}$	3	11	3	8	ns
t_{PHL}			4	11.5	4	9	
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$	2	7	2	6	ns
t_{PZL}			3	11	3	10	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$	2	7	2	6	ns
t_{PLZ}			2	7	2	6	

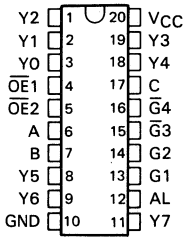
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TYPES SN54ALS538, SN74ALS538
3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS WITH 3-STATE OUTPUTS

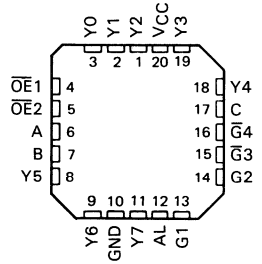
D2661, APRIL 1982—REVISED DECEMBER 1983

- **3-State Outputs**
- **Output Polarity Control**
- **Data Multiplexing Capability**
- **Multiple Enables for Expansion**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS538 . . . J PACKAGE
SN74ALS538 . . . N PACKAGE
SN74ALS538 . . . DW PACKAGE
(TOP VIEW)



SN54ALS538 . . . FH OR FK PACKAGE
SN74ALS538 . . . FN PACKAGE
(TOP VIEW)



description

The 'ALS538 decoder/demultiplexer accepts three address input signals (A, B, C) and decodes them to select one-of-eight mutually exclusive outputs. If the polarity control input (AL) is high, the outputs are active-low; if AL is low, the outputs are active-high. Two active-high and two active-low input enables are available for easy expansion to 1-of-32 decoding with four packages, or for data demultiplexing to 1-of-8 or 1-of-16 destinations. A high signal on either of the output enables ($\overline{OE}1$ and $\overline{OE}2$) forces all outputs to the high-impedance state.

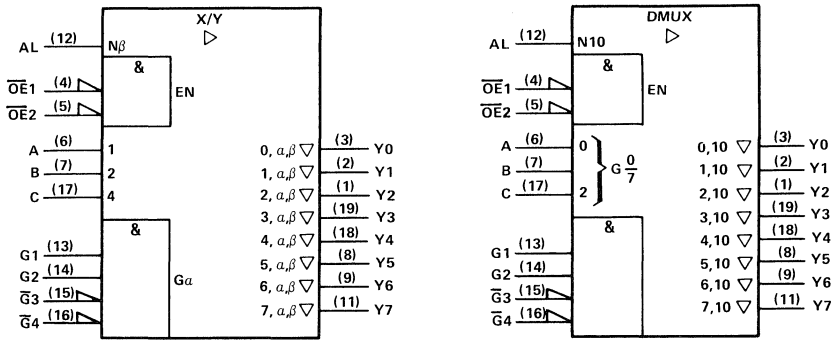
The SN54ALS538 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS538 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH DECODER/DEMULTIPLEXER)

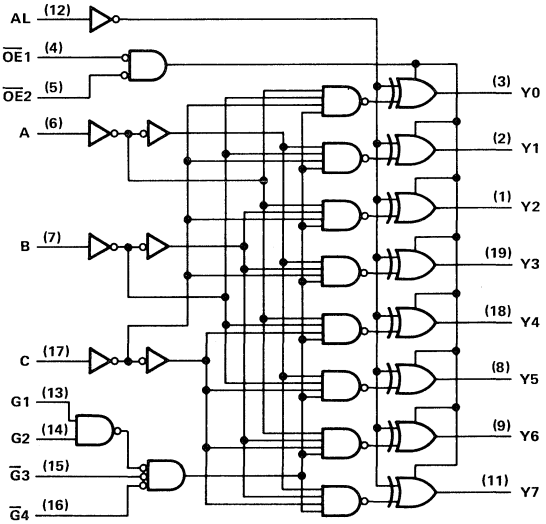
FUNCTION	INPUTS									OUTPUTS							
	$\overline{OE}1$	$\overline{OE}2$	G1	G2	$\overline{G}3$	$\overline{G}4$	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
High impedance	H	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
(AL = X)	X	H	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
	L	L	L	X	X	X	X	X	X								
Disable	L	L	X	L	X	X	X	X	X								
(AL = X)	L	L	X	X	H	X	X	X	X	All outputs same level as AL							
	L	L	X	X	X	H	X	X	X								
	L	L	H	H	L	L	L	L	L	H	L	L	L	L	L	L	L
	L	L	H	H	L	L	L	L	H	L	H	L	L	L	L	L	L
	L	L	H	H	L	L	L	H	L	L	L	H	L	L	L	L	L
Active-High	L	L	H	H	L	L	L	H	H	L	L	L	H	L	L	L	L
Output																	
(AL = L)	L	L	H	H	L	L	H	L	L	L	L	L	L	H	L	L	L
	L	L	H	H	L	L	H	L	H	L	L	L	L	L	H	L	L
	L	L	H	H	L	L	H	H	L	L	L	L	L	L	L	H	L
	L	L	H	H	L	L	H	H	H	L	L	L	L	L	L	L	H
	L	L	H	H	L	L	L	L	L	L	H	H	H	H	H	H	H
	L	L	H	H	L	L	L	L	H	H	L	H	H	H	H	H	H
	L	L	H	H	L	L	L	H	L	H	H	L	H	H	H	H	H
Active-Low	L	L	H	H	L	L	L	H	H	H	H	H	L	H	H	H	H
Output																	
(AL = H)	L	L	H	H	L	L	H	L	L	H	H	H	H	L	H	H	H
	L	L	H	H	L	L	H	L	H	H	H	H	H	H	L	H	H
	L	L	H	H	L	L	H	H	L	H	H	H	H	H	H	L	H
	L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	L

PRODUCT PREVIEW

logic symbols (alternatives)



logic diagram (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS538 . . . . . −55 °C to 125 °C
SN74ALS538 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS538			SN74ALS538			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS538			SN74ALS538			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	A, B, C or AL	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	All other					−0.1			−0.1	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high							mA
			Outputs low							
			Outputs disabled		25			25		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS538			SN74ALS538			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A, B, C	Any Y		22			22		ns
t_{PHL}				22			22		
t_{PLH}	G1 or G2	Any Y		18			18		ns
t_{PHL}				18			18		
t_{PLH}	$\overline{G}3$ or $\overline{G}4$	Any Y		22			22		ns
t_{PHL}				22			22		
t_{PLH}	AL	Any Y		20			20		ns
t_{PHL}				20			20		
t_{PZH}	$\overline{OE}1$ or $\overline{OE}2$	Any Y		10			10		ns
t_{PZL}				13			13		
t_{PHZ}	$\overline{OE}1$ or $\overline{OE}2$	Any Y		8			8		ns
t_{PLZ}				10			10		

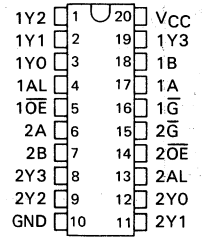
†All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

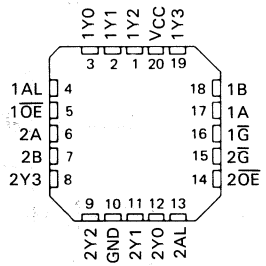
Additional information on these products can be obtained from the factory as it becomes available.

- **3-State Outputs**
- **Output Polarity Control**
- **Data Multiplexing Capability**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS539 . . . J PACKAGE
SN74ALS539 . . . N PACKAGE
SN74ALS539 . . . DW PACKAGE
(TOP VIEW)



SN54ALS539 . . . FH OR FK PACKAGE
SN74ALS539 . . . FN PACKAGE
(TOP VIEW)



description

The 'ALS539 decoder/demultiplexer contains two independent decoders, each of which accepts two address input signals (A and B) and decodes them to select one of four mutually exclusive outputs. If the polarity-control input (AL) is high, the outputs are active-low; if AL is low, the outputs are active-high. An active-low input enable ($\overline{G}$) is available for data demultiplexing. Data is routed to the selected output in noninverting form in the active-low mode or in inverted form in the active-high mode. A high signal on the output enable ($\overline{OE}$) forces the 3-state outputs to the high-impedance state.

The SN54ALS539 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS539 is characterized for operation from 0°C to 70°C.

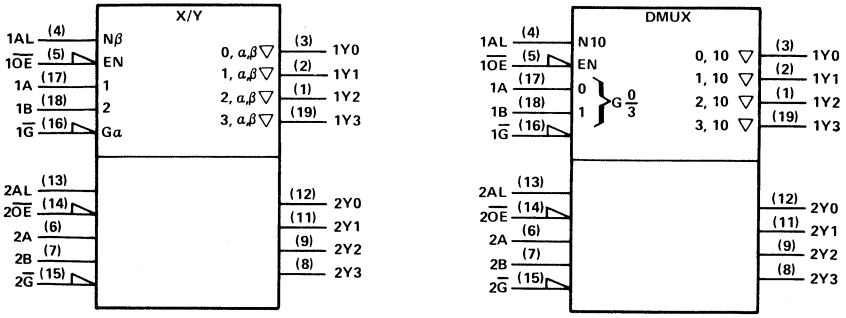
FUNCTION TABLE
(EACH DECODER/DEMULTIPLEXER)

FUNCTION	INPUTS				OUTPUTS			
	$\overline{OE}$	$\overline{G}$	B	A	Y_0	Y_1	Y_2	Y_3
High Impedance	H	X	X	X	Z	Z	Z	Z
Disable	L	H	X	X	All outputs same level as AL			
Active-high Output (AL = L)	L	L	L	L	H	L	L	L
	L	L	L	H	L	H	L	L
	L	L	H	L	L	L	H	L
	L	L	H	H	L	L	L	H
Active-low Output (AL = H)	L	L	L	L	L	H	H	H
	L	L	L	H	H	L	H	H
	L	L	H	L	H	H	L	H
	L	L	H	H	H	H	H	L

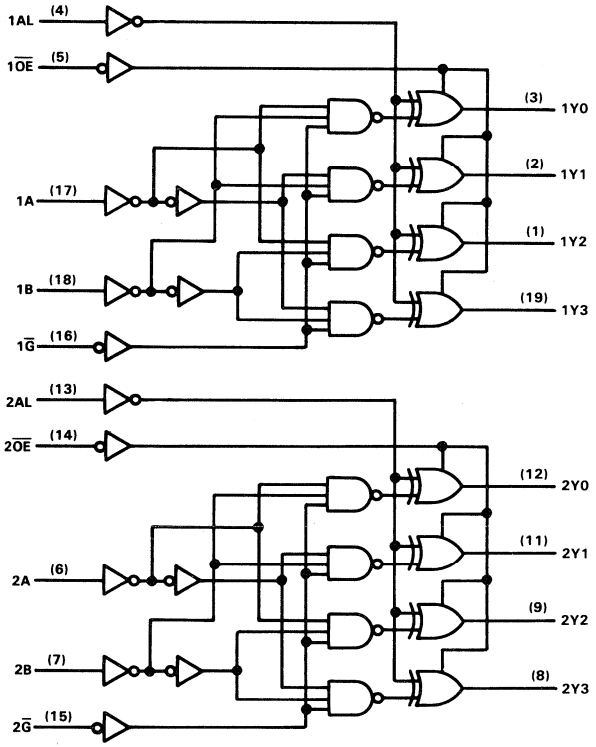
PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

logic symbols (alternatives)



logic diagram (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS539 . . . . . −55 °C to 125 °C
SN74ALS539 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS539			SN74ALS539			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS539			SN74ALS539			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	A, B, C or AL	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	All other					−0.1			−0.1	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high							mA
			Outputs low							
			Outputs disabled		24			24		

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS539			SN74ALS539			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A or B	Y		22			22		ns
t_{PHL}				22			22		
t_{PLH}	$\overline{G}$	Y		18			18		ns
t_{PHL}				18			18		
t_{PLH}	AL	Y		22			22		ns
t_{PHL}				22			22		
t_{PZH}	$\overline{OE}$	Y		10			10		ns
t_{PZL}				13			13		
t_{PHZ}	$\overline{OE}$	Y		8			8		ns
t_{PLZ}				10			10		

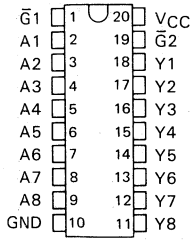
†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

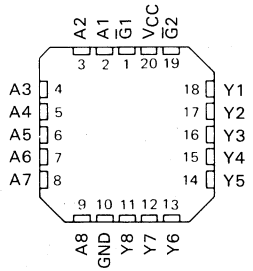
D2661, APRIL 1982 – REVISED DECEMBER 1984

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Data Flow-Thru Pinout (All Inputs on Opposite Side from Outputs)
- Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS540, SN54ALS541 . . . J PACKAGE
SN74ALS540, SN74ALS541 . . . N PACKAGE
SN74ALS540, SN74ALS541 . . . DW PACKAGE
(TOP VIEW)



SN54ALS540, SN54ALS541 . . . FH OR FK PACKAGE
SN74ALS540, SN74ALS541 . . . FN PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed to have the performance of the popular SN54ALS240/SN74ALS240 series and, at the same time, offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout.

The three-state control gate is a 2-input NOR such that if either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high-impedance state.

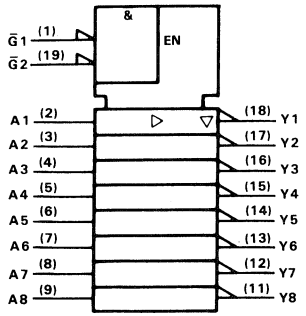
The 'ALS540 provides inverted data and the 'ALS541 provides true data at the outputs.

The -1 versions of the SN74ALS540 and SN74ALS541 parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS540 and SN54ALS541.

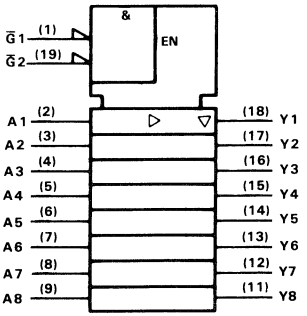
The SN54ALS540 and SN54ALS541 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS540 and SN74ALS541 are characterized for operation from 0°C to 70°C.

logic symbols

'ALS540



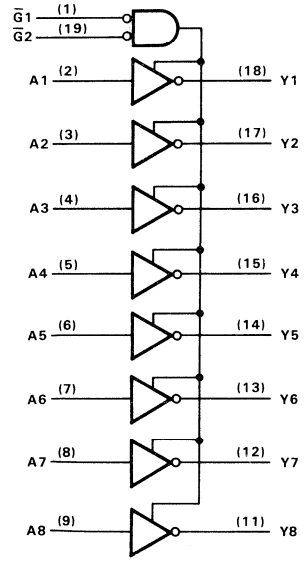
'ALS541



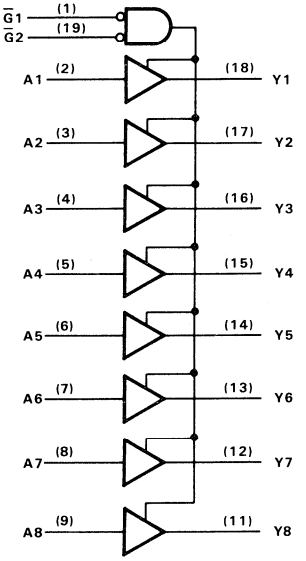
Pin numbers shown are for J and N packages

logic diagrams (positive logic)

'ALS540



'ALS541



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS540, SN54ALS541 . . . . . −55°C to 125°C
SN74ALS540, SN74ALS541 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS540 SN54ALS541			SN74ALS540 SN74ALS541			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limit applies only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48 mA limit applies for the SN74ALS540-1 and SN74ALS541-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS540 SN54ALS541			SN74ALS540 SN74ALS541			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA¶					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS540	V_{CC} = 5.5 V	Outputs high		5	10		5	10	mA
			Outputs low		13	22		13	22	
			Outputs disabled		11	19		11	19	
	'ALS541	V_{CC} = 5.5 V	Outputs high		6	14		6	14	mA
			Outputs low		15	25		15	25	
			Outputs disabled		13.5	22		13.5	22	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
¶ I_{OL} = 48 mA for −1 versions.

'ALS540 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54/74ALS540			SN54ALS540		SN74ALS540		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y		7.5	10	2	14	2	12	ns
t_{PHL}				5.6	8	2	11	2	9	
t_{PZH}	$\overline{G}$	Y		9	12	5	18	5	15	ns
t_{PZL}				12.5	16	8	24	8	20	
t_{PHZ}	$\overline{G}$	Y		4	6	1	12	1	10	ns
t_{PLZ}				7	9	2	14	2	12	

'ALS541 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54/74ALS541			SN54ALS541		SN74ALS541		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y		8.7	11	4	17	4	14	ns
t_{PHL}				7	9	2	12	2	10	
t_{PZH}	$\overline{G}$	Y		9	12	5	18	5	15	ns
t_{PZL}				12.5	16	8	24	8	20	
t_{PHZ}	$\overline{G}$	Y		4	6	1	12	1	10	ns
t_{PLZ}				7	9	2	14	2	12	

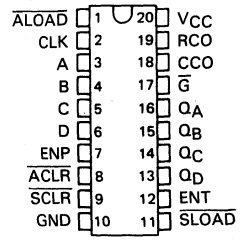
NOTE 1: For load circuit and voltage waveforms, see page 1-12

TYPES SN54ALS560A, SN54ALS561A, SN74ALS560A, SN74ALS561A
SYNCHRONOUS 4-BIT COUNTERS WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982—REVISED DECEMBER 1983

- **Carry Output for n-Bit Cascading**
- **Buffer-Type Outputs Drive Bus Lines Directly**
- **Choice of Asynchronous or Synchronous Load or Clear**
- **Internal Look-Ahead for Fast Cascading**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS560A, SN54ALS561A . . . J PACKAGE
SN74ALS560A, SN74ALS561A . . . N PACKAGE
SN74ALS560A, SN74ALS561A . . . DW PACKAGE
(TOP VIEW)



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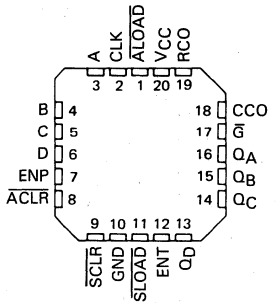
SN54ALS560A, SN54ALS561A . . . FH OR FK PACKAGE
SN74ALS560A, SN74ALS561A . . . FN PACKAGE
(TOP VIEW)



description

The 'ALS560A decade counters and 'ALS561A binary counters are programmable and offer synchronous and asynchronous clearing as well as synchronous and asynchronous loading. All synchronous functions are executed on the positive-going edge of the clock.

The clear function is initiated by applying a low level to either Asynchronous Clear ($\overline{ACLR}$) or Synchronous Clear ($\overline{SCLR}$). Asynchronous (direct) clearing overrides all other functions of the device, while synchronous clearing overrides only the other synchronous functions. Data is loaded from the A, B, C, and D inputs by applying a low level to Asynchronous Load ($\overline{ALOAD}$) or by the combination of a low level at Synchronous Load ($\overline{SLOAD}$) and a positive-going clock transition. The counting function is enabled only when Enable P (ENP), Enable T (ENT), $\overline{ACLR}$, $\overline{ALOAD}$, $\overline{SCLR}$, and $\overline{SLOAD}$ are all high.

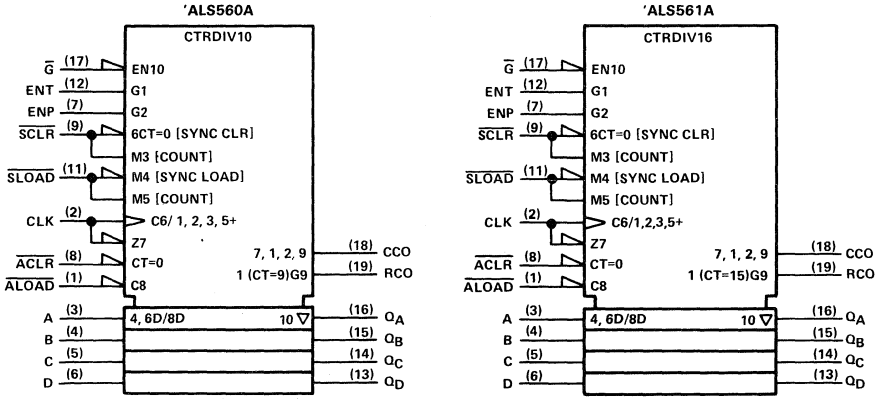
A high level at the Output Enable ($\overline{G}$) forces the Q outputs into the high-impedance state, and a low level enables those outputs. Counting is independent of $\overline{G}$. ENT is fed forward to enable the Ripple Carry Output (RCO) to produce a high-level pulse while the count is maximum (9 or 15). The Clocked Carry Output (CCO) produces a high-level pulse for a duration equal to that of the low level of the clock when RCO is high and the counter is enabled (both ENP and ENT are high); otherwise, CCO is low. CCO does not have the glitches commonly associated with a ripple-carry output. Cascading is normally accomplished by connecting RCO or CCO of the first counter to ENT of the next counter. However, for very-high-speed counting, RCO should be used for cascading since CCO does not become active until the clock returns to the low level.

The SN54ALS560A and SN54ALS561A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS560A and SN74ALS561A are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

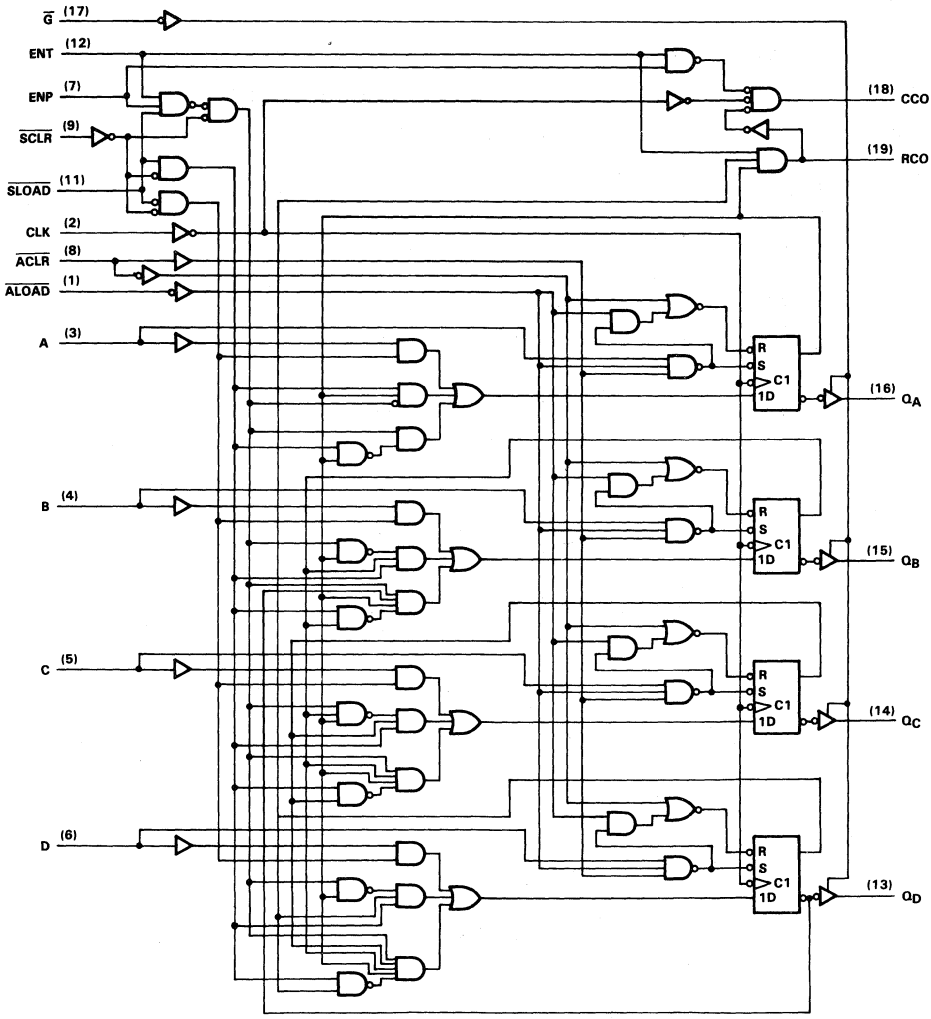
INPUTS								OPERATION
$\overline{G}$	$\overline{ACLR}$	$\overline{ALOAD}$	$\overline{SCLR}$	$\overline{SLOAD}$	ENT	ENP	CLK	
H	X	X	X	X	X	X	X	Q Outputs Disabled
L	L	X	X	X	X	X	X	Asynchronous Clear
L	H	L	X	X	X	X	X	Asynchronous Load
L	H	H	L	X	X	X	↑	Synchronous Clear
L	H	H	H	L	X	X	↑	Synchronous Load
L	H	H	H	H	H	H	↑	Count
L	H	H	H	H	L	X	X	Inhibit Counting
L	H	H	H	H	X	L	X	Inhibit Counting

logic symbols



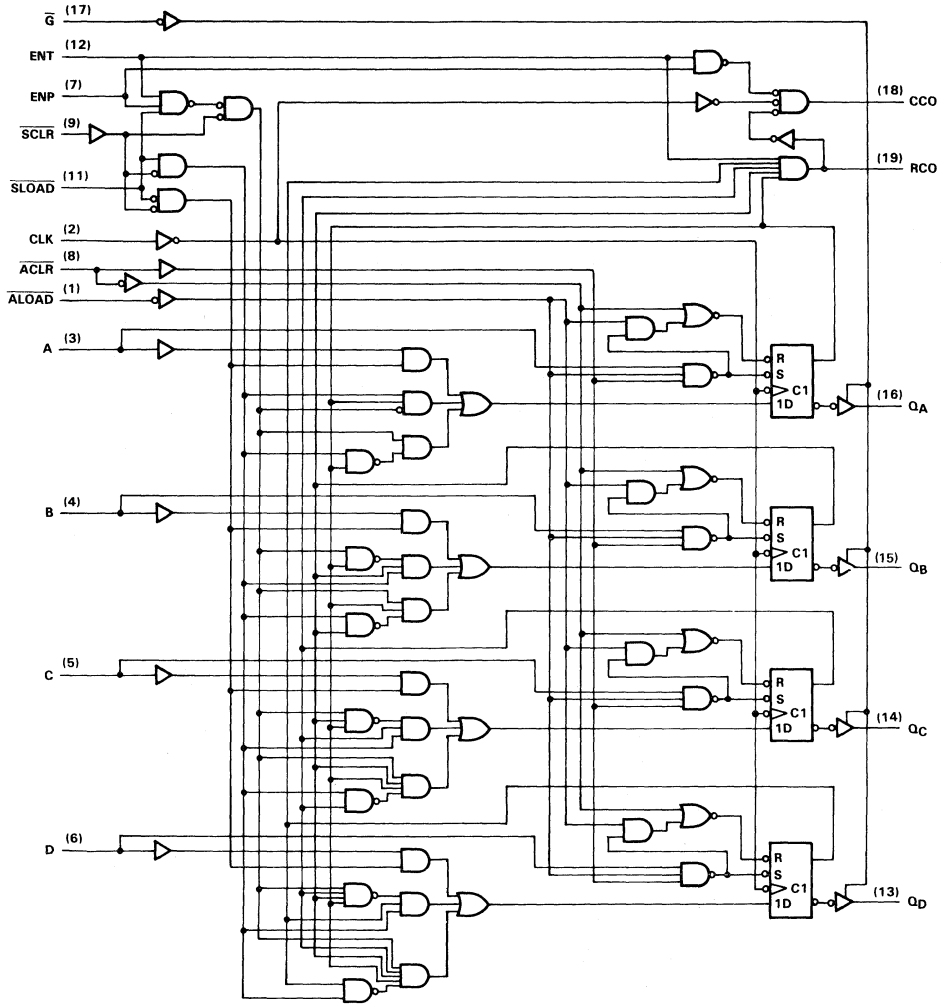
Pin numbers shown are for J and N packages.

'ALS560A logic diagram (positive logic)



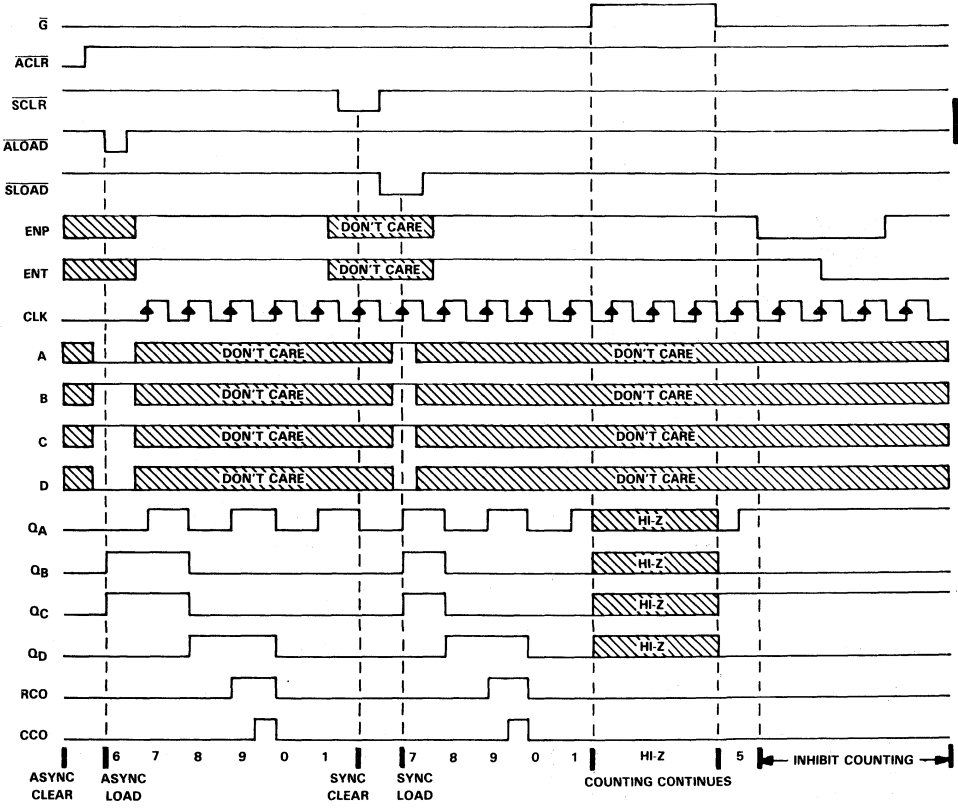
Pin numbers shown are for J and N packages

'ALS561A logic diagram (positive logic)

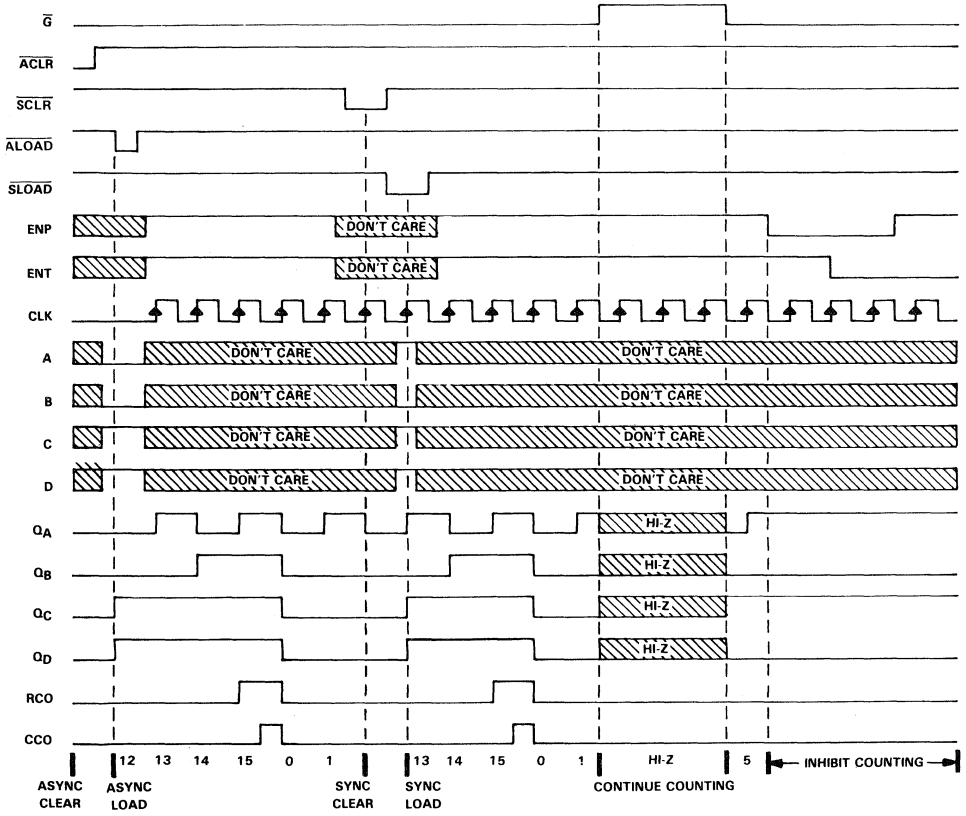


Pin numbers shown are for J and N packages

'ALS560A typical load, count, and inhibit sequences



'ALS561A typical load, count, and inhibit sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS560A, SN54ALS561A . . . . . −55°C to 125°C
SN74ALS560A, SN74ALS561A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

				SN54ALS560A SN54ALS561A			SN74ALS560A SN74ALS561A			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
I_{OH}	High-level output current	Q outputs				−1			−2.6	mA
		CCO and RCO				−0.4			−0.4	
I_{OL}	Low-level output current	Q outputs				12			24	mA
		CCO and RCO				4			8	
f_{clock}	Clock frequency	'ALS560A		0		18	0		20	MHz
		'ALS561A		0		25	0		30	
t_w	Pulse duration	$\overline{ACLR}$ or $\overline{ALOAD}$ low		20			15			ns
		'ALS560A	CLK high	27.5			25			
			CLK low	27.5			25			
		'ALS561A	CLK high	20			16.5			
			CLK low	20			16.5			
t_{su}	Setup time before CLK↑	ENP, ENT	High	25			20			ns
			Low	25			20			
		Data at A, B, C, D		25			20			
		$\overline{SCLR}$	Low	21			15			
			High (inactive)	35			30			
		$\overline{SLOAD}$	Low	20			15			
			High (inactive)	35			30			
		$\overline{ACLR}$ or $\overline{ALOAD}$ inactive		10			10			
t_h	Hold time after CLK↑ for data, ENP, ENT, $\overline{SCLR}$, or $\overline{SLOAD}$			0			0			ns
T_A	Operating free-air temperature			−55		125	0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS560A SN54ALS561A			SN74ALS560A SN74ALS561A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	Q outputs	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
	CCO and RCO	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	ENT and ENP	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	Other inputs					0.1			0.1	
I_{IH}	ENT and ENP	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	Other inputs					20			20	
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	CCO and RCO	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
	Q			−30		−112	−30		−112	
I_{CC}		V_{CC} = 5.5 V	Outputs high		17	27		17	27	mA
			Outputs low		21	33		21	33	
			Outputs disabled		22	36		22	36	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

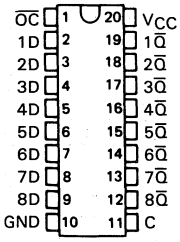
switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS560A SN54ALS561A		SN74ALS560A SN74ALS561A		
			MIN	MAX	MIN	MAX	
f_{max}	'ALS560A		18		20		MHz
	'ALS561A		25		30		
t_{PLH}	CLK	Any Q	4	15	4	12	ns
t_{PHL}			5	21	5	18	
t_{PLH}	CLK	RCO	9	35	9	29	ns
t_{PHL}			8	29	8	24	
t_{PLH}	CLK	CCO	8	31	8	26	ns
t_{PHL}			5	20	5	16	
t_{PLH}	$\overline{ALOAD}$	Any Q	10	38	10	35	ns
t_{PHL}			7	27	7	23	
t_{PLH}	$\overline{ALOAD}$	RCO	15	50	15	40	ns
t_{PHL}			12	35	12	30	
t_{PLH}	$\overline{ALOAD}$	CCO	25	65	25	55	ns
t_{PHL}			12	42	12	33	
t_{PLH}	A, B, C, or D	Any Q	8	35	8	30	ns
t_{PHL}			7	27	7	22	
t_{PLH}	ENT	RCO	5	20	5	16	ns
t_{PHL}			4	18	4	14	
t_{PLH}	ENT	CCO	12	35	12	32	ns
t_{PHL}			4	15	4	12	
t_{PLH}	ENP	CCO	5	22	5	18	ns
t_{PHL}			4	14	4	12	
t_{PHL}	$\overline{ACLR}$	Any Q	7	28	7	22	ns
t_{PZH}	$\overline{G}$	Any Q	5	24	5	19	ns
t_{PZL}			8	28	8	23	
t_{PHZ}	$\overline{G}$	Any Q	2	12	2	10	ns
t_{PLZ}			4	20	4	15	

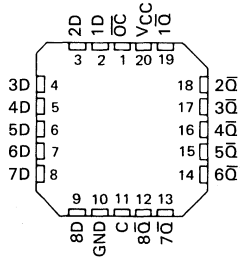
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas instruments Quality and Reliability**

SN54ALS563 . . . J PACKAGE
SN74ALS563 . . . N PACKAGE
SN74ALS563 . . . DW PACKAGE
(TOP VIEW)



SN54ALS563 . . . FH OR FK PACKAGE
SN74ALS563 . . . FN PACKAGE
(TOP VIEW)



description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type latches. While the enable (C) is high the $\overline{Q}$ outputs will follow the complements of data (D) inputs. When the enable is taken low the output will be latched at the inverses of the levels that were set up at the D inputs.

A buffered output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased high-logic level provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

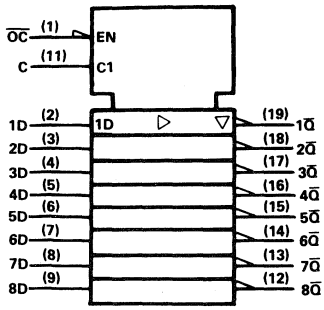
The output control ($\overline{OC}$) does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS563 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS563 is characterized for operation from 0°C to 70°C.

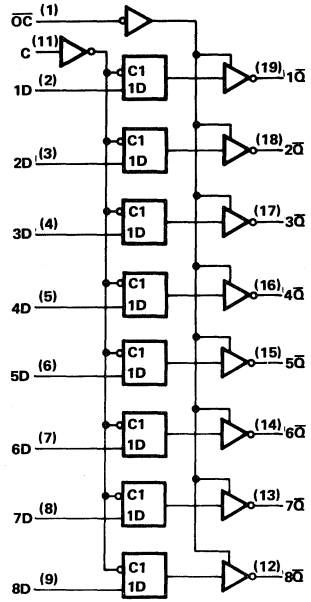
FUNCTION TABLE
(Each Latch)

INPUTS			OUTPUT
ENABLE			
$\overline{OC}$	C	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

logic symbol



logic diagram (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS563 . . . . . −55 °C to 125 °C
SN74ALS563 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS563			SN74ALS563			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
t_w	Pulse duration, enable C high	15			15			ns
t_{su}	Setup time, data before enable C↓	10			10			ns
t_h	Hold time, data after enable C↓	10			10			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS563			SN74ALS563			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		10	17		10	17	mA
		Outputs low		15	24		15	24	
		Outputs disabled		16	27		16	27	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

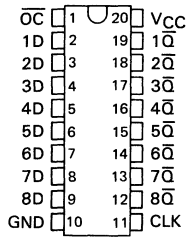
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = MIN to MAX				UNIT
			SN54ALS563		SN74ALS563		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$	3	21	3	18	ns
t_{PHL}			3	15	3	14	
t_{PLH}	C	$\overline{Q}$	8	29	8	22	ns
t_{PHL}			8	22	8	21	
t_{PZH}	$\overline{OC}$	$\overline{Q}$	4	21	4	18	ns
t_{PZL}			4	21	4	18	
t_{PHZ}	$\overline{OC}$	$\overline{Q}$	2	10	2	8	ns
t_{PLZ}			3	15	3	13	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

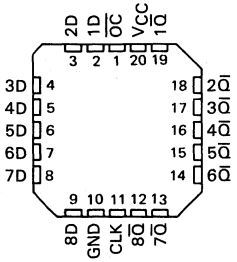
D2661, APRIL 1982—REVISED DECEMBER 1983

- **3-State Buffer-Type Inverting Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **Buffered Control Inputs**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS564 . . . J PACKAGE
SN74ALS564 . . . N PACKAGE
SN74ALS564 . . . DW PACKAGE
(TOP VIEW)



SN54ALS564 . . . FH OR FK PACKAGE
SN74ALS564 . . . FN PACKAGE
(TOP VIEW)



description

These 8-bit registers feature inverting three-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight-bit edge-triggered D-type flip-flops enter data on the low-to-high transition of the clock.

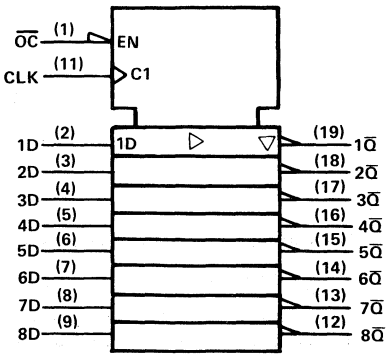
The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS564 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS564 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(EACH FLIP-FLOP)

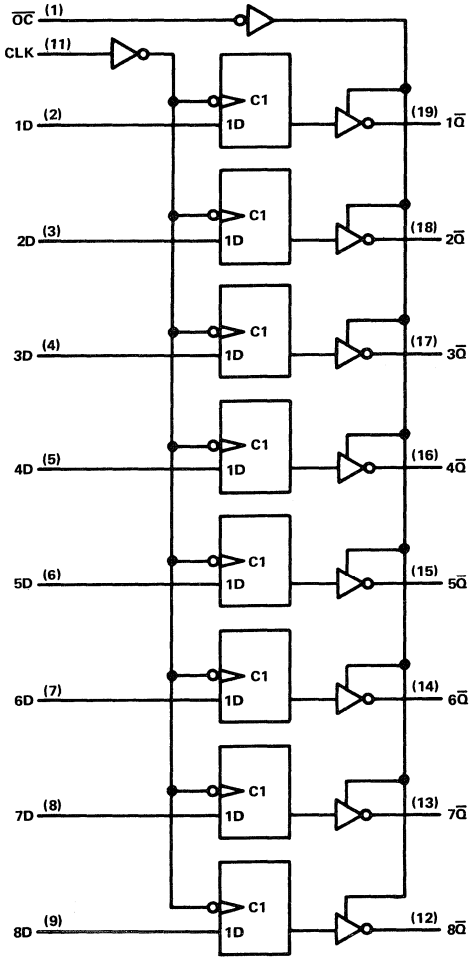
INPUTS			OUTPUT
$\overline{OC}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

logic symbol



Pin numbers shown are for J and N packages.

logic diagram (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS564 . . . . . −55 °C to 125 °C
SN74ALS564 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54ALS564			SN74ALS564			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency		0		30	0		35	MHz
t_w	Pulse duration	CLK high	16.5			14			ns
		CLK low	16.5			14			
t_{su}	Setup time, data before CLK↑		15			15			ns
t_h	Hold time, data after CLK↑		4			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS564			SN74ALS564			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		10	17		10	17	mA
		Outputs low		15	24		15	24	
		Outputs disabled		16	27		16	27	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS564		SN74ALS564		
			MIN	MAX	MIN	MAX	
f_{max}			30		35		MHz
t_{PLH}	CLK	$\overline{Q}$	4	15	4	14	ns
t_{PHL}			4	15	4	14	
t_{PZH}	$\overline{OC}$	$\overline{Q}$	4	21	4	18	ns
t_{PZL}			4	21	4	18	
t_{PHZ}	$\overline{OC}$	$\overline{Q}$	2	10	2	8	ns
t_{PLZ}			3	15	3	13	

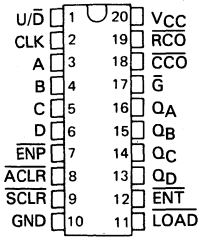
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TYPES SN54ALS568A, SN54ALS569A, SN74ALS568A, SN74ALS569A SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS WITH 3-STATE OUTPUTS

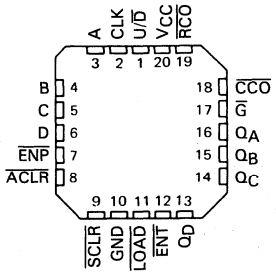
D2661, APRIL 1982—REVISED DECEMBER 1983

- **3-State Q Outputs Drive Bus Lines Directly**
- **Counter Operation Independent of 3-State Output**
- **Fully Synchronous Clear, Count, and Load**
- **Asynchronous Clear Also Provided**
- **Fully Cascadable**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS568A, SN54ALS569A . . . J PACKAGE
SN74ALS568A, SN74ALS569A . . . N PACKAGE
SN74ALS568A, SN74ALS569A . . . DW PACKAGE
(TOP VIEW)



SN54ALS568A, SN54ALS569A . . . FH OR FK PACKAGE
SN74ALS568A, SN74ALS569A . . . FN PACKAGE
(TOP VIEW)



description

The 'ALS568A decade counters and 'ALS569A binary counters are programmable, count up or down, and offer both synchronous and asynchronous clearing. All synchronous functions are executed on the positive-going edge of the clock.

The clear function is initiated by applying a low level to either Asynchronous Clear ($\overline{ACLR}$) or Synchronous Clear ($\overline{SCLR}$). Asynchronous (direct) clearing overrides all other functions of the device, while synchronous clearing overrides only the other synchronous functions. Data is loaded from the A, B, C, and D inputs by holding Load ($\overline{LOAD}$) low during a positive-going clock transition. The counting function is enabled only when Enable P ($\overline{ENP}$) and Enable T ($\overline{ENT}$) are low and $\overline{ACLR}$, $\overline{SCLR}$, and $\overline{LOAD}$ are high. The Up/Down (U/$\overline{D}$) input controls the direction of the count. These counters count up when U/$\overline{D}$ is high and count down when U/$\overline{D}$ is low.

A high level at the Output Enable ($\overline{G}$) forces the Q outputs into the high-impedance state, and a low level enables those outputs. Counting is independent of of $\overline{G}$. $\overline{ENT}$ is fed forward to enable the Ripple Carry Output ($\overline{RCO}$) to produce a low-level pulse while the count is zero (all Q outputs low) when counting down or maximum (9 or 15) when counting up. The Clocked Carry Output ($\overline{CCO}$) produces a low level pulse for a duration equal to that of the low level of the clock when $\overline{RCO}$ is low and the counter is enabled (both $\overline{ENP}$ and $\overline{ENT}$ are low); otherwise, $\overline{CCO}$ is high. $\overline{CCO}$ does not have the glitches commonly associated with a ripple-carry output. Cascading is normally accomplished by connecting $\overline{RCO}$ or $\overline{CCO}$ of the first counter to $\overline{ENT}$ of the next counter. However, for very-high-speed counting, $\overline{RCO}$ should be used for cascading since $\overline{CCO}$ does not become active until the clock returns to the low level.

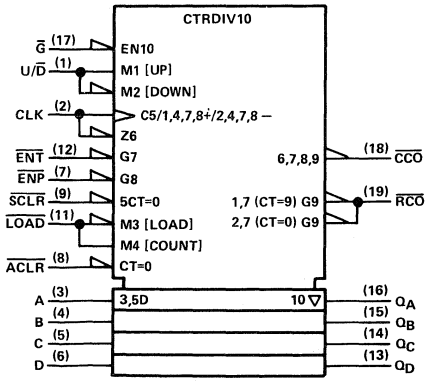
The SN54ALS568A and SN54ALS569A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS568A and SN74ALS569A are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

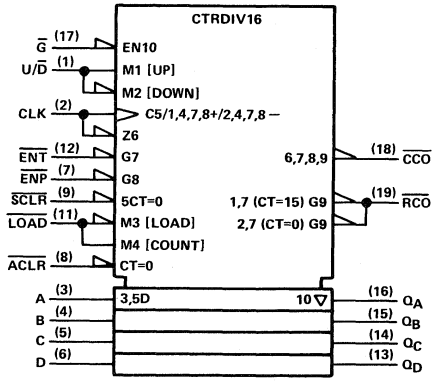
INPUTS								OPERATION
$\overline{G}$	$\overline{ACLR}$	$\overline{SCLR}$	$\overline{LOAD}$	$\overline{ENT}$	$\overline{ENP}$	U/$\overline{D}$	CLK	
H	X	X	X	X	X	X	X	Q Outputs Disabled
L	L	X	X	X	X	X	X	Asynchronous Clear
L	H	L	X	X	X	X	↑	Synchronous Clear
L	H	H	L	X	X	X	↑	Load
L	H	H	H	L	L	H	↑	Count Up
L	H	H	H	L	L	L	↑	Count Down
L	H	H	H	H	X	X	X	Inhibit Count
L	H	H	H	X	H	X	X	Inhibit Count

logic symbols

'ALS568A

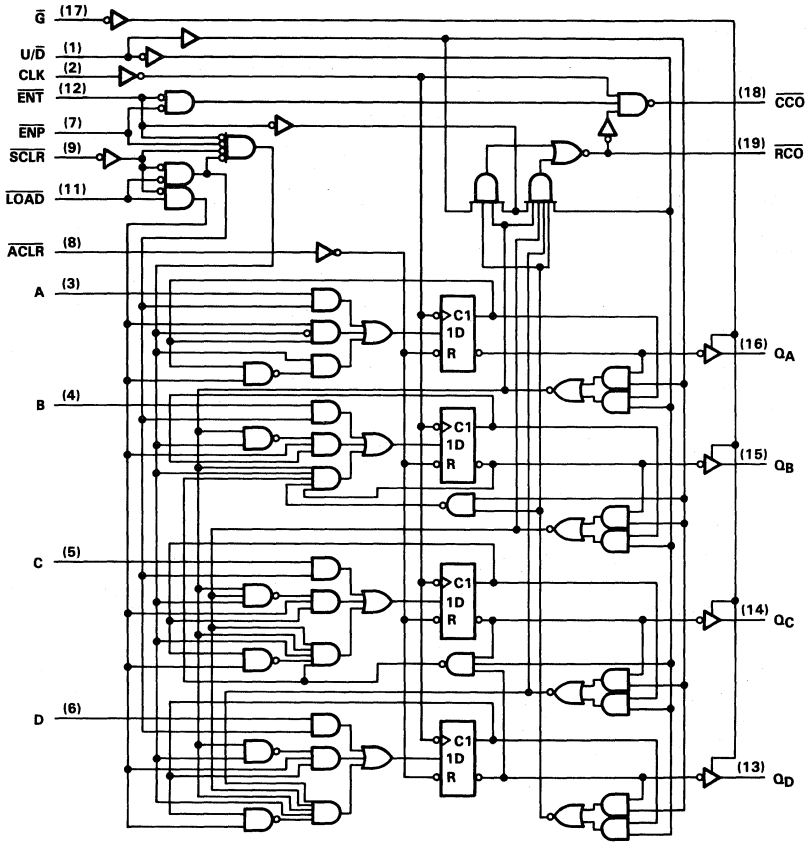


'ALS569A



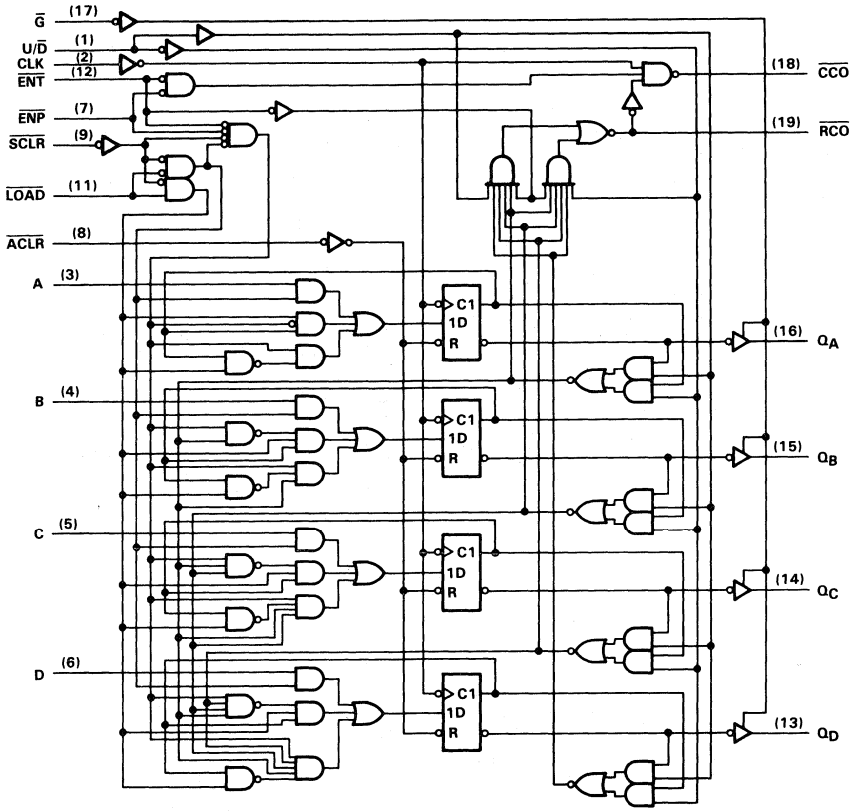
Pin numbers shown are for J and N packages.

'ALS568A logic diagram (positive logic)



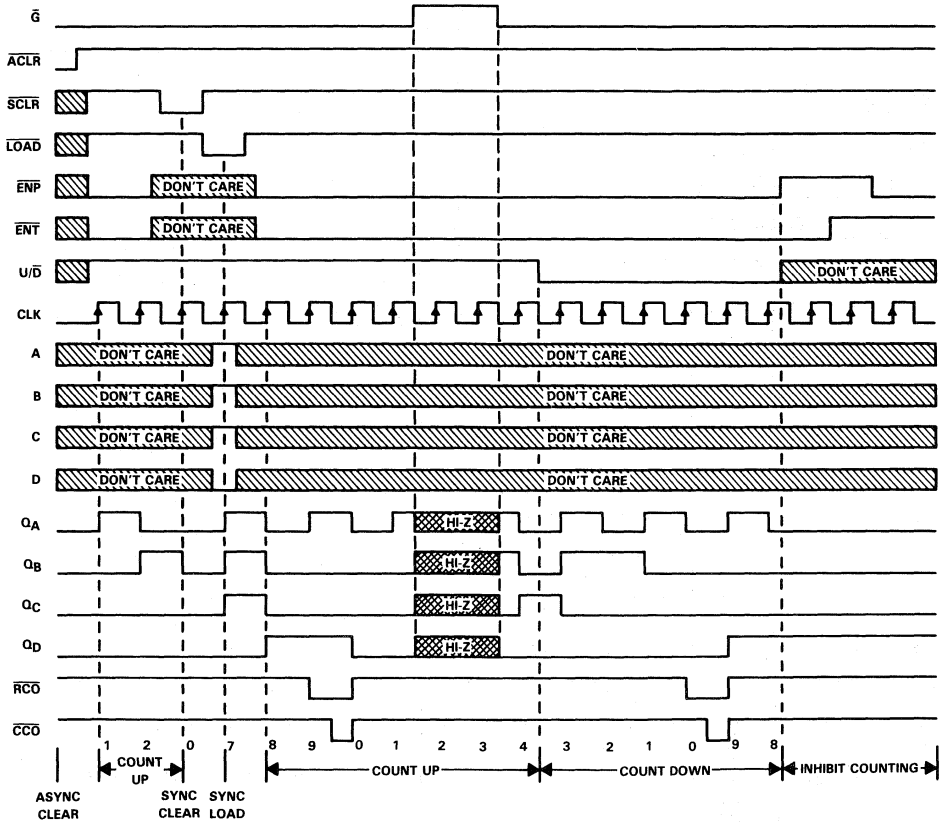
Pin numbers shown are for J and N packages

'ALS569A logic diagram (positive logic)

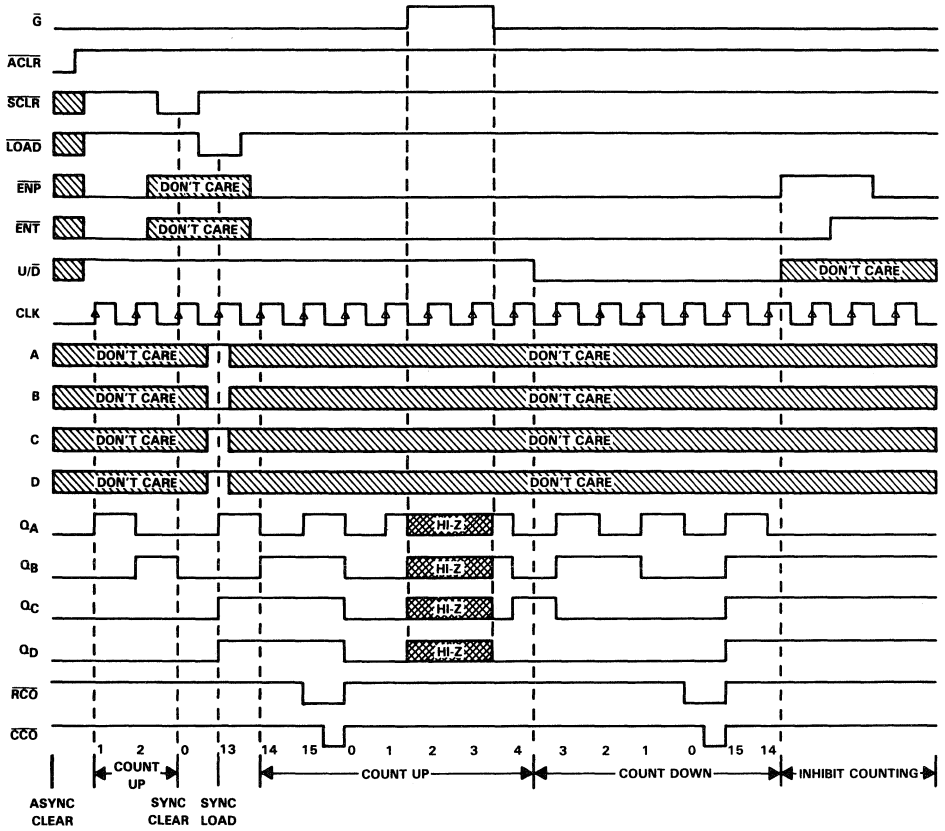


Pin numbers shown are for J and N packages

'ALS568A typical load, count, and inhibit sequences



'ALS569A typical load, count, and inhibit sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS568A, SN54ALS569A . . . . . −55 °C to 125 °C
SN74ALS568A, SN74ALS569A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

2

recommended operating conditions

				SN54ALS568A SN54ALS569A			SN74ALS568A SN74ALS569A			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltge					0.8			0.8	C
I_{OH}	High-level output current	Q outputs				−1			−2.6	mA
		$\overline{CCO}$ and $\overline{RCO}$				−0.4			−0.4	
I_{OL}	Low-level output current	Q outputs				12			24	mA
		$\overline{CCO}$ and $\overline{RCO}$				4			8	
f_{clock}	Clock frequency	'ALS568A		0		18	0		20	MHz
		'ALS569A		0		25	0		30	
t_w	Pulse duration	$\overline{ALCR}$ or $\overline{LOAD}$ low		20			15			ns
		'ALS568A	CLK high	27.5			25			
			CLK low	27.5			25			
		'ALS569A	CLK high	20			16.5			
			CLK low	20			16.5			
t_{su}	Setup time before CLK ↑	Data at A, B, C, D		25			20			ns
		$\overline{ENP}$, $\overline{ENT}$	High	35			30			
			Low	25			20			
		$\overline{SCLR}$	Low	20			15			
			High (inactive)	35			30			
		$\overline{LOAD}$	Low	20			15			
			High (inactive)	35			30			
		U/$\overline{D}$		35			30			
		$\overline{ACLR}$ inactive		10			10			
t_h	Hold time after CLK↑ for any input			0			0			ns
T_A	Operating free-air temperature			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS568A SN54ALS569A			SN74ALS568A SN74ALS569A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	Q outputs	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
	$\overline{CCO}$ and $\overline{RCO}$	V_{CC} = 4.5 V,	I_{OH} = 4 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	$\overline{CCO}$ and $\overline{RCO}$	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
	Q outputs			−30		−112	−30		−112	
I_{CC}		V_{CC} = 5.5 V	Outputs high		16	26		16	26	mA
			Outputs low		20	32		20	32	
			Outputs disabled		20	32		20	32	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS568A SN54ALS569A		SN74ALS568A SN74ALS569A		
			MIN	MAX	MIN	MAX	
f_{max}	'ALS568A		18		20		MHz
	'ALS569A		25		30		
t_{PLH}	CLK	Any Q	4	17	4	13	ns
t_{PHL}			7	18	7	16	
t_{PLH}	CLK	$\overline{RCO}$	12	31	12	28	ns
t_{PHL}			10	22	10	19	
t_{PLH}	CLK	$\overline{CCO}$	5	15	5	13	ns
t_{PHL}			6	30	6	25	
t_{PLH}	U/$\overline{D}$	$\overline{RCO}$	9	25	9	23	ns
t_{PHL}			9	23	9	19	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	6	17	6	15	ns
t_{PHL}			4	17	4	13	
t_{PLH}	$\overline{ENT}$	$\overline{CCO}$	5	15	5	13	ns
t_{PHL}			9	28	9	23	
t_{PLH}	$\overline{ENP}$	$\overline{CCO}$	4	14	4	12	ns
t_{PHL}			5	17	5	14	
t_{PHL}	$\overline{ACLR}$	Any Q	9	22	9	20	ns
t_{PZH}	$\overline{G}$	Any Q	6	21	6	18	ns
t_{PZL}			6	29	6	24	
t_{PHZ}	$\overline{G}$	Any Q	1	12	1	10	ns
t_{PLZ}			3	19	3	13	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982 REVISED NOVEMBER 1984

- 3-State Buffer-Type Outputs Drive Bus-Lines Directly
- Bus-Structured Pinout
- Choice of True or Inverting Logic

  'ALS573A, 'AS573 True Outputs
  'ALS580, 'AS580 Inverting Outputs
- Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

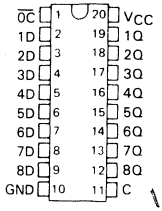
The eight latches are transparent D-type latches. While the enable (C) is high the outputs (Q or $\overline{Q}$) will respond to the data (D) inputs. When the enable is taken low the outputs will be latched to retain the data that was set up.

A buffered output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

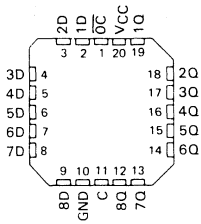
The output control ($\overline{OC}$) does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are at high impedance.

The SN54ALS' and SN54AS' devices are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS' and SN74AS' devices are characterized for operation from 0°C to 70°C.

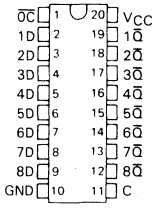
SN54ALS573, SN54AS573 . . . J PACKAGE
SN74ALS573, SN74AS573 . . . N PACKAGE
SN74ALS573, SN74AS573 . . . DW PACKAGE
(TOP VIEW)



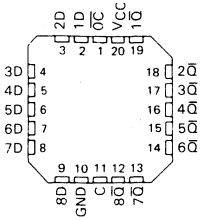
SN54ALS573, SN54AS573 . . . FH OR FK PACKAGE
SN74ALS573, SN74AS573 . . . FN PACKAGE
(TOP VIEW)



SN54ALS580, SN54AS580 . . . J PACKAGE
SN74ALS580, SN74AS580 . . . N PACKAGE
SN74ALS580, SN74AS580 . . . DW PACKAGE
(TOP VIEW)



SN54ALS580, SN54AS580 . . . FH OR FK PACKAGE
SN74ALS580, SN74AS580 . . . FN PACKAGE
(TOP VIEW)



FUNCTION TABLES

'ALS573A, 'AS573
(EACH LATCH)

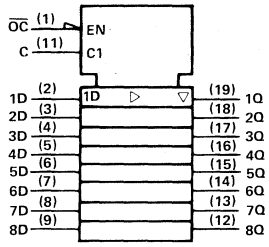
INPUTS			OUTPUT
ENABLE			
$\overline{OC}$	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

'ALS580, 'AS580
(EACH LATCH)

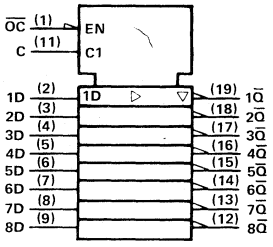
INPUTS			OUTPUT
ENABLE			
$\overline{OC}$	C	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

logic symbols

'ALS573A, 'AS573

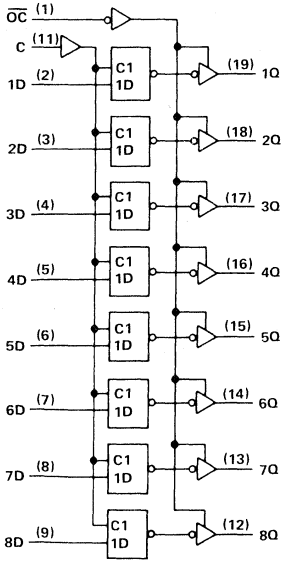


'ALS580, 'AS580

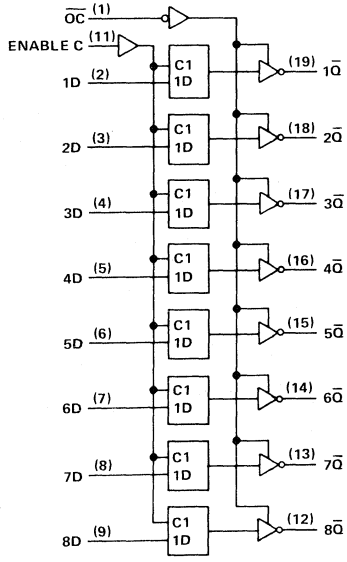


logic diagram (positive logic)

'ALS573A, 'AS573



'ALS580, 'AS580



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range; SN54ALS573A, SN54ALS580 . . . . . −55°C to 125°C
SN74ALS573A, SN74ALS580 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS573A SN54ALS580			SN74ALS573A SN74ALS580			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			−24	mA
t_w	Pulse duration, enable C high	'ALS573A	15			15			ns
		'ALS580	15			15			
t_{su}	Setup time, data before enable C↓		10			10			ns
t_h	Hold time, data after enable C↓	'ALS573A	7			7			ns
		'ALS580	10			10			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS573A SN54ALS580			SN74ALS573A SN74ALS580			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V,			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS573A	V_{CC} = 5.5 V	Outputs high		10	17		10	17	mA
			Outputs low		15	24		15	24	
			Outputs disabled		16	27		16	27	
	'ALS580		Outputs high		10	17		10	17	
			Outputs low		15	24		15	24	
			Outputs disabled		16	27		16	27	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS573A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54/74ALS573A			SN54ALS573A		SN74ALS573A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q		7	9	2	15	2	14	ns
t_{PHL}				7	9	2	15	2	14	
t_{PLH}	C	Q		12	16	8	25	8	20	ns
t_{PHL}				12	16	8	20	8	19	
t_{PZH}	$\overline{OC}$	Q		9	12	4	21	4	18	ns
t_{PZL}				11	17	4	21	4	18	
t_{PHZ}	$\overline{OC}$	Q		5	7	2	12	2	10	ns
t_{PLZ}				5	7	2	15	2	12	

'ALS580 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS580		SN74AS580		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$	3	21	3	18	ns
t_{PHL}			3	15	3	14	
t_{PLH}	C	$\overline{Q}$	8	29	8	22	ns
t_{PHL}			8	22	8	21	
t_{PZH}	$\overline{OC}$	$\overline{Q}$	4	21	4	18	ns
t_{PZL}			4	21	4	18	
t_{PHZ}	$\overline{OC}$	$\overline{Q}$	2	10	2	8	ns
t_{PLZ}			3	15	3	13	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS573, SN54AS580 . . . . . −55°C to 125°C
SN74AS573, SN74AS580 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS573 SN54AS580			SN74AS573 SN74AS580			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				32			−48	mA
t_w	Pulse duration, enable C high	'AS573	5.5			4.5			ns
		'AS580	3			2			
t_{su}	Setup time, data before enable C↑		2			2			ns
t_h	Hold time, data after enable C↑		3			3			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS573 SN54AS580			SN74AS573 SN74AS580			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.28	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.33	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V,			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS573	V_{CC} = 5.5 V	Outputs high		56	93		56	93	mA
			Outputs low		55	90		55	90	
			Outputs disabled		65	106		65	106	
	'ALS580		Outputs high		62	100		62	100	
			Outputs low		65	106		65	106	
			Outputs disabled		71	115		71	115	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS573 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS573		SN74AS573		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	3	9	3	6	ns
t_{PHL}			3	7	3	6	
t_{PLH}	C	Q	6	14	6	11.5	ns
t_{PHL}			4	9	4	7.5	
t_{PZH}	$\overline{OC}$	Q	2	8	2	6.5	ns
t_{PZL}			4	11	4	9.5	
t_{PHZ}	$\overline{OC}$	Q	2	8	2	6.5	ns
t_{PLZ}			2	8	2	7	

'AS580 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS580		SN74AS580		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$	3	10	3	7.5	ns
t_{PHL}			3	7.5	3	7	
t_{PLH}	C	$\overline{Q}$	5	12	5	9	ns
t_{PHL}			4	8.5	4	8	
t_{PZH}	$\overline{OC}$	$\overline{Q}$	2	7.5	2	6.5	ns
t_{PZL}			4	10.5	4	9.5	
t_{PHZ}	$\overline{OC}$	$\overline{Q}$	2	7.5	2	6.5	ns
t_{PLZ}			2	8	2	7	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

D2661, JUNE 1982—REVISED NOVEMBER 1984

- 3-State Buffer-Type Noninverting Outputs Drive Bus-Lines Directly
- Bus-Structured Pinout
- Buffered Control Inputs
- 'ALS575 and 'AS575 Have Synchronous Clear
- Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 8-bit registers feature three-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight edge-triggered D-type flip-flops enter data on the low-to-high transition of the clock. The 'ALS575 and 'AS575 may be synchronously cleared by taking the $\overline{CLR}$ input low.

The output-control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS' and SN54AS' devices are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS' and SN74AS' devices are characterized for operation from 0°C to 70°C.

FUNCTION TABLES

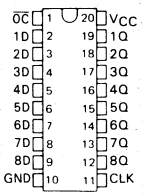
'ALS574A, 'AS574
(EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

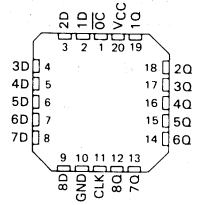
'ALS575, 'AS575
(EACH FLIP-FLOP)

INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	CLK	D	Q
L	L	↑	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	Q_0
H	X	X	X	Z

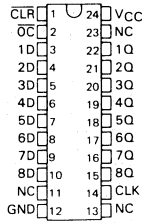
SN54ALS574A, SN54AS574 . . . J PACKAGE
SN74ALS574A, SN74AS574 . . . N PACKAGE
SN74ALS574A, SN74AS574 . . . DW PACKAGE
(TOP VIEW)



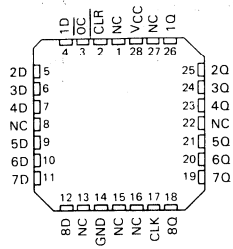
SN54ALS574A, SN54AS574 . . . FH OR FK PACKAGE
SN74ALS574A, SN74AS574 . . . FN PACKAGE
(TOP VIEW)



SN54ALS575, SN54AS575 . . . J PACKAGE
SN74ALS575, SN74AS575 . . . N PACKAGE
SN74ALS575, SN74AS575 . . . DW PACKAGE
(TOP VIEW)



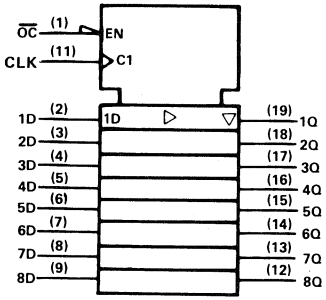
SN54ALS575, SN54AS575 . . . FH OR FK PACKAGE
SN74ALS575, SN74AS575 . . . FN PACKAGE
(TOP VIEW)



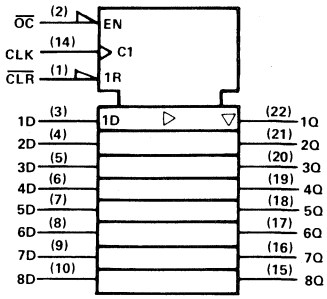
NC—No internal connection

logic symbols

'ALS574A, 'AS574

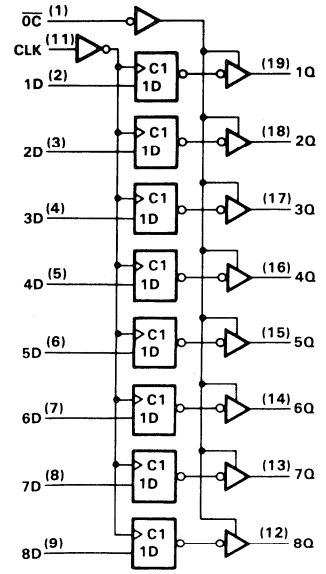


'ALS575, 'AS575



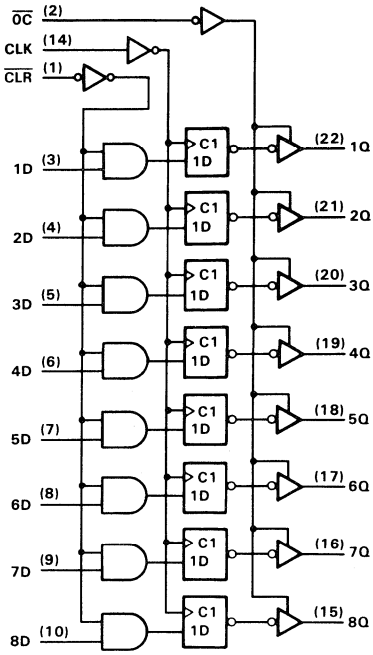
logic diagrams (positive logic)

'ALS574A, 'AS574



Pin numbers shown are for J and N packages.

'ALS575, 'AS575



Pin numbers shown are for JT and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS574A, SN54ALS575 . . . . . −55°C to 125°C
SN74ALS574A, SN74ALS575 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

				SN54ALS574A SN54ALS575			SN74ALS574A SN74ALS575			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
I_{OH}	High-level output current					−1			−2.6	mA
I_{OL}	Low-level output current					12			24	mA
f_{clock}	Clock frequency	'ALS574A		0		30	0		35	MHz
		'ALS575		0		25	0		30	
t_w	Pulse duration	'ALS574A CLK high or low		16.5			14			ns
		'ALS575 CLK high or low		20			16.5			
t_{su}	Setup time before CLK↑	Data		15			15			ns
		'ALS575	$\overline{CLR}$ high	20			20			
			$\overline{CLR}$ low	15			15			
t_h	Hold time after CLK↑	Data		4			0			ns
		'ALS575	$\overline{CLR}$	0			0			
T_A	Operating free-air temperature			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS574A SN54ALS575			SN74ALS574A SN74ALS575			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS574A	V_{CC} = 5.5 V	Outputs high		11	18		11	18	mA
			Outputs low		17	27		17	27	
			Outputs disabled		17	28		17	28	
	'ALS575		Outputs high		10	17		10	17	
			Outputs low		15	24		15	24	
			Outputs disabled		16	27		16	27	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS574A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C, SN54/74ALS574A			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX, SN54ALS574A		SN74ALS574A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			40	50		30		35		MHz
t_{PLH}	CLK	Q		8	10	4	15	4	14	ns
t_{PHL}				8	10	4	15	4	14	
t_{PZH}	$\overline{OC}$	Q		9	12	4	21	4	18	ns
t_{PZL}				12	15	4	21	4	18	
t_{PHZ}	$\overline{OC}$	Q		5	7	2	12	2	10	ns
t_{PLZ}				5	7	2	15	2	12	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

'ALS575 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS575		SN74ALS575		
			MIN	MAX	MIN	MAX	
f_{max}			25		30		MHz
t_{PLH}	CLK	Q	4	15	4	14	ns
t_{PHL}			4	15	4	14	
t_{PZH}	OC	Q	4	21	4	18	ns
t_{PZL}			4	21	4	18	
t_{PHZ}	$\overline{OC}$	Q	2	12	2	10	ns
t_{PLZ}			3	15	3	13	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

2

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS574, SN54AS575 . . . . . −55°C to 125°C
SN74AS574, SN74AS575 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

				SN54AS574 SN54AS575			SN74AS574 SN74AS575			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
I_{OH}	High-level output current					−12			−15	mA
I_{OL}	Low-level output current					32			48	mA
f_{clock}	Clock frequency			0		100	0		125	MHz
t_w	Pulse duration	CLK high		5			4			ns
		CLK low		3			2			
tsu	Setup time before CLK↑	Data		3			2			ns
		'AS575	$\overline{CLR}$ high or low	6.5			5.5			
t_h	Hold time after CLK↑	Data		3			2			ns
		'ALS575	$\overline{CLR}$	0			0			
T_A	Operating free-air temperature			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS574 SN54AS575			SN74AS574 SN74AS575			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.29	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.34	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	$\overline{OC}$, CLK, $\overline{CLR}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	D					−3			−2	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS574	V_{CC} = 5.5 V	Outputs high		73	116		73	116	mA
			Outputs low		85	134		85	134	
			Outputs disabled		84	134		84	134	
	'AS575		Outputs high		78	126		78	126	
			Outputs low		89	142		89	142	
			Outputs disabled		88	142		88	142	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

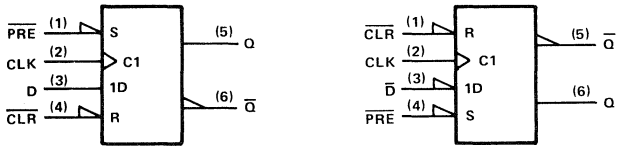
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS574 SN54AS575		SN74AS574 SN74AS575		
			MIN	MAX	MIN	MAX	
f_{max}			100		125		MHz
t_{PLH}	CLK	Any Q	3	11	3	8	ns
t_{PHL}			4	11	4	9	
t_{PZH}	$\overline{OC}$	Any Q	2	7	2	6	ns
t_{PZL}			3	11	3	10	
t_{PHZ}	$\overline{OC}$	Any Q	2	7	2	6	ns
t_{PLZ}			2	7	2	6	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

D flip-flop signal conventions

It is TI practice to name the outputs and other inputs of a D-type flip-flop and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a Q output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active low.

In some applications it may be advantageous to redesignate the data input $\overline{D}$. In that case all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.



Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (▷) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 ($\overline{Q}$) is still in phase with the data input $\overline{D}$, but now both are considered active-low.

- **3-State Buffer-Type Inverting Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **Buffered Control Inputs**
- **'ALS577 and 'AS577 Have Synchronous Clear**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 8-bit registers feature three-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight-bit edge-triggered D-type flip-flops enter data on the low-to-high transition of the clock.

The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN54ALS' and SN54AS' devices are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS' and SN74AS' devices are characterized for operation from 0°C to 70°C.

FUNCTION TABLES

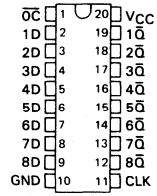
ALS576, AS576
(Each Flip-Flop)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

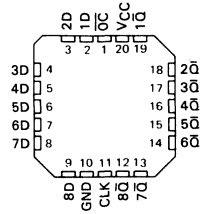
ALS577, AS577
(Each Flip-Flop)

INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	CLK	D	$\overline{Q}$
L	L	↑	X	H
L	H	↑	H	L
L	H	↑	L	H
L	H	L	X	$\overline{Q}_0$
H	X	X	X	Z

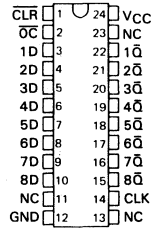
SN54ALS576, SN54AS576 . . . J PACKAGE
SN74ALS576, SN74AS576 . . . N PACKAGE
SN74ALS576, SN74AS576 . . . DW PACKAGE
(TOP VIEW)



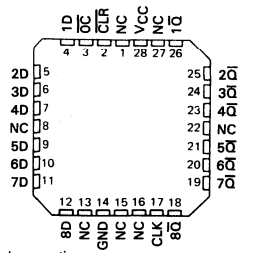
SN54ALS576, SN54AS576 . . . FH OR FK PACKAGE
SN74ALS576, SN74AS576 . . . FN PACKAGE
(TOP VIEW)



SN54ALS577, SN54AS577 . . . J PACKAGE
SN74ALS577, SN74AS577 . . . N PACKAGE
SN74ALS577, SN74AS577 . . . DW PACKAGE
(TOP VIEW)



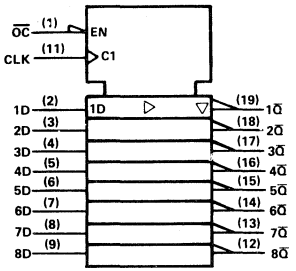
SN54ALS577, SN54AS577 . . . FH OR FK PACKAGE
SN74ALS577, SN74AS577 . . . FN PACKAGE
(TOP VIEW)



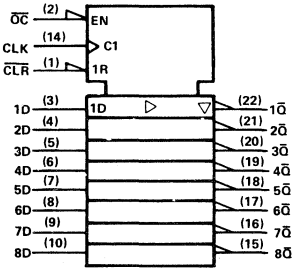
NC — No internal connection

logic symbols

'ALS576, 'AS576

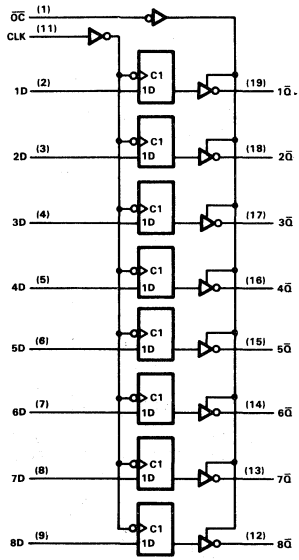


'ALS577, 'AS577



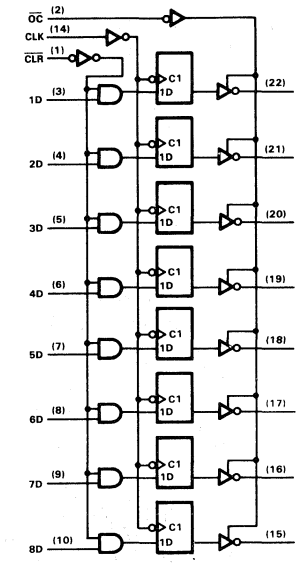
logic diagrams (positive logic)

'ALS576, 'AS576



Pin numbers shown are for J and N packages.

'ALS577, 'AS577



Pin numbers shown are for JT and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS', SN54AS' . . . . . −55 °C to 125 °C
SN74ALS', SN74AS' . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54ALS576 SN54ALS577			SN74ALS576 SN74ALS577			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency	'ALS576	0		25	0		30	MHz
		'ALS577	0		25	0		30	
t_w	Pulse duration	CLK high or low 'ALS576	20			16.5			ns
		CLK high or low 'ALS577	20			16.5			
t_{su}	Setup time before CLK↑	Data	15			15			ns
		$\overline{CLR}$ ('ALS577)	15			15			
t_h	Hold time after CLK↑	Data	4			0			ns
		$\overline{CLR}$ ('ALS577)	4			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS576 SN54ALS577			SN74ALS576 SN74ALS577			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4				V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		10	17		10	17	mA
		Outputs low		15	24		15	24	
		Outputs disabled		16	27		16	27	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS576 SN54ALS577		SN74ALS576 SN74ALS577		
			MIN	MAX	MIN	MAX	
f_{max}	'ALS576		25		30		MHz
	'ALS577		25		30		
t_{PLH}	CLK	Any $\overline{Q}$	4	15	4	14	ns
t_{PHL}			4	15	4	14	
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$	4	21	4	18	ns
t_{PZL}			4	21	4	18	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$ ALS576	2	10	2	8	ns
		Any $\overline{Q}$ ALS577	2	12	2	10	
t_{PLZ}		Any $\overline{Q}$	3	15	3	13	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

recommended operating conditions

			SN54AS576 SN54AS577			SN74AS576 SN74AS577			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				32			48	mA
f_{clock}	Clock frequency		0		100	0		125	MHz
t_w	Pulse duration	CLK high	5			4			ns
		CLK low	3			2			
t_{su}	Setup time before CLK↑	Data	3			2			ns
		$\overline{CLR}$ ('AS577)	6.5			5.5			
t_h	Hold time after CLK↑	Data	3			2			ns
		$\overline{CLR}$ ('AS577)	0			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS576 SN54AS577			SN74AS576 SN74AS577			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.29	0.5				V
		V_{CC} = 4.5 V	I_{OL} = 48 mA					0.33	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	D	V_{CC} = 5.5 V,	V_I = 0.4 V			−3			−2	mA
	All other					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS576	V_{CC} = 5.5 V	Outputs high		77	125		77	125	mA
			Outputs low		84	135		84	135	
			Outputs disabled		84	135		84	135	
	'AS577		Outputs high		78	126		78	126	
			Outputs low		76	123		76	123	
			Outputs disabled		88	142		88	142	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS576 SN54AS577		SN74AS576 SN74AS577		
			MIN	MAX	MIN	MAX	
f_{max}			100		125		MHz
t_{PLH}	CLK	Any $\overline{Q}$	3	11	3	8	ns
t_{PHL}			4	11	4	9	
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$	2	7	2	6	ns
t_{PZL}			3	11	3	10	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$	2	7	2	6	ns
t_{PLZ}			2	7	2	6	

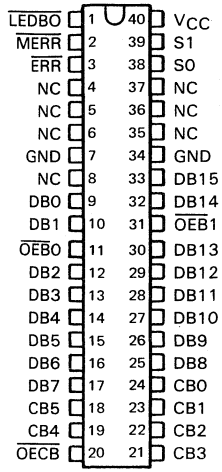
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D2640, APRIL 1984—REVISED JANUARY 1985

- **Detects and Corrects Single-Bit Errors**
- **Detects and Flags Dual-Bit Errors**
- **Built-In Diagnostic Capability**
- **Fast Write and Read Cycle Processing Times**
- **Byte-Write Capability**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	OUTPUT
'ALS616	3-State
'ALS617	Open-Collector

SN54ALS616, SN54ALS617 . . . JD PACKAGE
SN74ALS616, SN74ALS617 . . . JD OR N PACKAGE
(TOP VIEW)



NC—No internal connection.

For chip carrier information, contact the factory.

description

The 'ALS616 and 'ALS617 are 16-bit parallel error detection and correction circuits in 40-pin, 600-mil packages. The EDACs use a modified Hamming code to generate a 6-bit check word from a 16-bit data word. This check word is stored along with the data word during the memory write cycle. During memory read cycles, the 22-bit words from memory are processed by the EDACs to determine if errors have occurred in memory.

Single-bit errors in the 16-bit data word are flagged and corrected. Single-bit errors in the 6-bit check word are flagged, but the data word will remain unaltered. The 6-bit error syndrome code will pinpoint the error-generating location.

Dual-bit errors are flagged but not corrected. These errors may occur in any two bits of the 22-bit word from memory. The gross-error condition of all lows or all highs from memory will be detected. Otherwise, errors in three or more bits of the 22-bit word are beyond the capabilities of these devices to detect.

Read-modify-write (byte-control) operations can be performed with the 'ALS616 and 'ALS617 EDACs by using output latch enable, $\overline{\text{LEDBO}}$, and individual $\overline{\text{OEB0}}$ and $\overline{\text{OEB1}}$ byte control pins.

Diagnostics are performed on the EDACs by controls and internal paths that allow the user to read the contents of the DB and CB input latches. These will determine if the failure occurred in memory or in the EDAC.

The SN54ALS616 and SN54ALS617 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS616 and SN74ALS617 are characterized for operation from 0°C to 70°C.

TABLE 1. WRITE CONTROL FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB CONTROL $\overline{OEB0}$ & $\overline{OEB1}$	DB OUTPUT LATCH $\overline{LEDBO}$	CHECK I/O	CB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$	ERROR FLAGS $\overline{MERR}$
Write	Generate check word	L	L	Input	H	X	Output check bits†	L	H	H

†See Table 2 for details on check bit generation.

memory write cycle details

During a memory write cycle, the check bits (CB0 thru CB5) are generated internally in the EDAC by six 8-input parity generators using the 16-bit data word as defined in Table 2. These six check bits are stored in memory along with the original 16-bit data word. This 22-bit word will later be used in the memory read cycle for error detection and correction.

TABLE 2. PARITY ALGORITHM

CHECK WORD BIT	16-BIT DATA WORD 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CB0			X		X	X	X			X			X		X	X
CB1		X		X		X	X	X				X		X		X
CB2	X			X	X			X	X		X			X	X	
CB3	X	X	X				X	X			X	X	X			
CB4	X	X	X	X	X	X			X	X						
CB5									X	X	X	X	X	X	X	X

The six check bits are parity bits derived from the matrix of data bits as indicated by "X" for each bit.

error detection and correction details

During a memory read cycle, the 6-bit check word is retrieved along with the actual data. In order to be able to determine whether the data from memory is acceptable to use as presented to the bus, the error flags must be tested to determine if they are at the high level.

The first case in Table 3 represents the normal, no-error conditions. The EDAC presents highs on both flags. The next two cases of single-bit errors give a high on $\overline{MERR}$ and a low on $\overline{ERR}$, which is the signal for a correctable error, and the EDAC should be sent through the correction cycle. The last three cases of double-bit errors will cause the EDAC to signal lows on both $\overline{ERR}$ and $\overline{MERR}$, which is the interrupt indication for the CPU.

TABLE 3. ERROR FUNCTION

TOTAL NUMBER OF ERRORS 16-BIT DATA WORD	6-BIT CHECK WORD	ERROR FLAGS $\overline{ERR}$	ERROR FLAGS $\overline{MERR}$	DATA CORRECTION
0	0	H	H	Not applicable
1	0	L	H	Correction
0	1	L	H	Correction
1	1	L	L	Interrupt
2	0	L	L	Interrupt
0	2	L	L	Interrupt

TABLE 4. READ, FLAG, AND CORRECT FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB CONTROL $\overline{OEB0}$ & $\overline{OEB1}$	DB OUTPUT LATCH $\overline{LEDBO}$	CHECK I/O	CB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$ $\overline{MERR}$
Read	Read & flag	H	L	Input	H	X	Input	H	Enabled†
Read	Latch input data & check bits	H	H	Latched input data	H	L	Latched input check word	H	Enabled†
Read	Output corrected data and syndrome bits	H	H	Output corrected data word	L	X	Output syndrome bits‡	L	Enabled†

†See Table 3 for error description.
‡See Table 5 for error location.

Error detection is accomplished as the 6-bit check word and the 16-bit data word from memory are applied to the internal parity generators/checkers. If the parity of all six groupings of data and check bits are correct, it is assumed that no error has occurred and both error flags will be high.

If the parity of one or more of the check groups is incorrect, an error has occurred and the proper error flag or flags will be set low. The two-bit error is not correctable since the parity tree can only identify single-bit errors. Both error flags are set low when any two-bit error is detected.

Three or more simultaneous bit errors can cause the EDAC to believe that no error, a correctable error, or an uncorrectable error has occurred and will produce erroneous results in all three cases. It should be noted that the gross-error conditions of all highs will be detected.

As the corrected word is made available on the data I/O port (DB0 thru DB15), the check word I/O port (CB0 thru CB5) presents a 6-bit syndrome error code. This syndrome code can be used to locate the bad memory chip. See Table 5 for syndrome decoding.

TABLE 5. SYNDROME DECODING

SYNDROME BITS						ERROR
5	4	3	2	1	0	
L	L	L	L	L	L	2-bit
L	L	L	L	L	H	unc
L	L	L	L	H	L	unc
L	L	L	L	H	H	2-bit
L	L	L	H	L	L	unc
L	L	L	H	L	H	2-bit
L	L	L	H	H	L	2-bit
L	L	L	H	H	H	unc
L	L	H	L	L	L	unc
L	L	H	L	L	H	2-bit
L	L	H	L	H	L	2-bit
L	L	H	L	H	H	DB7
L	L	H	H	L	L	2-bit
L	L	H	H	L	H	unc
L	L	H	H	H	L	DB6
L	L	H	H	H	H	2-bit

SYNDROME BITS						ERROR
5	4	3	2	1	0	
L	H	L	L	L	L	unc
L	H	L	L	L	H	2-bit
L	H	L	L	H	L	2-bit
L	H	L	L	H	H	DB5
L	H	L	H	L	L	2-bit
L	H	L	H	L	H	DB4
L	H	L	H	H	L	DB3
L	H	L	H	H	H	2-bit
L	H	H	L	L	L	2-bit
L	H	H	L	L	H	DB2
L	H	H	L	H	L	DB1
L	H	H	L	H	H	2-bit
L	H	H	H	L	L	DB0
L	H	H	H	L	H	2-bit
L	H	H	H	H	L	2-bit
L	H	H	H	H	H	CB5

SYNDROME BITS						ERROR
5	4	3	2	1	0	
H	L	L	L	L	L	unc
H	L	L	L	L	H	2-bit
H	L	L	L	H	L	2-bit
H	L	L	L	H	H	DB15
H	L	L	H	L	L	2-bit
H	L	L	H	L	H	DB14
H	L	L	H	H	L	DB13
H	L	L	H	H	H	2-bit
H	L	H	L	L	L	2-bit
H	L	H	L	L	H	DB12
H	L	H	L	H	L	DB11
H	L	H	L	H	H	2-bit
H	L	H	H	L	L	DB10
H	L	H	H	L	H	2-bit
H	L	H	H	H	L	2-bit
H	L	H	H	H	H	CB4

SYNDORME BITS						ERROR
5	4	3	2	1	0	
H	H	L	L	L	L	2-bit
H	H	L	L	L	H	DB8
H	H	L	L	H	L	unc
H	H	L	L	H	H	2-bit
H	H	L	H	L	L	DB9
H	H	L	H	L	H	2-bit
H	H	L	H	H	L	2-bit
H	H	L	H	H	H	CB3
H	H	H	L	L	L	unc
H	H	H	L	L	H	2-bit
H	H	H	L	H	L	2-bit
H	H	H	L	H	H	CB2
H	H	H	H	L	L	2-bit
H	H	H	H	L	H	CB1
H	H	H	H	H	L	CB0
H	H	H	H	H	H	none

CB X = error in check bit X
DB Y = error in data bit Y
2-bit = double-bit error
unc = uncorrectable multibit error

read-modify-write (byte control) operations

The 'ALS616 and 'ALS617 devices are capable of byte-write operations. The 22-bit word from memory must first be latched into the DB and CB input latches. This is easily accomplished by switching from the read and flag mode (S1 = H, S0 = L) to the latch input mode (S1 = H, S0 = H). The EDAC will then make any corrections, if necessary, to the data word and place it at the input of the output data latch. This data word must then be latched into the output data latch by taking $\overline{\text{LEDBO}}$ from a low to a high.

Byte control can now be employed on the data word through the $\overline{\text{OEB}}$0 or $\overline{\text{OEB}}$1 controls. $\overline{\text{OEBO}}$ controls DB0-DB7 (byte 0), $\overline{\text{OEB}}$1 controls DB8-DB15 (byte 1).

Placing a high on the byte control will disable the output and the user can modify the byte. If a low is placed on the byte control, then the original byte is allowed to pass onto the data bus unchanged. If the original data word is altered through byte control, a new check word must be generated before it is written back into memory. This is easily accomplished by taking control S1 and S0 low. Table 6 lists the read-modify-write functions.

TABLE 6. READ-MODIFY-WRITE FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1	CONTROL S0	BYTEn†	$\overline{OEBn}$†	DB OUTPUT LATCH $\overline{LEDBO}$	CHECK I/O	CB CONTROL	ERROR FLAG $\overline{ERR}$	ERROR FLAG $\overline{MERR}$
Read	Read & Flag	H	L	Input	H	X	Input	H	Enabled	
Read	Latch input data & check bits	H	H	Latched Input data	H	L	Latched input check word	H	Enabled	
Read	Latch corrected data word into output latch	H	H	Latched output data word	H	H	Hi-Z	H	Enabled	
							Output Syndrome bits	L		
Modify/ write	Modify appropriate byte or bytes & generate new check word	L	L	Input modified BYTE0	H	H	Output check word	L	H	H
				Output unchanged BYTE0	L					

†$\overline{OEB0}$ controls DB0-DB7 (BYTE0), $\overline{OEB1}$ controls DB8-DB15 (BYTE1)

diagnostic operations

The 'ALS616 and 'ALS617 are capable of diagnostics that allow the user to determine whether the EDAC or the memory is failing. The diagnostic function tables will help the user to see the possibilities for diagnostic control.

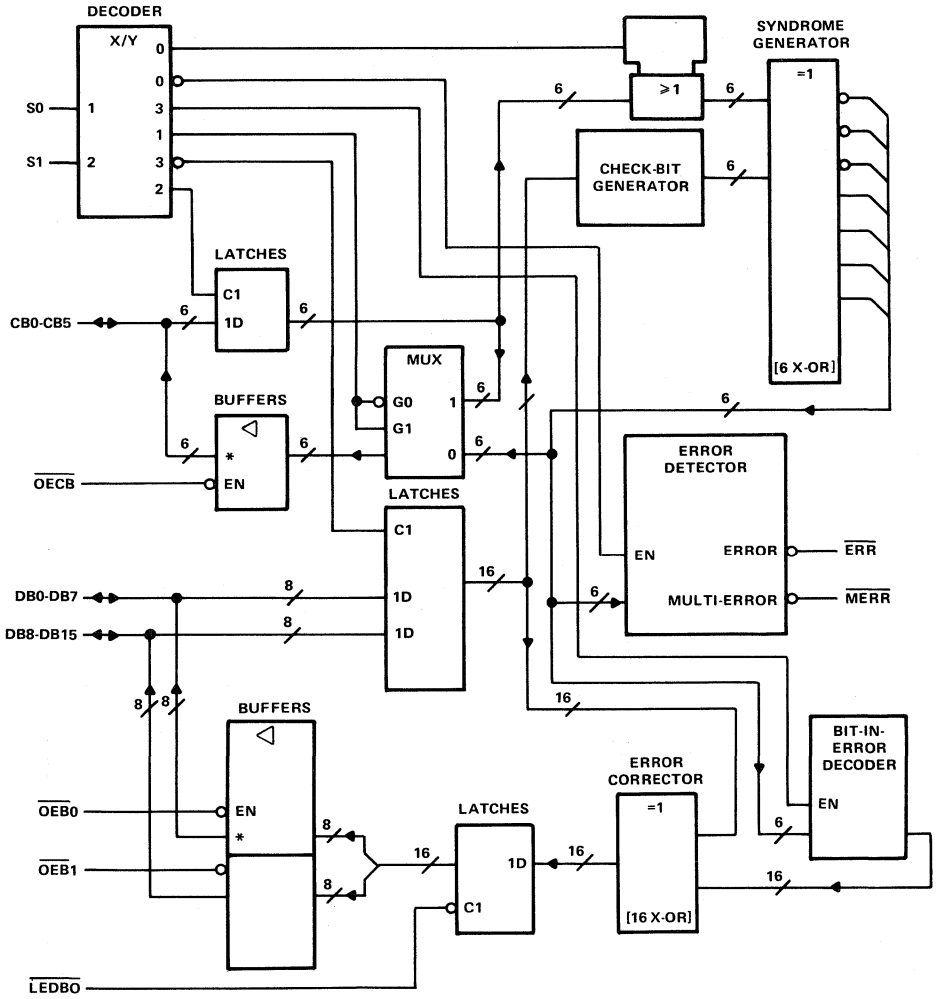
In the diagnostic mode (S1 = L, S0 = H), the checkword is latched into the input latch while the data input latch remains transparent. This lets the user apply various data words against a fixed known checkword. If the user applies a diagnostic data word with an error in any bit location, the $\overline{ERR}$ flag should be low. If a diagnostic data word with two errors in any bit location is applied, the $\overline{MERR}$ flag should be low. After the checkword is latched into the input latch, it can be verified by taking $\overline{OECB}$ low. This outputs the latched checkword. The diagnostic data word can be latched into the output data latch and verified via the $\overline{LEDB0}$ control pin. By changing from the diagnostic mode (S1 = L, S0 = H), the user can verify that the EDAC will correct the diagnostic data word. Also, the syndrome bits can be produced to verify that the EDAC pinpoints the error location. Table 7 lists the diagnostic functions.

TABLE 7. DIAGNOSTIC FUNCTION

EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB BYTE CONTROL $\overline{OEBn}$	DB OUTPUT LATCH $\overline{LEDBO}$	CHECK I/O	CB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$	ERROR FLAGS $\overline{MERR}$
Read & flag	H	L	Input correct data word	H	X	Input correct check bits	H	H	H
Latch input check word while data input latch remains transparent	L	H	Input diagnostic data word†	H	L	Latched input check bits	H	Enabled	
Latch diagnostic data word into output latch	L	H	Input diagnostic data word†	H	H	Output latched check bits	L	Enabled	
						Hi-Z	H		
Latch diagnostic data word into input latch	H	H	Latched input diagnostic data word	H	H	Output syndrome bits	L	Enabled	
						Hi-Z	H		
Output diagnostic data word & syndrome bits	H	H	Output diagnostic data word	L	H	Output syndrome bits	L	Enabled	
						Hi-Z	H		
Output corrected diagnostic data word & output syndrome bits	H	H	Output corrected diagnostic data word	L	L	Output syndrome bits	L	Enabled	
						Hi-Z	H		

†Diagnostic data is a data word with an error in one bit location except when testing the $\overline{MERR}$ error flag. In this case, the diagnostic data word will contain errors in two bit locations.

logic diagram (positive logic)



*'ALS616 has 3-state (▽) check-bit and data outputs.
'ALS617 has open-collector(◇) check-bit and data outputs.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: CB and DB . . . . . 5.5 V
All others . . . . . 7 V
Operating case temperature range, SN54ALS616, SN54ALS617, ... −55°C to 125°C
Operating free-air temperature range, SN74ALS616, SN74ALS617 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS616 SN54ALS617			SN74ALS616 SN74ALS617			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.675			0.8	V
V_{OH}	High-level output voltage	DB or CB, 'ALS617			5.5			5.5	V
I_{OH}	High-level output current	$\overline{ERR}$ or $\overline{MERR}$			−0.4			−0.4	mA
		DB or CB, 'ALS616			−1			−2.6	
I_{OL}	Low-level output current	$\overline{ERR}$ or $\overline{MERR}$			4			8	mA
		DB or CB			12			24	
t_w	Pulse duration	$\overline{LEDB0}$ low	45			25			ns
t_{su}	Setup time	(1) Data and check word before S0↑ (S1 = H)	15			12			ns
		(2) S0 high before $\overline{LEDB0}$↑ (S1 = H)†	45			45			
		(3) $\overline{LEDB0}$ high before the earlier of S0↓ or S1↓†	0			0			
		(4) $\overline{LEDB0}$ high before S1↑ (S0 = H)	0			0			
		(5) Diagnostic data word before S1↑ (S0 = H)	28			12			
		(6) Diagnostic check word before the later of S1↓ or S0↑	15			12			
		(7) Diagnostic data word before $\overline{LEDB0}$↑ (S1 = L and S0 = H)†	35			20			
t_h	Hold time	(8) Read-mode, S0 low and S1 high	35			30			ns
		(9) Data and check word after S0↑ (S1 = H)	20			15			
		(10) Data word after S1↑ (S0 = H)	20			15			
		(11) Check word after the later of S1↓ or S0↑	20			15			
		(12) Diagnostic data word after $\overline{LEDB0}$↑ (S1 = L, S0 = H)‡	0			0			
t_{corr}	Correction time (see Figure 1)		70			65			ns
T_C	Operating case temperature		−55		125				°C
T_A	Operating free-air temperature					0		70	°C

†These times ensure that corrected data is saved in the output data latch.
‡These times ensure that the diagnostic data word is saved in the output data latch.

'ALS616 electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS616			SN74ALS616			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	DB or CB	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5 V,	I_{OH} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
	DB or CB	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	S0 or S1	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	DB or CB	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	S0 or S1	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	DB or CB‡					20			20	
I_{IL}	S0 or S1	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.4			−0.4	mA
	DB or CB‡					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	See Note 1		110	190		110	170	mA

'ALS617 electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS617			SN74ALS617			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
I_{OH}	DB or CB	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5 V,	I_{OH} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
	DB or CB	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	S0 or S1	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	DB or CB	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	S0 or S1	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	DB or CB‡					20			20	
I_{IL}	S0 or S1	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.4			−0.4	mA
	DB or CB‡					−0.1			−0.1	
I_O§	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	See Note 1		110			110		mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

NOTE 1: I_{CC} is measured with S0 and S1 at 4.5 V and all CB and DB pins grounded.

Additional information on these products can be obtained from the factory as it becomes available.

'ALS616 switching characteristics, V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_C = −55°C to 125°C for SN54ALS616, T_A = 0°C to 70°C for SN74ALS616

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ALS616		SN74ALS616		UNIT
				MIN	MAX	MIN	MAX	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500 Ω	10	43	10	40	ns
	DB	$\overline{ERR}$	S1 = L, S0 = H, R_L = 500 Ω	10	43	10	40	
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500 Ω	15	65	15	55	ns
	DB	$\overline{MERR}$	S1 = L, S0 = H, R_L = 500 Ω	15	65	15	55	
t_{pd}	S0↓ and S1↓	CB	R1 = R2 = 500 Ω	10	60	10	49	ns
t_{pd}	DB	CB	S1 = L, S0 = L, R1 = R2 = 500 Ω	10	60	10	49	ns
t_{pd}	$\overline{LEDBO}$↓	DB	S1 = X, S0 = H, R1 = R2 = 500 Ω	7	35	7	30	ns
t_{pd}	S1↑	CB	S0 = H, R1 = R2 = 500 Ω	10	50	10	50	ns
t_{en}	$\overline{OECB}$↓	CB	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	30	2	27	ns
t_{dis}	$\overline{OECB}$↑	CB	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	30	2	27	ns
t_{en}	$\overline{OEB0}$ and $\overline{OEB1}$↓	DB	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	30	2	27	ns
t_{dis}	$\overline{OEB0}$ and $\overline{OEB1}$↑	DB	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	30	2	27	ns

'ALS617 switching characteristics, V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_C = −55°C to 125°C for SN54ALS617, T_A = 0°C to 70°C for SN74ALS617

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ALS617			SN74ALS617			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500 Ω		26			26		ns
	DB	$\overline{ERR}$	S1 = L, S0 = H, R_L = 500 Ω		26			26		
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500 Ω		40			40		ns
			S1 = L, S0 = H, R_L = 500 Ω		40			40		
t_{pd}	S0↓ and S1↓	CB	R_L = 680 Ω		40			40		ns
t_{pd}	DB	CB	S1 = L, S0 = L, R_L = 680 Ω		40			40		ns
t_{pd}	$\overline{LEDBO}$↓	DB	S1 = X, S0 = H, R_L = 680 Ω		26			26		ns
t_{pd}	S1↑	CB	S0 = H, R_L = 680 Ω		40			40		ns
t_{PLH}	$\overline{OECB}$↑	CB	S1 = X, S0 = H, R_L = 680 Ω		24			24		ns
t_{PHL}	$\overline{OECB}$↓	CB	S1 = X, S0 = H, R_L = 680 Ω		24			24		ns
t_{PLH}	$\overline{OEB0}$ and $\overline{OEB1}$↑	DB	S1 = X, S0 = H, R_L = 680 Ω		24			24		ns
t_{PHL}	$\overline{OEB0}$ and $\overline{OEB1}$↓	DB	S1 = X, S0 = H, R_L = 680 Ω		24			24		ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

Additional information on these products can be obtained from the factory as it becomes available.

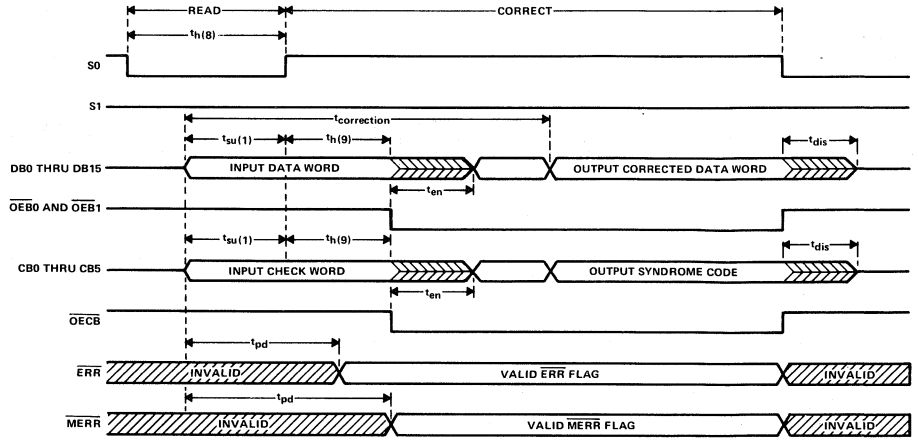


FIGURE 1. READ, FLAG, AND CORRECT MODE SWITCHING WAVEFORMS

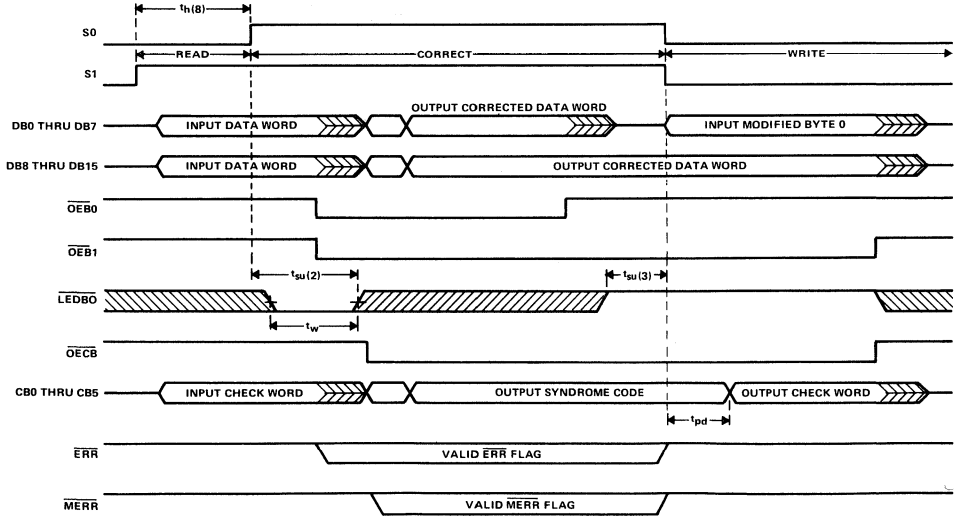


FIGURE 2. READ, CORRECT, MODIFY MODE SWITCHING WAVEFORMS

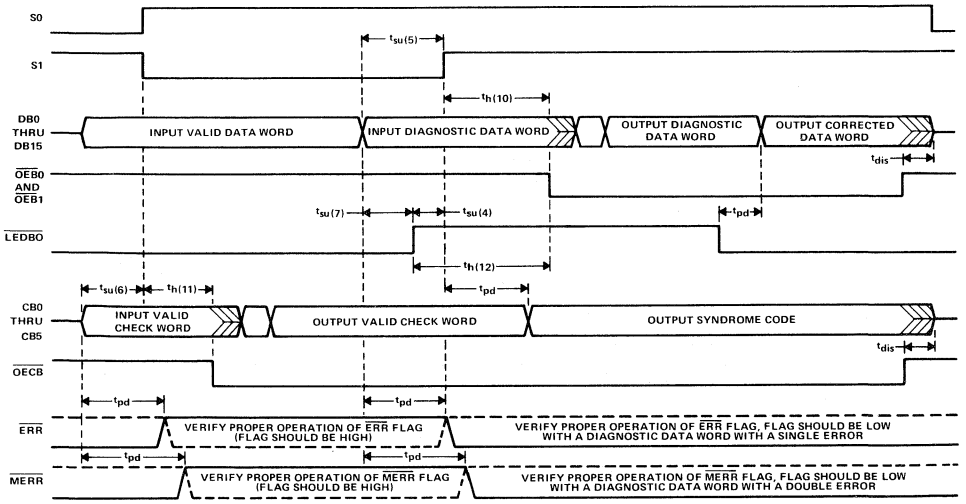


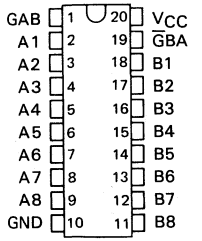
FIGURE 3. DIAGNOSTIC MODE SWITCHING WAVEFORM

D2661, DECEMBER 1982—REVISED FEBRUARY 1984

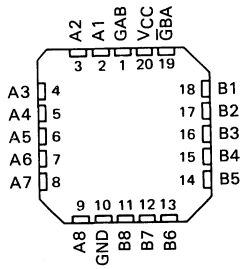
- **Bus Transceivers in High-Density 20-Pin DIP and Small Outline (SO) and the New Plastic and Ceramic Chip Carriers**
- **Local Bus-Latch Capability**
- **Choice of True or Inverting Logic**
- **Choice of 3-State or Open-Collector Outputs**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	OUTPUT	LOGIC
'ALS620A, 'AS620	3-State	Inverting
'ALS621A, 'AS621	Open-Collector	True
'ALS622A, 'AS622	Open-Collector	Inverting
'ALS623A, 'AS623	3-State	True

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . N PACKAGE
SN74ALS', SN74AS' . . . DW PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FH OR FK PACKAGE
SN74ALS', SN74AS' . . . FN PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}$BA and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the octal bus transceivers the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the 'ALS621A, 'AS621 and 'ALS623A, 'AS623 or complementary for the 'ALS620A, 'AS620 and 'ALS622A, 'AS622.

The -1 versions of the SN74ALS' parts are identical to their standard versions except that the recommended maximum I_{OL} is increased to 48 mA. There are no -1 versions of the SN54ALS' parts.

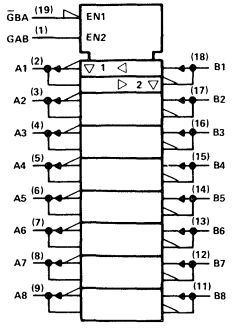
The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

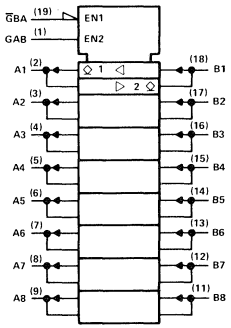
ENABLE INPUTS		OPERATION	
$\overline{G}$BA	GAB	'ALS620A, 'ALS622A 'AS620, 'AS622	'ALS621A, 'ALS623A 'AS621, 'AS623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Isolation	Isolation
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus	B data to A bus, A data to B bus

logic symbols

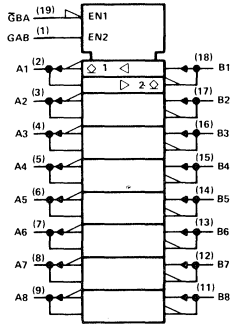
'ALS620A, 'AS620



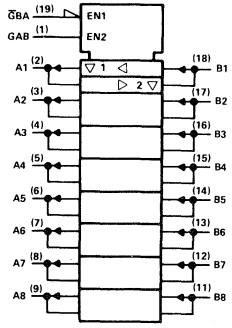
'ALS621A, 'AS621



'ALS622A, 'AS622



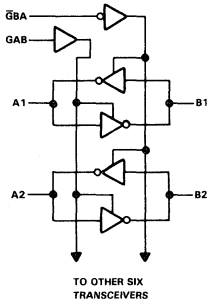
'ALS623A, 'AS623



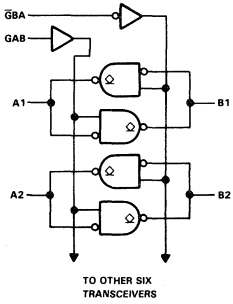
Pin numbers shown are for J and N packages.

logic diagrams (positive logic)

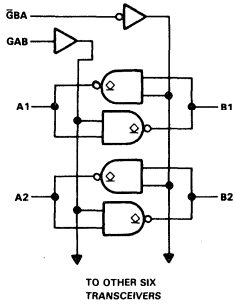
'ALS620A, 'AS620



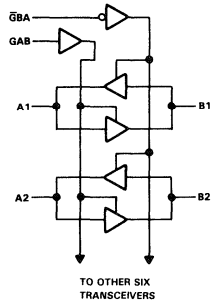
'ALS621A, 'AS621



'ALS622A, 'AS622



'ALS623A, 'AS623



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS620A, SN54ALS623A . . . . . −55°C to 125°C
SN74ALS620A, SN74ALS623A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS620A SN54ALS623A			SN74ALS620A SN74ALS623A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS620A-1 and SN74ALS623A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS620A SN54ALS623A			SN74ALS620A SN74ALS623A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports§					−0.1			−0.1	
I_O¶		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS620A	V_{CC} = 5.5 V	Outputs high		24	39		24	34	mA
			Outputs low		31	49		31	44	
			Outputs disabled		33	52		33	47	
	'ALS623A	V_{CC} = 5.5 V	Outputs high		32	48		32	43	
			Outputs low		39	55		39	50	
			Outputs disabled		42	60		42	55	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS620A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS620A		SN74ALS620A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2	12	2	10	ns
t_{PHL}			2	12	2	10	
t_{PLH}	B	A	2	12	2	10	ns
t_{PHL}			2	12	2	10	
t_{PZH}	$\overline{G}$BA	A	3	23	3	17	ns
t_{PZL}			5	31	5	25	
t_{PHZ}	$\overline{G}$BA	A	2	14	2	12	ns
t_{PLZ}			3	22	3	18	
t_{PZH}	GAB	B	3	23	3	18	ns
t_{PZL}			5	31	5	25	
t_{PHZ}	GAB	B	2	14	2	12	ns
t_{PLZ}			3	22	3	18	

'ALS623A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS623A		SN74ALS623A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2	15	2	13	ns
t_{PHL}			3	13	3	11	
t_{PLH}	B	A	2	15	2	13	ns
t_{PHL}			3	13	3	11	
t_{PZH}	$\overline{G}$BA	A	5	25	5	22	ns
t_{PZL}			5	25	5	22	
t_{PHZ}	$\overline{G}$BA	A	2	19	2	16	ns
t_{PLZ}			2	23	2	19	
t_{PZH}	GAB	B	5	25	5	22	ns
t_{PZL}			5	25	5	22	
t_{PHZ}	GAB	B	2	19	2	16	ns
t_{PLZ}			2	23	2	19	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs and I/O ports . . . . . 7 V
Operating free-air temperature range: SN54ALS621A, SN54ALS622A . . . . . −55°C to 125°C
SN74ALS621A, SN74ALS622A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS621A SN54ALS622A			SN74ALS621A SN74ALS622A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS621A-1 and SN74ALS622A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS621A SN54ALS622A			SN74ALS621A SN74ALS622A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for -1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports§					−0.1			−0.1	
I_{CC}	'ALS621A	V_{CC} = 5.5 V	Outputs high		29	45		29	40	mA
			Outputs low		35	53		35	48	
	'ALS622A	V_{CC} = 5.5 V	Outputs high		11	20		11	15	
			Outputs low		20	33		20	28	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

'ALS621A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS621A		SN74ALS621A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	10	45	10	33	ns
t_{PHL}			5	24	5	20	
t_{PLH}	B	A	10	45	10	33	ns
t_{PHL}			5	24	5	20	
t_{PLH}	$\overline{G}BA$	A	10	47	10	39	ns
t_{PHL}			12	40	12	35	
t_{PLH}	GAB	B	10	47	10	39	ns
t_{PHL}			12	40	12	35	

'ALS622A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS622A		SN74ALS622A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	8	42	8	35	ns
t_{PHL}			5	23	5	19	
t_{PLH}	B	A	8	42	8	35	ns
t_{PHL}			5	23	5	19	
t_{PLH}	$\overline{G}BA$	A	8	45	8	38	ns
t_{PHL}			10	40	10	35	
t_{PLH}	GAB	B	8	45	8	38	ns
t_{PHL}			10	40	10	35	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54AS620, SN54AS623 . . . . . −55 °C to 125 °C
SN74AS620, SN74AS623 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS620 SN54AS623			SN74AS620 SN74AS623			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS620 SN54AS623			SN74AS620 SN74AS623			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.30	0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA					0.35	0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					70			70	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A or B ports‡					−0.75			−0.75	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−150	−50		−150	mA
I_{CC}	'AS620	V_{CC} = 5.5 V	Outputs high		35	57		35	57	mA
			Outputs low		74	122		74	122	
			Outputs disabled		48	77		48	77	
	'AS623	V_{CC} = 5.5 V	Outputs high		57	93		57	93	
			Outputs low		116	189		116	189	
			Outputs disabled		71	116		71	116	

†All typical values are at V_{CC2} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS620 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS620		SN74AS620		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1	8	1	7	ns
t_{PHL}			2	7	2	6	
t_{PLH}	B	A	1	8	1	7	ns
t_{PHL}			2	7	2	6	
t_{PZH}	$\overline{G}$BA	A	2	8.5	2	8	ns
t_{PZL}			2	10	2	9	
t_{PHZ}	$\overline{G}$BA	A	1	7.5	1	6	ns
t_{PLZ}			2	15	2	12	
t_{PZH}	GAB	B	2	9	2	8	ns
t_{PZL}			2	10.5	2	9	
t_{PHZ}	GAB	B	1	6.5	1	6	ns
t_{PLZ}			2	16	2	13	

'AS623 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS623		SN74AS623		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1	10	1	9	ns
t_{PHL}			1	9	1	8	
t_{PLH}	B	A	1	10	1	9	ns
t_{PHL}			1	9.5	1	8.5	
t_{PZH}	$\overline{G}$BA	A	2	11.5	2	11	ns
t_{PZL}			2	11	2	10	
t_{PHZ}	$\overline{G}$BA	A	1	8.5	1	7.5	ns
t_{PLZ}			1	13.5	1	11.5	
t_{PZH}	GAB	B	2	13	2	11.5	ns
t_{PZL}			2	12	2	11	
t_{PHZ}	GAB	B	1	8	1	7	ns
t_{PLZ}			1	10.5	1	9	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs and I/O ports . . . . . 7 V
Operating free-air temperature range: SN54AS621, SN54AS622 . . . . . −55°C to 125°C
SN74AS621, SN74AS622 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS621 SN54AS622			SN74AS621 SN74AS622			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS621 SN54AS622			SN74AS621 SN74AS622			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.30	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					70			70	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A or B ports‡					−0.75			−0.75	
I_{CC}	'AS621	V_{CC} = 5.5 V	Outputs high		48	79		48	79	mA
			Outputs low		116	189		116	189	
	'AS622	V_{CC} = 5.5 V	Outputs high		24	39		24	39	
			Outputs low		63	103		63	103	

†All typical values are at V_{CC} = 5 V, T_A = 25°C
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

'AS621 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS621		SN74AS621		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	5	28.5	5	24	ns
t_{PHL}			1	8.5	1	7.5	
t_{PLH}	B	A	5	23	5	21	ns
t_{PHL}			1	8.5	1	7.5	
t_{PLH}	$\overline{G}$BA	A	5	24	5	21	ns
t_{PHL}			1	10	1	9	
t_{PLH}	GAB	B	5	26	5	22	ns
t_{PHL}			1	11	1	10	

'AS622 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS622		SN74AS622		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	5	28.5	5	24.5	ns
t_{PHL}			1	8.5	1	8	
t_{PLH}	B	A	5	30	5	25	ns
t_{PHL}			1	8.5	1	8	
t_{PLH}	$\overline{G}$BA	A	5	26	5	22	ns
t_{PHL}			1	11.5	1	10	
t_{PLH}	GAB	B	5	26	5	23	ns
t_{PHL}			1	11.5	1	10.5	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

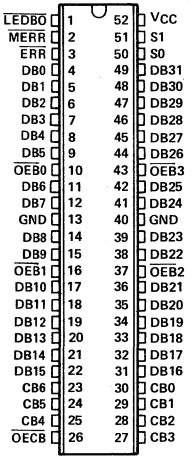
32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

D2661, DECEMBER 1982—REVISED SEPTEMBER 1984

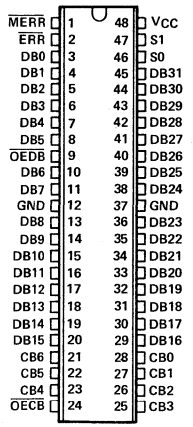
- **Detects and Corrects Single-Bit Errors**
- **Detects and Flags Dual-Bit Errors**
- **Built-In Diagnostic Capability**
- **Fast Write and Read Cycle Processing Times**
- **Byte-Write Capability . . . 'ALS632A and 'ALS633**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	PACKAGE	BYTE-WRITE	OUTPUT
'ALS632A	52-pin	yes	3-State
'ALS633	52-pin	yes	Open-Collector
'ALS634	48-pin	no	3-State
'ALS635	48-pin	no	Open-Collector

'ALS632A, 'ALS633 . . . JD PACKAGE
(TOP VIEW)



'ALS634, 'ALS635 . . . . JD PACKAGE
(TOP VIEW)



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description

The 'ALS632A and 'ALS633 through 'ALS635 devices are 32-bit parallel error detection and correction circuits (EDACs) in 52-pin ('ALS632A and 'ALS633) or 48-pin ('ALS634 and 'ALS635) 600-mil packages. The EDACs use a modified Hamming code to generate a 7-bit check word from a 32-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 39-bit words from memory are processed by the EDACs to determine if errors have occurred in memory.

Single-bit errors in the 32-bit data word are flagged and corrected.

Single-bit errors in the 7-bit check word are flagged, and the CPU sends the EDAC through the correction cycle even though the 32-bit data word is not in error. The correction cycle will simply pass along the original 32-bit data word in this case and produce error syndrome bits to pinpoint the error-generating location.

Dual-bit errors are flagged but not corrected. These errors may occur in any two bits of the 39-bit word from memory (two errors in the 32-bit data word, two errors in the 7-bit check word, or one error in each word). The gross-error condition of all lows or all highs from memory will be detected. Otherwise, errors in three or more bits of the 39-bit word are beyond the capabilities of these devices to detect.

Read-modify-write (byte-control) operations can be performed with the 'ALS632A and 'ALS633 EDACs by using output latch enable, $\overline{\text{LEDBO}}$, and the individual $\overline{\text{OEB0}}$ thru $\overline{\text{OEB3}}$ byte control pins.

Diagnostics are performed on the EDACs by controls and internal paths that allow the user to read the contents of the DB and CB input latches. These will determine if the failure occurred in memory or in the EDAC.

TABLE 1. WRITE CONTROL FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB CONTROL $\overline{OEBn}$ OR $\overline{OEDB}$	DB OUTPUT LATCH ('ALS632A, 'ALS633) $\overline{LEDBO}$	CHECK I/O	CB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$	ERROR FLAGS $\overline{MERR}$
Write	Generate check word	L	L	Input	H	X	Output check bits†	L	H	H

†See Table 2 for details on check bit generation.

memory write cycle details

During a memory write cycle, the check bits (CB0 thru CB6) are generated internally in the EDAC by seven 16-input parity generators using the 32-bit data word as defined in Table 2. These seven check bits are stored in memory along with the original 32-bit data word. This 32-bit word will later be used in the memory read cycle for error detection and correction.

TABLE 2. PARITY ALGORITHM

CHECK WORD	32-BIT DATA WORD																													
BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CB0	X		X	X		X					X		X	X	X			X			X		X	X	X	X		X				X
CB1				X		X		X		X		X		X	X	X				X		X		X		X		X		X	X	X
CB2	X		X			X	X		X			X	X			X	X		X				X	X		X			X	X		X
CB3			X	X	X				X	X	X				X	X			X	X	X				X	X	X			X	X
CB4	X	X							X	X	X	X	X	X			X	X							X	X	X	X	X	X		
CB5	X	X	X	X	X	X	X	X									X	X	X	X	X	X	X	X								
CB6	X	X	X	X	X	X	X	X																	X	X	X	X	X	X	X	X

The seven check bits are parity bits derived from the matrix of data bits as indicated by "X" for each bit.

error detection and correction details

During a memory read cycle, the 7-bit check word is retrieved along with the actual data. In order to be able to determine whether the data from memory is acceptable to use as presented to the bus, the error flags must be tested to determine if they are at the high level.

The first case in Table 3 represents the normal, no-error conditions. The EDAC presents highs on both flags. The next two cases of single-bit errors give a high on $\overline{MERR}$ and a low on $\overline{ERR}$, which is the signal for a correctable error, and the EDAC should be sent through the correction cycle. The last three cases of double-bit errors will cause the EDAC to signal lows on both $\overline{ERR}$ and $\overline{MERR}$, which is the interrupt indication for the CPU.

TABLE 3. ERROR FUNCTION

Total Number of Errors		Error Flags		Data Correction
32-Bit Data Word	7-Bit Check Word	$\overline{ERR}$	$\overline{MERR}$	
0	0	H	H	Not applicable
1	0	L	H	Correction
0	1	L	H	Correction
1	1	L	L	Interrupt
2	0	L	L	Interrupt
0	2	L	L	Interrupt

Error detection is accomplished as the 7-bit check word and the 32-bit data word from memory are applied to internal parity generators/checkers. If the parity of all seven groupings of data and check bits are correct, it is assumed that no error has occurred and both error flags will be high.

If the parity of one or more of the check groups is incorrect, an error has occurred and the proper error flag or flags will be set low. Any single error in the 32-bit data word will change the state of either three or five bits of the 7-bit check word. Any single error in the 7-bit check word changes the state of only that one bit. In either case, the single error flag ($\overline{ERR}$) will be set low while the dual error flag ($\overline{MERR}$) will remain high.

Any two-bit error will change the state of an even number of check bits. The two-bit error is not correctable since the parity tree can only identify single-bit errors. Both error flags are set low when any two-bit error is detected.

Three or more simultaneous bit errors can cause the EDAC to believe that no error, a correctable error, or an uncorrectable error has occurred and will produce erroneous results in all three cases. It should be noted that the gross-error conditions of all lows and all highs will be detected.

TABLE 4. READ, FLAG, AND CORRECT FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB CONTROL $\overline{OEBn}$ OR $\overline{OEDB}$	DB OUTPUT LATCH ('ALS632A, 'ALS633) $\overline{LEDBO}$	CHECK I/O	CB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$ $\overline{MERR}$
Read	Read & flag	H	L	Input	H	X	Input	H	Enabled†
Read	Latch input data & check bits	H	H	Latched input data	H	L	Latched input check word	H	Enabled†
Read	Output corrected data & syndrome bits	H	H	Output corrected data word	L	X	Output syndrome bits‡	L	Enabled†

†See Table 3 for error description.
‡See Table 5 for error location.

As the corrected word is made available on the data I/O port (DB0 thru DB31), the check word I/O port (CB0 thru CB6) presents a 7-bit syndrome error code. This syndrome error code can be used to locate the bad memory chip. See Table 5 for syndrome decoding.

TABLE 5. SYNDROME DECODING

SYNDROME BITS							ERROR
6	5	4	3	2	1	0	
L	L	L	L	L	L	L	unc
L	L	L	L	L	L	H	2-bit
L	L	L	L	L	H	L	2-bit
L	L	L	L	L	H	H	unc
L	L	L	L	H	L	L	2-bit
L	L	L	L	H	L	H	unc
L	L	L	L	H	H	L	unc
L	L	L	L	H	H	H	2-bit
L	L	L	H	L	L	L	2-bit
L	L	L	H	L	L	H	unc
L	L	L	H	L	H	L	DB31
L	L	L	H	L	H	H	2-bit
L	L	L	H	H	L	L	unc
L	L	L	H	H	L	H	2-bit
L	L	L	H	H	H	L	2-bit
L	L	L	H	H	H	H	DB30
L	L	H	L	L	L	L	2-bit
L	L	H	L	L	L	H	unc
L	L	H	L	L	H	L	DB29
L	L	H	L	L	H	H	2-bit
L	L	H	L	H	L	L	DB28
L	L	H	L	H	L	H	2-bit
L	L	H	L	H	H	L	2-bit
L	L	H	L	H	H	H	DB27
L	L	H	H	L	L	L	DB26
L	L	H	H	L	L	H	2-bit
L	L	H	H	L	H	L	2-bit
L	L	H	H	L	H	H	DB25
L	L	H	H	H	L	L	2-bit
L	L	H	H	H	L	H	DB24
L	L	H	H	H	H	L	unc
L	L	H	H	H	H	H	2-bit

SYNDROME BITS							ERROR
6	5	4	3	2	1	0	
L	H	L	L	L	L	L	2-bit
L	H	L	L	L	L	H	unc
L	H	L	L	L	H	L	DB7
L	H	L	L	L	H	H	2-bit
L	H	L	L	H	L	L	DB6
L	H	L	L	H	L	H	2-bit
L	H	L	L	H	H	L	2-bit
L	H	L	L	H	H	H	DB5
L	H	L	H	L	L	L	DB4
L	H	L	H	L	L	H	2-bit
L	H	L	H	L	H	L	2-bit
L	H	L	H	L	H	H	DB3
L	H	L	H	H	L	L	2-bit
L	H	L	H	H	L	H	DB2
L	H	L	H	H	H	L	unc
L	H	L	H	H	H	H	2-bit
L	H	H	L	L	L	L	DB0
L	H	H	L	L	L	H	2-bit
L	H	H	L	L	H	L	2-bit
L	H	H	L	L	H	H	unc
L	H	H	L	H	L	L	2-bit
L	H	H	L	H	L	H	DB1
L	H	H	L	H	H	L	unc
L	H	H	L	H	H	H	2-bit
L	H	H	H	L	L	L	2-bit
L	H	H	H	L	L	H	unc
L	H	H	H	L	H	L	unc
L	H	H	H	L	H	H	2-bit
L	H	H	H	H	L	L	unc
L	H	H	H	H	L	H	2-bit
L	H	H	H	H	H	L	2-bit
L	H	H	H	H	H	H	CB6

SYNDROME BITS							ERROR
6	5	4	3	2	1	0	
H	L	L	L	L	L	L	2-bit
H	L	L	L	L	L	H	unc
H	L	L	L	L	H	L	unc
H	L	L	L	L	H	H	2-bit
H	L	L	L	H	L	L	unc
H	L	L	L	H	L	H	2-bit
H	L	L	L	H	H	L	2-bit
H	L	L	L	H	H	H	unc
H	L	L	H	L	L	L	unc
H	L	L	H	L	L	H	2-bit
H	L	L	H	L	H	L	2-bit
H	L	L	H	L	H	H	DB15
H	L	L	H	H	L	L	2-bit
H	L	L	H	H	L	H	unc
H	L	L	H	H	H	L	DB14
H	L	L	H	H	H	H	2-bit
H	L	H	L	L	L	L	unc
H	L	H	L	L	L	H	2-bit
H	L	H	L	L	H	L	2-bit
H	L	H	L	L	H	H	DB13
H	L	H	L	H	L	L	2-bit
H	L	H	L	H	L	H	DB12
H	L	H	L	H	H	L	DB11
H	L	H	L	H	H	H	2-bit
H	L	H	H	L	L	L	2-bit
H	L	H	H	L	L	H	DB10
H	L	H	H	L	H	L	DB9
H	L	H	H	L	H	H	2-bit
H	L	H	H	H	L	L	DB8
H	L	H	H	H	L	H	2-bit
H	L	H	H	H	H	L	2-bit
H	L	H	H	H	H	H	CB5

SYNDROME BITS							ERROR
6	5	4	3	2	1	0	
H	H	L	L	L	L	L	unc
H	H	L	L	L	L	H	2-bit
H	H	L	L	L	H	L	2-bit
H	H	L	L	L	H	H	DB23
H	H	L	L	H	L	L	2-bit
H	H	L	L	H	L	H	DB22
H	H	L	L	H	H	L	DB21
H	H	L	L	H	H	H	2-bit
H	H	L	H	L	L	L	2-bit
H	H	L	H	L	L	H	DB20
H	H	L	H	L	H	L	DB19
H	H	L	H	L	H	H	2-bit
H	H	L	H	H	L	L	DB18
H	H	L	H	H	L	H	2-bit
H	H	L	H	H	H	L	2-bit
H	H	L	H	H	H	H	CB4
H	H	H	L	L	L	L	2-bit
H	H	H	L	L	L	H	DB16
H	H	H	L	L	H	L	unc
H	H	H	L	L	H	H	2-bit
H	H	H	L	H	L	L	DB17
H	H	H	L	H	L	H	2-bit
H	H	H	L	H	H	L	2-bit
H	H	H	L	H	H	H	CB3
H	H	H	H	L	L	L	unc
H	H	H	H	L	L	H	2-bit
H	H	H	H	L	H	L	2-bit
H	H	H	H	L	H	H	CB2
H	H	H	H	H	L	L	2-bit
H	H	H	H	H	L	H	CB1
H	H	H	H	H	H	L	CB0
H	H	H	H	H	H	H	none

CB X = error in check bit X
DB Y = error in data bit Y
2-bit = double-bit error
unc = uncorrectable multibit error

read-modify-write (byte control) operations

The 'ALS632A and 'ALS633 devices are capable of byte-write operations. The 39-bit word from memory must first be latched into the DB and CB input latches. This is easily accomplished by switching from the read and flag mode (S1 = H, S0 = L) to the latch input mode (S1 = H, S0 = H). The EDAC will then make any corrections, if necessary, to the data word and place it at the input of the output data latch. This data word must then be latched into the output data latch by taking $\overline{\text{LEDBO}}$ from a low to a high.

Byte control can now be employed on the data word through the $\overline{\text{OEB}}$0 through $\overline{\text{OEB}}$3 controls. $\overline{\text{OEB}}$0 controls DB0-DB7 (byte 0), $\overline{\text{OEB}}$1 controls DB8-DB15 (byte 1), $\overline{\text{OEB}}$2 controls DB16-DB23 (byte 2), and $\overline{\text{OEB}}$3 controls DB24-DB31 (byte 3). Placing a high on the byte control will disable the output and the user can modify the byte. If a low is placed on the byte control, then the original byte is allowed to pass onto the data bus unchanged. If the original data word is altered through byte control, a new check word must be generated before it is written back into memory. This is easily accomplished by taking control S1 and S0 low. Table 6 lists the read-modify-write functions.

TABLE 6. READ-MODIFY-WRITE FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1	CONTROL S0	BYTEn†	$\overline{OEB}$n†	DB OUTPUT LATCH $\overline{LEDBO}$	CHECK I/O	CB CONTROL	ERROR FLAG $\overline{ERR}$	ERROR FLAG $\overline{MERR}$
Read	Read & Flag	H	L	Input	H	X	Input	H	Enabled	
Read	Latch input data & check bits	H	H	Latched Input data	H	L	Latched input check word	H	Enabled	
Read	Latch corrected data word into output latch	H	H	Latched output data word	H	H	Hi-Z	H	Enabled	
							Output Syndrome bits	L		
Modify /write	Modify appropriate byte or bytes & generate new check word	L	L	Input modified BYTE0	H	H	Output check word	L	H	H
				Output unchanged BYTE0	L					

†$\overline{OEB}$0 controls DB0-DB7 (BYTE0), $\overline{OEB}$1 controls DB8-DB15 (BYTE1), $\overline{OEB}$2 controls DB16-DB23 (BYTE2), $\overline{OEB}$3 controls DB24-DB31 (BYTE3).

diagnostic operations

The 'ALS632A and 'ALS633 thru 'ALS635 are capable of diagnostics that allow the user to determine whether the EDAC or the memory is failing. The diagnostic function tables will help the user to see the possibilities for diagnostic control.

In the diagnostic mode (S1 = L, S0 = H), the checkword is latched into the input latch while the data input latch remains transparent. This lets the user apply vaious data words against a fixed known checkword. If the user applies a diagnostic data word with an error in any bit location, the $\overline{ERR}$ flag should be low. If a diagnostic data word with two errors in any bit location is applied, the $\overline{MERR}$ flag should be low. After the checkword is latched into the input latch, it can be verified by taking $\overline{OECB}$ low. This outputs the latched checkword. With the 'ALS632A and 'ALS633, the diagnostic data word can be latched into the output data latch and verified. It should be noted that the 'ALS634 and 'ALS635 do not have this pass-through capability because they do not contain an output data latch. By changing from the diagnostic mode (S1 = L, S0 = H) to the correction mode (S1 = H, S0 = H), the user can verify that the EDAC will correct the diagnostic data word. Also, the syndrome bits can be produced to verify that the EDAC pinpoints the error location. Table 7 ('ALS632A and 'ALS633) and Table 8 ('ALS634 and 'ALS635) list the diagnostic functions.

TABLE 7. 'ALS632A, 'ALS633 DIAGNOSTIC FUNCTION

EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB BYTE CONTROL $\overline{OEBn}$	DB OUTPUT LATCH $\overline{LEDBO}$	CHECK I/O	CB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$	ERROR FLAGS $\overline{MERR}$
Read & flag	H	L	Input correct data word	H	X	Input correct check bits	H	H	H
Latch input check word while data input latch remains transparent	L	H	Input diagnostic data word†	H	L	Latched input check bits	H	Enabled	
Latch diagnostic data word into output latch	L	H	Input diagnostic data word†	H	H	Output latched check bits	L	Enabled	
						Hi-Z	H		
Latch diagnostic data word into input latch	H	H	Latched input diagnostic data word	H	H	Output syndrome bits	L	Enabled	
						Hi-Z	H		
Output diagnostic data word & syndrome bits	H	H	Output diagnostic data word	L	H	Output syndrome bits	L	Enabled	
						Hi-Z	H		
Output corrected diagnostic data word & output syndrome bits	H	H	Output corrected diagnostic data word	L	L	Output syndrome bits	L	Enabled	
						Hi-Z	H		

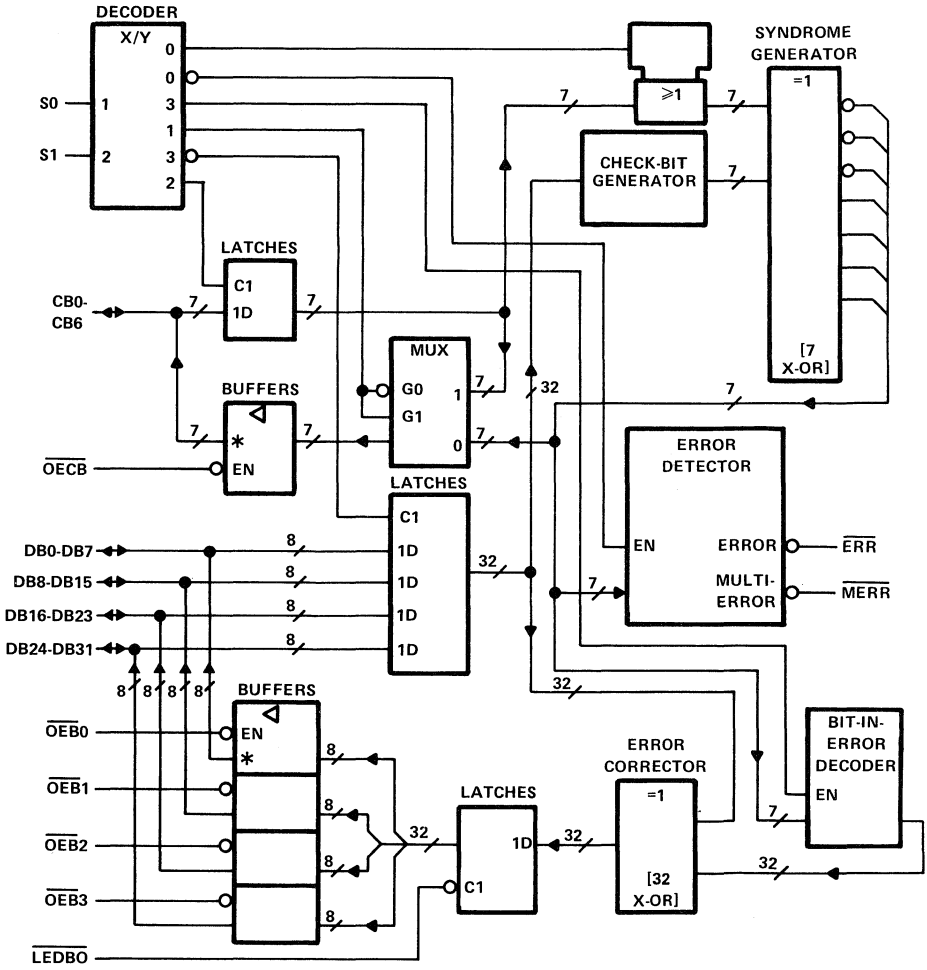
†Diagnostic data is a data word with an error in one bit location except when testing the $\overline{MERR}$ error flag. In this case, the diagnostic data word will contain errors in two bit locations.

TABLE 8. 'ALS634, 'ALS635 DIAGNOSTIC FUNCTION

EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB CONTROL $\overline{OEDB}$	CHECK I/O	DB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$	ERROR FLAGS $\overline{MERR}$
Read & flag	H	L	Input correct data word	H	Input correct check bits	H	H	H
Latch input check bits while data input latch remains transparent	L	H	Input diagnostic data word†	H	Latched input check bits	H	Enabled	
Output input check bits	L	H	Input diagnostic data word†	H	Output input check bits	L	Enabled	
Latch diagnostic data into input latch	H	H	Latched input diagnostic data word	H	Output syndrome bits	L	Enabled	
					Hi-Z	H		
Output corrected diagnostic data word	H	H	Output corrected diagnostic data word	L	Output syndrome bits	L	Enabled	
					Hi-Z	H		

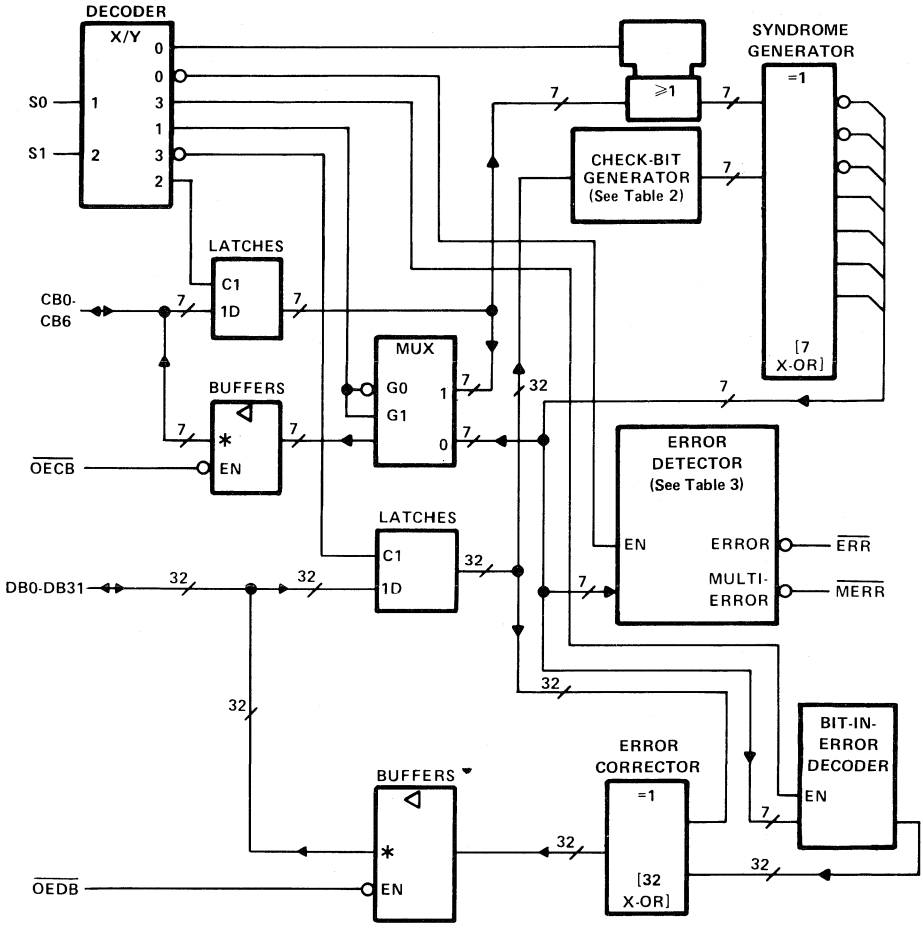
†Diagnostic data is a data word with an error in one bit location except when testing the $\overline{MERR}$ error flag. In this case, the diagnostic data word will contain errors in two bit locations.

'ALS632A, 'ALS633 logic diagram (positive logic)



*'ALS632A has 3-state (▽) check-bit and data outputs.
'ALS633 has open-collector (◇) check-bit and data outputs.

'ALS634, 'ALS635 logic diagram (positive logic)



*'ALS634 has 3-state (▽) check-bit and data outputs.
'ALS635 has open-collector (◇) check-bit and data outputs.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: CB and DB . . . . . 5.5 V
All others . . . . . 7 V
Operating free-air temperature range: SN54ALS632A, SN54ALS633 thru SN54ALS635 . . . . −55°C to 125°C
SN74ALS632A, SN74ALS633 thru SN74ALS635 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS632A SN54ALS633 THRU SN54ALS635			SN74ALS632A SN54ALS633 THRU SN74ALS635			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	$\overline{ERR}$ or $\overline{MERR}$			−0.4			−0.4	mA
		DB or CB | 'ALS632A, 'ALS634			−1			−2.6	
I_{OL}	Low-level output current	$\overline{ERR}$ or $\overline{MERR}$			4			8	mA
		DB or CB			12			24	
t_w	Pulse duration	$\overline{LEDBO}$ low	25			25			ns
t_{su}	Setup time	(1) Data and check word before S0↑ (S1 = H)	15			10			ns
		(2) S0 high before $\overline{LEDBO}$↑ (S1 = H)†	45			45			
		(3) $\overline{LEDBO}$ high before the earlier of S0↓ or S1↓†	0			0			
		(4) $\overline{LEDBO}$ high before S1↑ (S0 = H)	0			0			
		(5) Diagnostic data word before S1↑ (S0 = H)	15			10			
		(6) Diagnostic check word before the later of S1↓ or S0↑	15			10			
		(7) Diagnostic data word before $\overline{LEDBO}$↑ (S1 = L and S0 = H)‡	25			20			
t_h	Hold time	(8) Read-mode, S0 low and S1 high	35			30			ns
		(9) Data and check word after S0↑ (S1 = H)	20			15			
		(10) Data word after S1↑ (S0 = H)	20			15			
		(11) Check word after the later of S1↓ or S0↑	20			15			
		(12) Diagnostic data word after $\overline{LEDBO}$↑ (S1 = L and S0 = H)‡	0			0			
t_{corr}	Correction time (see Figure 1)		65			58			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

†These times ensure that corrected data is saved in the output data latch.
‡These times ensure that the diagnostic data word is saved in the output data latch.

'ALS632A, 'ALS634 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS632A SN54ALS634			SN74ALS632A SN74ALS634			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
	DB or CB	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
	DB or CB	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	S0 or S1	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	All others	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	S0 or S1	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	All others‡					20			20	
I_{IL}	S0 or S1	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.4			−0.4	mA
	All others‡					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		150	250		150	250	mA

'ALS633, 'ALS635 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS633 SN54ALS635			SN74ALS633 SN74ALS635			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
I_{OH}	DB or CB	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
	DB or CB	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	S0 or S1	V_{CC} = 5.5 V,	V_I = 7 V							mA
	All others	V_{CC} = 5.5 V,	V_I = 5.5 V							
I_{IH}	S0 or S1	V_{CC} = 5.5 V,	V_I = 2.7 V							μA
	All others‡									
I_{IL}	S0 or S1	V_{CC} = 5.5 V,	V_I = 0.4 V							mA
	All others‡									
I_O§	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		150			150		mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡For I/O ports (Q_A through Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

NOTE 1: I_{CC} is measured with S0 and S1 at 4.5 V and all CB and DB pins grounded.

Additional information on these products can be obtained from the factory as it becomes available.

'ALS632A switching characteristics, V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_A = MIN to MAX (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ALS632A		SN74ALS632A		UNIT
				MIN	MAX	MIN	MAX	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500 Ω	10	43	10	40	ns
	DB	$\overline{ERR}$	S1 = L, S0 = H, R_L = 500 Ω	10	43	10	40	
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500 Ω	15	67	15	55	ns
	DB	$\overline{MERR}$	S1 = L, S0 = H, R_L = 500 Ω	15	67	15	55	
t_{pd}	S0↓ and S1↓	CB	R1 = R2 = 500 Ω	10	60	10	48	ns
t_{pd}	DB	CB	S1 = L, S0 = L, R1 = R2 = 500 Ω	10	60	10	48	ns
t_{pd}	$\overline{LEDBO}$↓	DB	S1 = X, S0 = H, R1 = R2 = 500 Ω	7	35	7	30	ns
t_{pd}	S1↑	CB	S0 = H, R1 = R2 = 500 Ω	10	60	10	50	ns
t_{en}	$\overline{OECB}$↓	CB	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	30	2	25	ns
t_{dis}	$\overline{OECB}$↑	CB	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	30	2	25	ns
t_{en}	$\overline{OEB0}$ thru $\overline{OEB3}$↓	DB	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	30	2	25	ns
t_{dis}	$\overline{OEB0}$ thru $\overline{OEB3}$↑	DB	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	30	2	25	ns

'ALS633 switching characteristics, V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_A = MIN to MAX (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ALS633			SN74ALS633			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500 Ω		26			26		ns
	DB	$\overline{ERR}$	S1 = L, S0 = H, R_L = 500 Ω		26			26		
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500 Ω		40			40		ns
			S1 = L, S0 = H, R_L = 500 Ω		40			40		
t_{pd}	S0↓ and S1↓	CB	R_L = 680 Ω		40			40		ns
t_{pd}	DB	CB	S1 = L, S0 = L, R_L = 680 Ω		40			40		ns
t_{pd}	$\overline{LEDBO}$↓	DB	S1 = X, S0 = H, R_L = 680 Ω		26			26		ns
t_{pd}	S1↑	CB	S0 = H, R_L = 680 Ω		40			40		ns
t_{PLH}	$\overline{OECB}$↑	CB	S1 = X, S0 = H, R_L = 680 Ω		24			24		ns
t_{PHL}	$\overline{OECB}$↓	CB	S1 = X, S0 = H, R_L = 680 Ω		24			24		ns
t_{PLH}	$\overline{OEB0}$ thru $\overline{OEB3}$↑	DB	S1 = X, S0 = H, R_L = 680 Ω		24			24		ns
t_{PHL}	$\overline{OEB0}$ thru $\overline{OEB3}$↓	DB	S1 = X, S0 = H, R_L = 680 Ω		24			24		ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

Additional information on these products can be obtained from the factory as it becomes available.

'ALS634 switching characteristics, V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_A = MIN to MAX

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ALS634			SN74ALS634			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500 Ω		26			26		ns
			S1 = L, S0 = H, R_L = 500 Ω		26			26		
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500 Ω		40			40		ns
			S1 = L, S0 = H, R_L = 500 Ω		40			40		
t_{pd}	S0↓ and S1↓	CB	R1 = R2 = 500 Ω		35			35		ns
t_{pd}	DB	CB	S1 = L, S0 = L, R1 = R2 = 500 Ω		35			35		ns
t_{pd}	S1↑	CB	S0 = H, R1 = R2 = 500 Ω		35			35		ns
t_{en}	$\overline{OECB}$↓	CB	S1 = X, S0 = H, R1 = R2 = 500 Ω		18			18		ns
t_{dis}	$\overline{OECB}$↑	CB	S1 = X, S0 = H, R1 = R2 = 500 Ω		18			18		ns
t_{en}	$\overline{OECB}$↓	DB	S1 = X, S0 = H, R1 = R2 = 500 Ω		18			18		ns
t_{dis}	$\overline{OECB}$↑	DB	S1 = X, S0 = H, R1 = R2 = 500 Ω		18			18		ns

'ALS635 switching characteristics, V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_A = MIN to MAX

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ALS635			SN74ALS635			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500 Ω		26			26		ns
	DB	$\overline{ERR}$	S1 = L, S0 = H, R_L = 500 Ω		26			26		
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500 Ω		40			40		ns
			S1 = L, S0 = H, R_L = 500 Ω		40			40		
t_{pd}	S0↓ and S1↓	CB	R_L = 680 Ω		40			40		ns
t_{pd}	DB	CB	S1 = L, S0 = L, R_L = 680 Ω		40			40		ns
t_{pd}	S1↑	DB	S0 = H, R_L = 680 Ω		40			40		ns
t_{PLH}	$\overline{OECB}$↑	CB	S1 = X, S0 = H, R_L = 680 Ω		24			24		ns
t_{PHL}	$\overline{OECB}$↓	CB	S1 = X, S0 = H, R_L = 680 Ω		24			24		ns
t_{PLH}	$\overline{OEDB}$↑	DB	S1 = X, S0 = H, R_L = 680 Ω		24			24		ns
t_{PHL}	$\overline{OEDB}$↓	DB	S1 = X, S0 = H, R_L = 680 Ω		24			24		ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

Additional information on these products can be obtained from the factory as it becomes available.

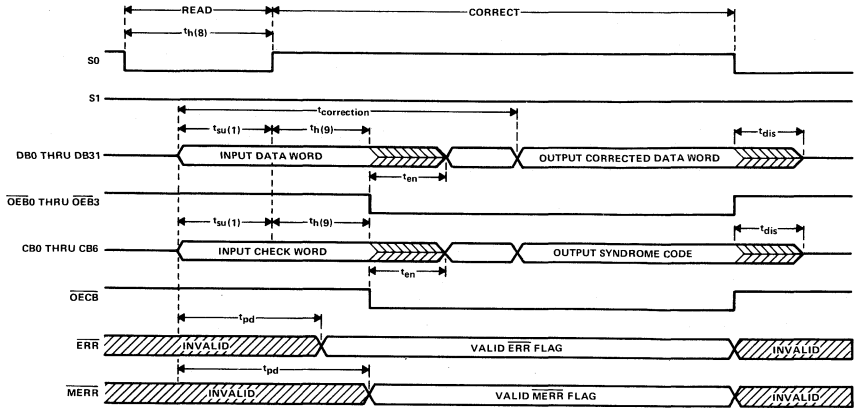


FIGURE 1. READ, FLAG, AND CORRECT MODE SWITCHING WAVEFORMS

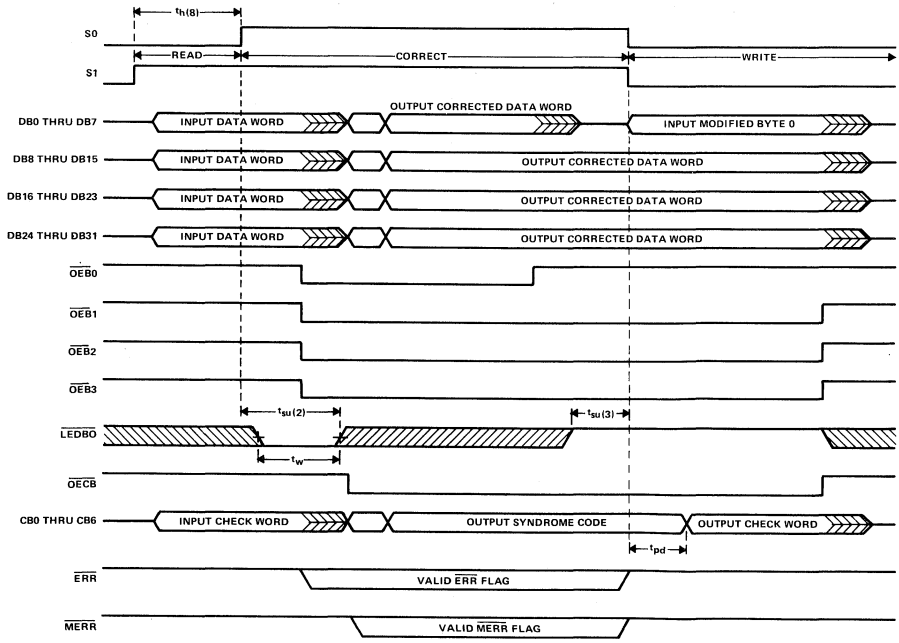


FIGURE 2. READ, CORRECT, MODIFY MODE SWITCHING WAVEFORMS

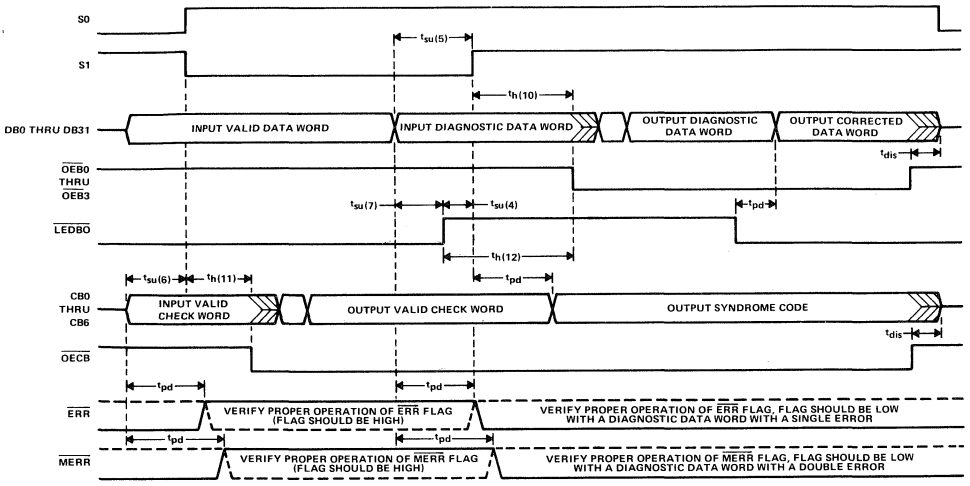
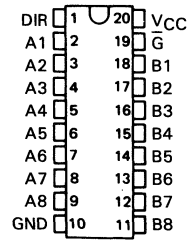


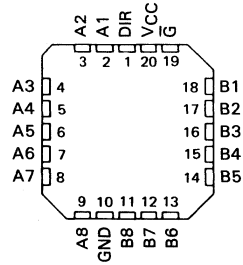
FIGURE 3. DIAGNOSTIC MODE SWITCHING WAVEFORM

- **Bidirectional Bus Transceivers in High-Density 20-Pin Packages**
- **Choice of True or Inverting Logic**
- **A Bus Outputs are Open-Collector; B Bus Outputs are 3-State**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . N PACKAGE
SN74ALS', SN74AS' . . . DW PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FH OR FK PACKAGE
SN74ALS', SN74AS' . . . FN PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between open-collector and 3-state buses. The devices transmit data from the A bus (open-collector) to the B bus (3-state) or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so the buses are isolated.

DEVICE	A OUTPUT	B OUTPUT	LOGIC
'ALS638A, 'AS638	Open-Collector	3-State	Inverting
'ALS639A, 'AS639	Open-Collector	3-State	True

The –1 versions of the SN74ALS' parts are identical to the standard versions except that recommended maximum of I_{OL} is increased to 48 milliamperes. There are no –1 versions of the SN54ALS' parts.

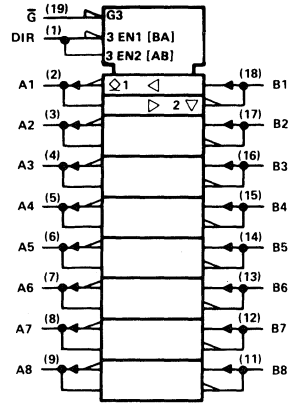
The SN54' family is characterized for operation over the full military temperature range of –55 °C to 125 °C. The SN74' family is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE

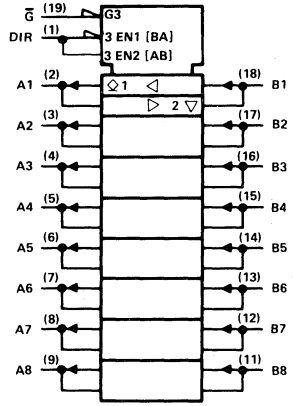
CONTROL INPUTS		OPERATION	
$\overline{G}$	DIR	'ALS638A 'AS638	'ALS639A 'AS639
L	L	$\overline{B}$ data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus
H	X	Isolation	Isolation

logic symbols

'ALS638A, 'AS638



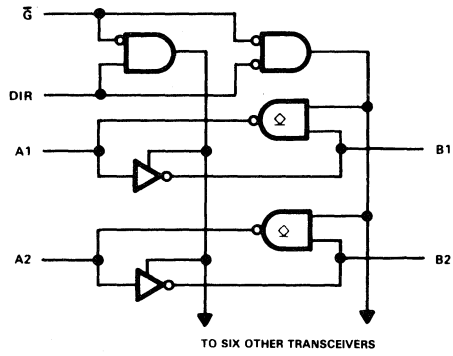
'ALS639A, 'AS639



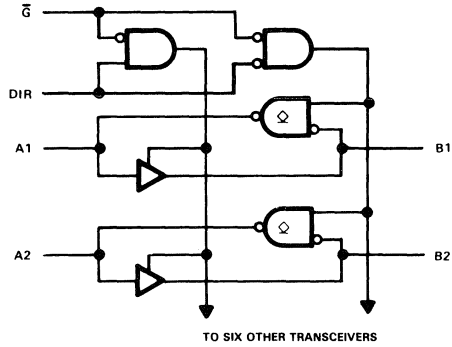
Pin numbers shown are for J and N packages.

functional block diagrams (positive logic)

'ALS638A, 'AS638



'ALS639A, 'AS639



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
A bus I/O ports . . . . . 7 V
B bus I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS638A, SN54ALS639A . . . . . −55°C to 125°C
SN74ALS638A, SN74ALS639A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS638A SN54ALS639A			SN74ALS638A SN74ALS639A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{OH}	High-level output voltage	A ports			5.5			5.5	V
I_{OH}	High-level output current	B ports			−12			−15	mA
I_{OL}	Low-level output current	A or B ports			12			24	mA
								48†	
T_A	Operating free-air temperature		−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS638A-1 and SN74ALS639A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS638A SN54ALS639A			SN74ALS638A SN74ALS639A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	A ports	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OH}	B ports	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	A or B ports	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports§					−0.1			−0.1	
I_O¶	B ports	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS638A	V_{CC} = 5.5 V	Outputs high		18	36		18	30	mA
			Outputs low		25	48		26	41	
			Outputs disabled		16	35		16	30	
	'ALS639A		Outputs high		25	45		25	40	
			Outputs low		30	55		30	50	
			Outputs disabled		33	60		33	54	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS638A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω (A outputs), R1 = R2 = 500 Ω (B outputs), T_A = MIN to MAX				UNIT
			SN54ALS638A		SN74ALS638A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2	15	2	12	ns
t_{PHL}			2	15	2	12	
t_{PLH}	B	A	8	30	8	25	ns
t_{PHL}			8	35	8	30	
t_{PLH}	$\overline{G}$	A	5	30	5	25	ns
t_{PHL}			10	50	10	45	
t_{PZH}	$\overline{G}$	B	5	25	5	20	ns
t_{PZL}			5	28	5	22	
t_{PHZ}	$\overline{G}$	B	2	12	2	10	ns
t_{PLZ}			3	18	3	15	

'ALS639A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω (A outputs), R1 = R2 = 500 Ω (B outputs), T_A = MIN to MAX				UNIT
			SN54ALS639A		SN74ALS639A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2	15	2	12	ns
t_{PHL}			2	15	2	12	
t_{PLH}	B	A	10	35	10	30	ns
t_{PHL}			5	28	5	22	
t_{PLH}	$\overline{G}$	A	10	35	10	30	ns
t_{PHL}			10	40	10	35	
t_{PZH}	$\overline{G}$	B	6	28	6	21	ns
t_{PZL}			8	30	8	25	
t_{PHZ}	$\overline{G}$	B	2	12	2	10	ns
t_{PLZ}			3	19	3	16	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
A bus I/O ports . . . . . 7 V
B bus I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54AS638, SN54AS639 . . . . . −55°C to 125°C
SN74AS638, SN74AS639 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS638 SN54AS639			SN74AS638 SN74AS639			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{OH}	High-level output voltage	A ports			5.5			5.5	V
I_{OH}	High-level output current	B ports			−12			−15	mA
I_{OL}	Low-level output current	A or B ports			48			64	mA
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS638 SN54AS639			SN74AS638 SN74AS639			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}	A ports	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OH}	B ports	V_{CC} = 4.5 V, to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4			
V_{OL}	A or B ports	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.3	0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA					0.35	0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					50			50	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A or B ports‡					−0.75			−0.75	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS638	V_{CC} = 5.5 V	Outputs high		24	40		24	40	mA
			Outputs low		75	122		75	122	
			Outputs disabled		37	61		37	61	
	'AS639		Outputs high		56	92		56	92	
			Outputs low		95	154		95	154	
			Outputs disabled		62	100		62	100	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS638 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω (A outputs), R1 = R2 = 500 Ω (B outputs), T_A = MIN to MAX				UNIT
			SN54AS638		SN74AS638		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2	8	2	7	ns
t_{PHL}			2	7.5	2	6.5	
t_{PLH}	B	A	5	23	5	20	ns
t_{PHL}			2	8	2	7	
t_{PLH}	$\overline{G}$	A	5	20	5	19	ns
t_{PHL}			2	10	2	9	
t_{PZH}	$\overline{G}$	B	2	10	2	8	ns
t_{PZL}			2	12	2	10	
t_{PHZ}	$\overline{G}$	B	2	8	2	7	ns
t_{PLZ}			2	12	2	10	

'AS639 switching characteristics (see Note 1)

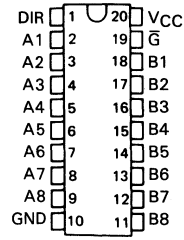
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω (A outputs), R1 = R2 = 500 Ω (B outputs), T_A = MIN to MAX				UNIT
			SN54AS639		SN74AS639		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2	11	2	9.5	ns
t_{PHL}			2	10.5	2	9	
t_{PLH}	B	A	5	25	5	22	ns
t_{PHL}			2	10	2	9	
t_{PLH}	$\overline{G}$	A	5	23	5	21.5	ns
t_{PHL}			2	12.5	2	11.5	
t_{PZH}	$\overline{G}$	B	2	12	2	10.5	ns
t_{PZL}			2	12	2	10.5	
t_{PHZ}	$\overline{G}$	B	2	7.5	2	7	ns
t_{PLZ}			2	12	2	10.5	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

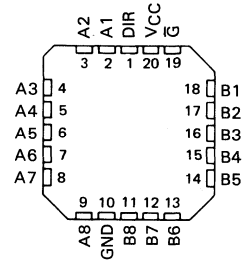
- **Bidirectional Bus Transceivers in High-Density 20-Pin Packages**
- **Choice of True or Inverting Logic**
- **Choice of 3-State or Open-Collector Outputs**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	OUTPUT	LOGIC
'ALS640A, 'AS640	3-State	Inverting
'ALS641A, 'AS641	Open-Collector	True
'ALS642A, 'AS642	Open-Collector	Inverting
'ALS643A, 'AS643	3-State	True and Inverting
'ALS644A, 'AS644	Open-Collector	True and Inverting
'ALS645A, 'AS645	3-State	True

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . N PACKAGE
SN74ALS', SN74AS' . . . DW PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FH OR FK PACKAGE
SN74ALS', SN74AS' . . . FN PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so the buses are effectively isolated.

The –1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no –1 versions of the SN54ALS' parts.

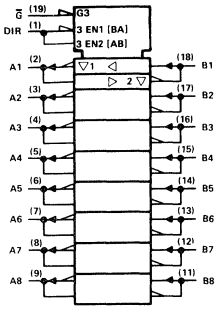
The SN54' family is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

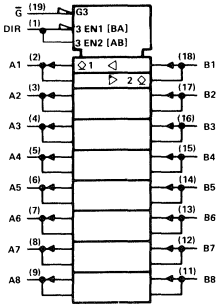
CONTROL INPUTS		OPERATION		
$\overline{G}$	DIR	'ALS640A, 'AS640 'ALS642A, 'AS642	'ALS641A, 'AS641 'ALS645A, 'AS645	'ALS643A, 'AS643 'ALS644A, 'AS644
L	L	$\overline{B}$ data to A bus	B data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus	$\overline{A}$ data to B bus
H	X	Isolation	Isolation	Isolation

logic symbols

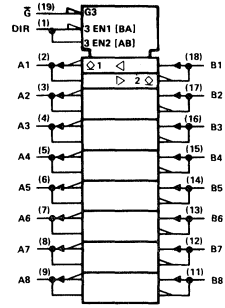
'ALS640A, 'AS640



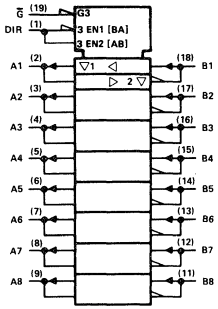
'ALS641A, 'AS641



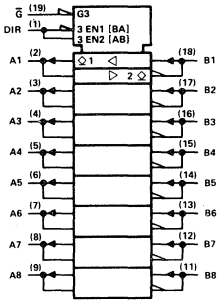
'ALS642A, 'AS642



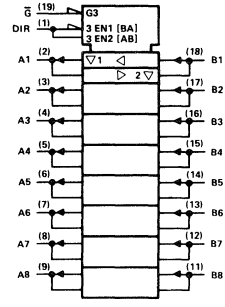
'ALS643A, 'AS643



'ALS644A, 'AS644

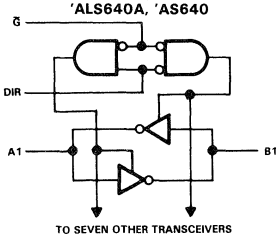


'ALS645A, 'AS645

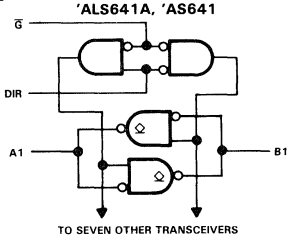


functional block diagrams (positive logic)

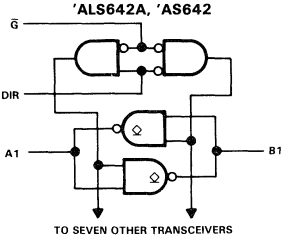
'ALS640A, 'AS640



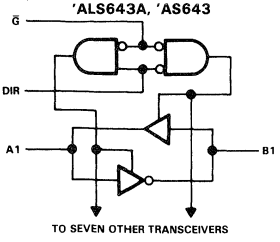
'ALS641A, 'AS641



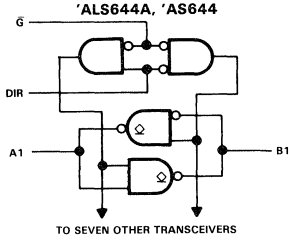
'ALS642A, 'AS642



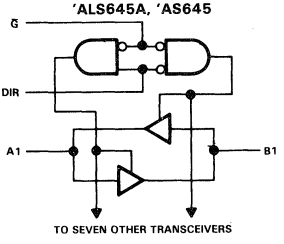
'ALS643A, 'AS643



'ALS644A, 'AS644



'ALS645A, 'AS645



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS640A, SN54ALS643A, SN54ALS645A . . . . . −55°C to 125°C
SN74ALS640A, SN74ALS643A, SN74ALS645A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS640A SN54ALS643A SN54ALS645A			SN74ALS640A SN74ALS643A SN74ALS645A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS640A-1, SN74ALS643A-1, and SN74ALS645A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS'			SN74ALS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports§					−0.1			−0.1	
I_O¶		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS640A	V_{CC} = 5.5 V	Outputs high		19	35		19	30	mA
			Outputs low		27	45		27	40	
			Outputs disabled		28	48		28	43	
	'ALS643A		Outputs high		25	37		25	35	
			Outputs low		33	47		33	45	
			Outputs disabled		35	50		35	48	
	'ALS645A		Outputs high		30	48		30	45	
			Outputs low		36	60		36	55	
			Outputs disabled		38	63		38	58	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS640A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS640A		SN74ALS640A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	14	2	11	ns
t_{PHL}			2	13	2	10	
t_{PZH}	$\overline{G}$	A or B	5	25	5	21	ns
t_{PZL}			8	27	8	24	
t_{PHZ}	$\overline{G}$	A or B	2	12	2	10	ns
t_{PLZ}			3	20	3	15	

'ALS643A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS643A		SN74ALS643A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2	15	2	13	ns
t_{PHL}			2	13	2	11	
t_{PLH}	B	A	2	15	2	13	ns
t_{PHL}			2	13	2	11	
t_{PZH}	$\overline{G}$	A	5	28	5	25	ns
t_{PZL}			5	28	5	25	
t_{PHZ}	$\overline{G}$	A	2	12	2	10	ns
t_{PLZ}			3	22	3	17	
t_{PZH}	$\overline{G}$	B	5	28	5	25	ns
t_{PZL}			5	28	5	25	
t_{PHZ}	$\overline{G}$	B	2	12	2	10	ns
t_{PLZ}			3	22	3	17	

'ALS645A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS645A		SN74ALS645A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	3	15	3	10	ns
t_{PHL}			3	13	3	10	
t_{PZH}	$\overline{G}$	A or B	5	25	5	20	ns
t_{PZL}			5	25	5	20	
t_{PHZ}	$\overline{G}$	A or B	2	12	2	10	ns
t_{PLZ}			4	18	4	15	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs and I/O ports . . . . . 7 V
Operating free-air temperature range: SN54ALS641A, SN54ALS642A, SN54ALS644A . . . . . −55°C to 125°C
SN74ALS641A, SN74ALS642A, SN74ALS644A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS641A SN54ALS642A SN54ALS644A			SN74ALS641A SN74ALS642A SN74ALS644A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 and 5.25 V.
The 48-mA limit applies for the SN74ALS641A−1, SN74ALS642A−1, and SN74ALS644A−1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS641A SN54ALS642A SN54ALS644A			SN74ALS641A SN74ALS642A SN74ALS644A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports§					−0.1			−0.1	
I_{CC}	'ALS641A	V_{CC} = 5.5 V	Outputs high		25	40		25	37	mA
			Outputs low		33	50		33	47	
	'ALS642A		Outputs high		8	15		8	15	
			Outputs low		18	28		18	28	
	'ALS644A		Outputs high		16	32		16	29	
			Outputs low		25	44		25	40	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

'ALS641A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS641A		SN74ALS641A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	5	30	5	25	ns
t_{PHL}			3	23	3	18	
t_{PLH}	$\overline{G}$	A or B	8	35	8	30	ns
t_{PHL}			8	35	8	30	
t_{PLH}	DIR	A or B	8	37	8	32	ns
t_{PHL}			8	37	8	32	

'ALS642A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS642A		SN74ALS642A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	10	35	10	30	ns
t_{PHL}			5	25	5	22	
t_{PLH}	$\overline{G}$ or DIR	A or B	10	35	10	30	ns
t_{PHL}			15	43	15	38	

'ALS644A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS644A		SN74ALS644A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	10	35	10	30	ns
t_{PHL}			5	25	5	22	
t_{PLH}	B	A	10	35	10	30	ns
t_{PHL}			5	23	5	21	
t_{PLH}	$\overline{G}$	A	8	35	8	30	ns
t_{PHL}			10	38	10	35	
t_{PLH}	$\overline{G}$	B	8	31	8	26	ns
t_{PHL}			15	40	15	35	
t_{PLH}	DIR	A	8	31	8	26	ns
t_{PHL}			10	40	10	35	
t_{PLH}	DIR	B	10	35	10	30	ns
t_{PHL}			15	40	15	35	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54AS640, SN54AS643, SN54AS645 . . . . . −55°C to 125°C
SN74AS640, SN74AS643, SN74AS645 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS640 SN54AS643 SN54AS645			SN74AS640 SN74AS643 SN74AS645			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS'			SN74AS'			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.30	0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA					0.35	0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					50			50	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A or B ports‡					−0.75			−0.75	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS640	V_{CC} = 5.5 V	Outputs high		37	58		37	58	mA
			Outputs low		78	123		78	123	
			Outputs disabled		51	80		51	80	
	'AS643		Outputs high		48	79		48	79	
			Outputs low		88	143		88	143	
			Outputs disabled		61	100		61	100	
	'AS645		Outputs high		62	97		62	97	
			Outputs low		95	149		95	149	
			Outputs disabled		79	123		79	123	

†All typical values are at V_{CC} = 5 V, T_A = 25°C
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS640 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS640		SN74AS640		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	8	2	7	ns
t_{PHL}			2	7	2	6	
t_{PZH}	$\overline{G}$	A or B	2	10	2	8	ns
t_{PZL}			2	12	2	10	
t_{PHZ}	$\overline{G}$	A or B	2	9	2	8	ns
t_{PLZ}			2	16	2	13	

'AS643 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS643		SN74AS643		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2	10	2	8	ns
t_{PHL}			2	7.5	2	7	
t_{PLH}	B	A	2	11.5	2	10	ns
t_{PHL}			2	10	2	9	
t_{PZH}	$\overline{G}$	A	2	13	2	11	ns
t_{PZL}			2	13	2	11	
t_{PHZ}	$\overline{G}$	A	2	8.5	2	7.5	ns
t_{PLZ}			2	12	2	10.5	
t_{PZH}	$\overline{G}$	B	2	11.5	2	10	ns
t_{PZL}			2	12	2	10	
t_{PHZ}	$\overline{G}$	B	2	8	2	7	ns
t_{PLZ}			2	12	2	10	

'AS645 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS645		SN74AS645		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	11	2	9.5	ns
t_{PHL}			2	10.5	2	9	
t_{PZH}	$\overline{G}$	A or B	2	12	2	11	ns
t_{PZL}			2	12	2	10	
t_{PHZ}	$\overline{G}$	A or B	2	8	2	7	ns
t_{PLZ}			2	13	2	12	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs and I/O ports . . . . . 7 V
Operating free-air temperature range: SN54AS641, SN54AS642, SN54AS644 . . . . . −55 °C to 125 °C
SN74AS641, SN74AS642, SN74AS644 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS641 SN54AS642 SN54AS644			SN74AS641 SN74AS642 SN74AS644			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS641 SN54AS642 SN54AS644			SN74AS641 SN74AS642 SN74AS644			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.3	0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA					0.35	0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					50			50	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A or B ports‡					−0.75			−0.75	
I_{CC}	'AS641	V_{CC} = 5.5 V	Outputs high		50	82		50	82	mA
			Outputs low		84	136		84	136	
	'AS642		Outputs high		25	42		25	42	
			Outputs low		64	104		64	104	
	'AS644		Outputs high		38	62		38	62	
			Outputs low		76	124		76	124	

†All typical values are at V_{CC} = 5 V, T_A = 25 °C
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

'AS641 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54AS641		SN74AS641		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	5	23	5	21	ns
t_{PHL}			1	8.5	1	7.5	
t_{PLH}	$\overline{G}$	A or B	5	24	5	21	ns
t_{PHL}			1	10	1	9	
t_{PLH}	DIR	A or B	5	26	5	22	ns
t_{PHL}			1	11	1	10	

'AS642 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54AS642		SN74AS642		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	5	28.5	5	24	ns
t_{PHL}			1	8.5	1	7.5	
t_{PLH}	$\overline{G}$	A or B	5	25	5	22	ns
t_{PHL}			1	11	1	10	
t_{PLH}	DIR	A or B	5	26.5	5	23.5	ns
t_{PHL}			1	12.5	1	11.5	

'AS644 switching characteristics (see Note 1)

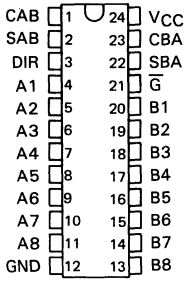
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54AS644		SN74AS644		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	5	28.5	5	24	ns
t_{PHL}			1	8.5	1	7.5	
t_{PLH}	B	A	5	23	5	21	ns
t_{PHL}			1	8.5	1	7.5	
t_{PLH}	$\overline{G}$	A or B	5	24	5	21	ns
t_{PHL}			1	10	1	9	
t_{PLH}	DIR	A or B	5	26	5	22	ns
t_{PHL}			1	11	1	10	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

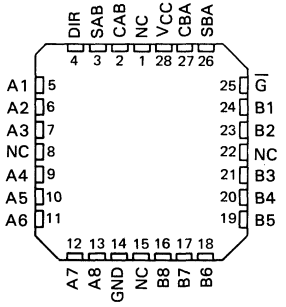
- **Independent Registers for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Choice of True or Inverting Data Paths**
- **Choice of 3-State or Open-Collector Outputs**
- **Included Among the Package Options Are Compact 24-pin 300-mil Wide DIPs and Small Outline (SO) and 28-pin Plastic and Ceramic Chip Carriers**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	OUTPUT	LOGIC
'ALS646, 'AS646	3-State	True
'ALS647	Open-Collector	True
'ALS648, 'AS648	3-State	Inverting
'ALS649	Open-Collector	Inverting

SN54ALS', SN54AS' . . . JT PACKAGE
SN74ALS', SN74AS' . . . NT PACKAGE
SN74ALS', SN74AS' . . . DW PACKAGE
(TOP VIEW)

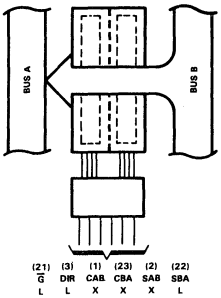


SN54ALS', SN54AS' . . . FH OR FK PACKAGE
SN74ALS', SN74AS' . . . FN PACKAGE
(TOP VIEW)

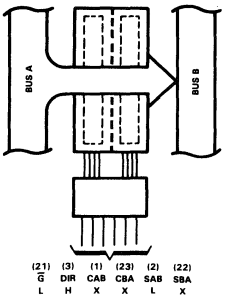


description

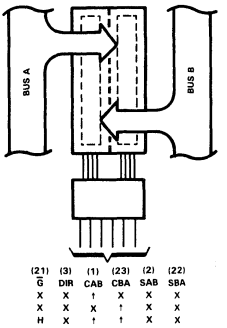
These devices consist of bus transceiver circuits with 3-state or open-collector outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.



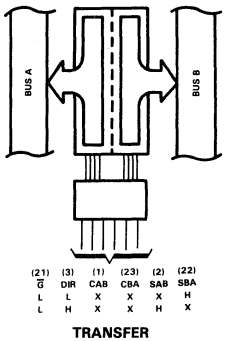
REAL-TIME TRANSFER
BUS B TO BUS A



REAL-TIME TRANSFER
BUS A TO BUS B



STORAGE FROM
A, B, OR A AND B



TRANSFER
STORED DATA
TO A OR B

Enable ($\overline{G}$) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when enable $\overline{G}$ is active (low). In the isolation mode (control $\overline{G}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The –1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no –1 versions of the SN54ALS' parts.

The SN54' family is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74' family is characterized for operation from 0° to 70°C.

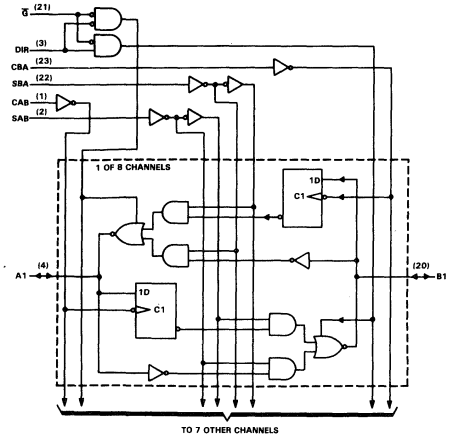
FUNCTION TABLE

INPUTS						DATA I/O*		OPERATION OR FUNCTION	
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'ALS646, 'ALS647 'AS646	'ALS648, 'ALS649 'AS648
X	X	↑	X	X	X	Input	Not specified	Store A, B unspecified	Store A, B unspecified
X	X	X	↑	X	X	Not specified	Input	Store B, A unspecified	Store B, A unspecified
H	X	↑	↑	X	X	Input	Input	Store A and B Data	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time $\overline{B}$ Data to A Bus
L	L	X	X	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time $\overline{A}$ Data to B Bus
L	H	X	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

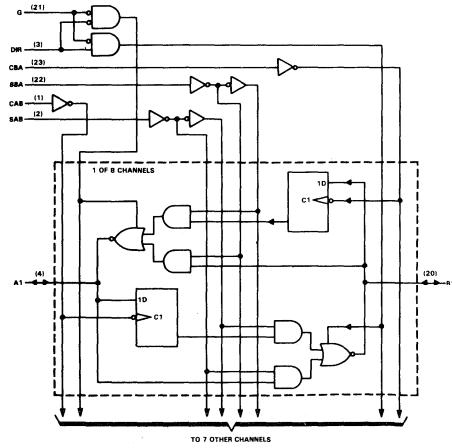
*The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

functional block diagrams (positive logic)

'ALS646, 'AS646, 'ALS647



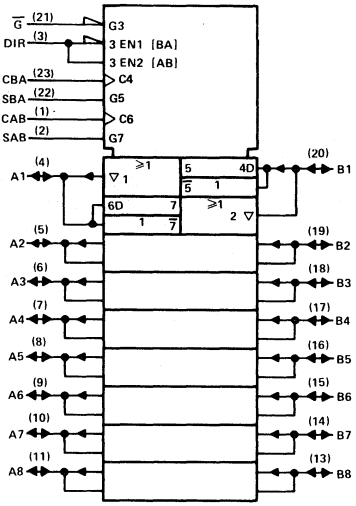
'ALS648, 'AS648, 'ALS649



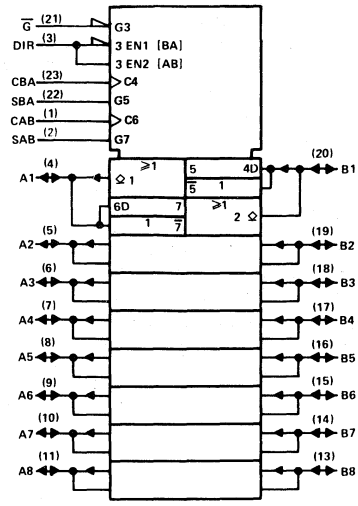
Pin numbers shown are for JT and NT packages.

logic symbols

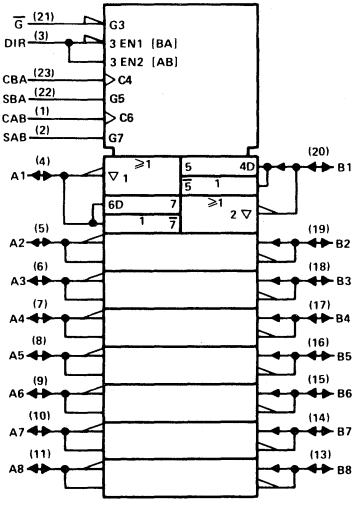
'ALS646, 'AS646



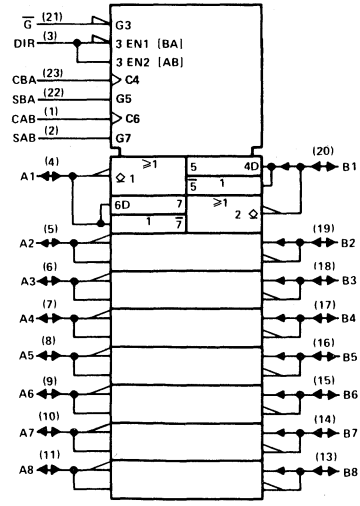
'ALS647



'ALS648, 'AS648



'ALS649



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: Control inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS646, SN54ALS648 . . . . . −55 °C to 125 °C
SN74ALS646, SN74ALS648 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS646 SN54ALS648			SN74ALS646 SN74ALS648			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48†	
f_{clock}	Clock frequency							MHz
t_w	Pulse duration, clocks high or low							ns
t_{su}	Setup time, A before CAB↑ or B before CBA↑							ns
t_h	Hold time, A after CAB↑ or B after CBA↑							ns
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended condition applies if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS646-1 and SN74ALS648-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS646 SN54ALS648			SN74ALS646 SN74ALS648			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports§					−0.2			−0.2	
I_O¶		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS646	V_{CC} = 5.5 V	Outputs high		60			60		mA
			Outputs low		68			68		
			Outputs disabled		68			68		
	'ALS648		Outputs high		52			52		
			Outputs low		57			57		
			Outputs disabled		58			58		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
Additional information on these products can be obtained from the factory as it becomes available.

'ALS646 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS646			SN74ALS646			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}									MHz
t_{PLH}	CBA or CAB	A or B		11			11		ns
t_{PHL}				13			13		
t_{PLH}	A or B	B or A		8			8		ns
t_{PHL}				8			8		
t_{PLH}	SBA or SAB‡ (with A or B high)	A or B		16			16		ns
t_{PHL}				16			16		
t_{PLH}	SBA or SAB‡ (with A or B low)	A or B		15			15		ns
t_{PHL}				12			12		
t_{PZH}	$\overline{G}$	A or B		17			17		ns
t_{PZL}				20			20		
t_{PHZ}	$\overline{G}$	A or B		10			10		ns
t_{PLZ}				12			12		
t_{PZH}	DIR	A or B		17			17		ns
t_{PZL}				20			20		
t_{PHZ}	DIR	A or B		10			10		ns
t_{PLZ}				12			12		

'ALS648 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS648			SN74ALS648			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}									MHz
t_{PLH}	CBA or CAB	A or B		11			11		ns
t_{PHL}				13			13		
t_{PLH}	A or B	B or A		10			10		ns
t_{PHL}				12			12		
t_{PLH}	SBA or SAB‡ (with A or B high)	A or B		16			16		ns
t_{PHL}				16			16		
t_{PLH}	SBA or SAB‡ (with A or B low)	A or B		15			15		ns
t_{PHL}				15			15		
t_{PZH}	$\overline{G}$	A or B		17			17		ns
t_{PZL}				20			20		
t_{PHZ}	$\overline{G}$	A or B		10			10		ns
t_{PLZ}				12			12		
t_{PZH}	DIR	A or B		17			17		ns
t_{PZL}				20			20		
t_{PHZ}	DIR	A or B		10			10		ns
t_{PLZ}				12			12		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
Additional information on these products can be obtained from the factory as it becomes available.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS647, SN54ALS649 . . . . . −55 °C to 125 °C
SN74ALS647, SN74ALS649 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS647 SN54ALS649			SN74ALS647 SN74ALS649			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
							48†	
f_{clock}	Clock frequency							MHz
t_w	Pulse duration, clocks high or low							ns
t_{su}	Setup time, A before CAB↑ or B before CBA↑							ns
t_h	Hold time, A after CAB↑ or B after CBA↑							ns
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended condition applies if V_{CC} is maintained between 4.75 and 5.25 V.
The 48-mA limit applies for the SN74ALS647-1 and SN74ALS649-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS647 SN54ALS649			SN74ALS647 SN74ALS649			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4				V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	
I_{IH}	A or B ports§	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	Control inputs					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports§					−0.2			−0.2	
I_{CC}	'ALS647	V_{CC} = 5.5 V	Outputs high		52			52		mA
			Outputs low		62			62		
	'ALS649		Outputs high		50			50		
			Outputs low		60			60		

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
Additional information on these products can be obtained from the factory as it becomes available.

'ALS647 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX						UNIT
			SN54ALS647			SN74ALS647			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}									MHz
t_{PLH}	CBA or CAB	A or B		24			24		ns
t_{PHL}				15			15		
t_{PLH}	A or B	B or A		24			24		ns
t_{PHL}				12			12		
t_{PLH}	SBA or SAB‡ (with A or B high)	A or B		26			26		ns
t_{PHL}				15			15		
t_{PLH}	SBA or SAB‡ (with A or B low)	A or B		26			26		ns
t_{PHL}				15			15		
t_{PLH}	$\overline{G}$	A or B		24			24		ns
t_{PHL}				17			17		
t_{PLH}	DIR	A or B		24			24		ns
t_{PHL}				17			17		

'ALS649 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX						UNIT
			SN54ALS649			SN74ALS649			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}									MHz
t_{PLH}	CBA or CAB	A or B		24			24		ns
t_{PHL}				15			15		
t_{PLH}	A or B	B or A		24			24		ns
t_{PHL}				10			10		
t_{PLH}	SBA or SAB‡ (with A or B high)	A or B		26			26		ns
t_{PHL}				15			15		
t_{PLH}	SBA or SAB‡ (with A or B low)	A or B		26			26		ns
t_{PHL}				15			15		
t_{PLH}	$\overline{G}$	A or B		24			24		ns
t_{PHL}				17			17		
t_{PLH}	DIR	A or B		24			24		ns
t_{PHL}				17			17		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.
Additional information on these products can be obtained from the factory as it becomes available.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: Control inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54AS646, SN54AS648 . . . . . −55 °C to 125 °C
SN74AS646, SN74AS648 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54AS646 SN54AS648			SN74AS646 SN74AS648			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				48			64	mA
f_{clock}	Clock frequency		0		75	0		90	MHz
t_w	Pulse duration	Clock high	6			5			ns
		Clock low	7			6			
t_{su}	Setup time, A before CAB↑ or B before CBA↑		7			6			ns
t_h	Hold time, A after CAB↑ or B after CBA↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS646 SN54AS648			SN74AS646 SN74AS648			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.35	0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA					0.35	0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					50			50	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A or B ports‡					−0.5			−0.5	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS646	V_{CC} = 5.5 V	Outputs high		120	195		120	195	mA
			Outputs low		130	211		130	211	
			Outputs disabled		130	211		130	211	
	'AS648		Outputs high		110	185		110	185	
			Outputs low		120	195		120	195	
			Outputs disabled		120	195		120	195	

†All typical values are at V_{CC} = 5 V, T_A = 25 °C
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS646 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS646		SN74AS646		
			MIN	MAX	MIN	MAX	
f_{max}			75		90		MHz
t_{PLH}	CBA or CAB	A or B	2	9.5	2	8.5	ns
t_{PHL}			2	10	2	9	
t_{PLH}	A or B	B or A	2	11	2	9	ns
t_{PHL}			1	8	1	7	
t_{PLH}	SBA or SAB† (with A or B high)	A or B	2	12	2	11	ns
t_{PHL}			2	10	2	9	
t_{PZH}	$\overline{G}$	A or B	2	10	2	9	ns
t_{PZL}			3	15	3	14	
t_{PHZ}	$\overline{G}$	A or B	2	11	2	9	ns
t_{PLZ}			2	11	2	9	
t_{PZH}	DIR	A or B	3	19	3	16	ns
t_{PZL}			3	21	3	18	
t_{PHZ}	DIR	A or B	2	12	2	10	ns
t_{PLZ}			2	12	2	10	

'AS648 switching characteristics (see Note 1)

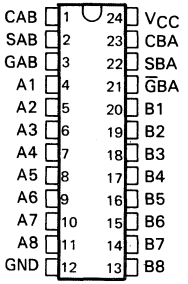
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS648		SN74AS648		
			MIN	MAX	MIN	MAX	
f_{max}			75		90		MHz
t_{PLH}	CBA or CAB	A or B	2	9.5	2	8.5	ns
t_{PHL}			2	10	2	9	
t_{PLH}	A or B	B or A	2	9	2	8	ns
t_{PHL}			1	8	1	7	
t_{PLH}	SBA or SAB† (with A or B high)	A or B	2	12	2	11	ns
t_{PHL}			2	10	2	9	
t_{PZH}	$\overline{G}$	A or B	2	10	2	9	ns
t_{PZL}			3	18	3	15	
t_{PHZ}	$\overline{G}$	A or B	2	11	2	9	ns
t_{PLZ}			2	11	2	9	
t_{PZH}	DIR	A or B	3	19	3	16	ns
t_{PZL}			3	21	3	18	
t_{PHZ}	DIR	A or B	2	12	2	10	ns
t_{PLZ}			2	12	2	10	

†These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

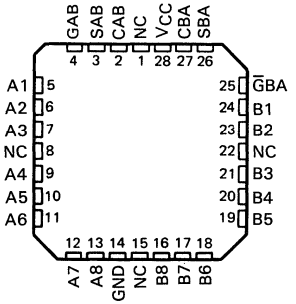
- **Bus Transceivers/Registers**
- **Independent Registers and Enables for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Choice of True and Inverting Data Paths**
- **Choice of 3-State or Open-Collector Outputs to A Bus**
- **Included Among the Package Options Are Compact 24-Pin 300-mil Wide DIPs and Small Outline (SO) and 28-Pin Plastic and Ceramic Chip Carriers**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	A OUTPUT	B OUTPUT	LOGIC
'ALS651, 'AS651	3-State	3-State	Inverting
'ALS652, 'AS652	3-State	3-State	True
'ALS653	Open-Collector	3-State	Inverting
'ALS654	Open-Collector	3-State	True

SN54ALS', SN54AS' . . . JT PACKAGE
SN74ALS', SN74AS' . . . NT PACKAGE
SN74ALS', SN74AS' . . . DW PACKAGE
(TOP VIEW)



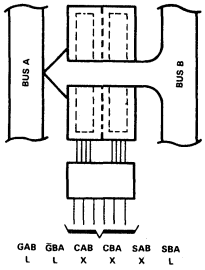
SN54ALS', SN54AS' . . . FH OR FK PACKAGE
SN74ALS', SN74AS' . . . FN PACKAGE
(TOP VIEW)



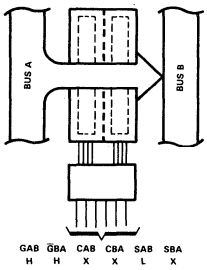
NC — No internal connection

description

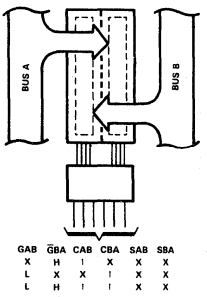
These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and GBA are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.



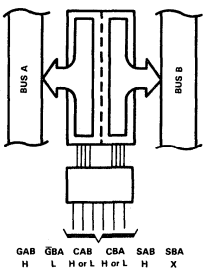
REAL-TIME TRANSFER BUS B TO BUS A



REAL-TIME TRANSFER BUS A TO BUS B



STORAGE FROM A AND/OR B



TRANSFER STORED DATA TO A AND/OR B

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{G}$BA. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The –1 versions of the SN74ALS651 through SN74ALS654 are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no –1 versions of the SN54ALS651 through SN54ALS654.

The SN54' family is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

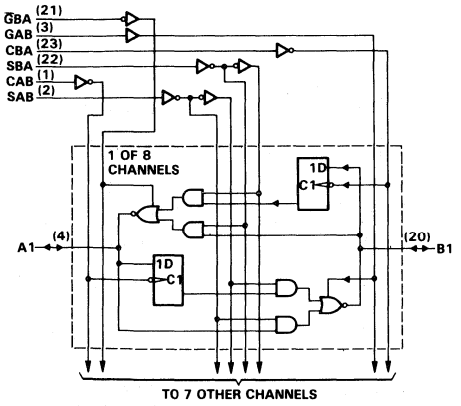
FUNCTION TABLE

INPUTS						DATA I/O*		OPERATION OR FUNCTION	
GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'ALS651, 'ALS653 'AS651	'ALS652, 'ALS654 'AS652
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X			Store A and B Data	Store A and B Data
X	H	↑	H or L	X	X	Input	Not specified	Store A, Hold B	Store A, Hold B
H	H	↑	↑	X	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Not specified	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	X	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored $\overline{A}$ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus and Stored $\overline{B}$ Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

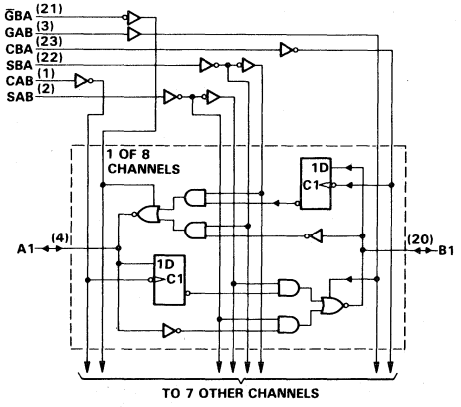
*The data output functions may be enabled or disabled by various signals at the GAB and $\overline{G}$BA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

logic diagrams (positive logic)

'ALS651, 'AS651, 'ALS653



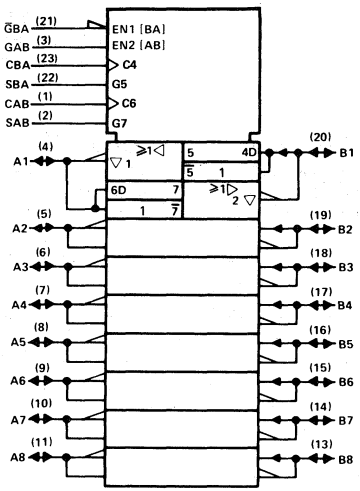
'ALS652, 'AS652, 'ALS654



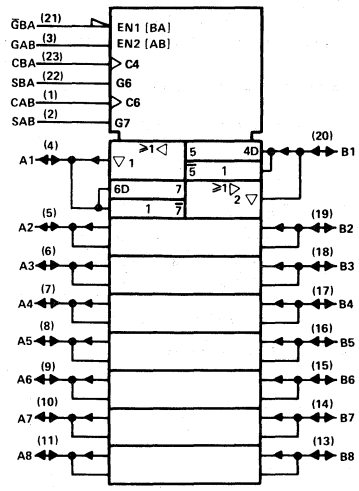
Pin numbers shown are for JT and NT packages.

logic symbols

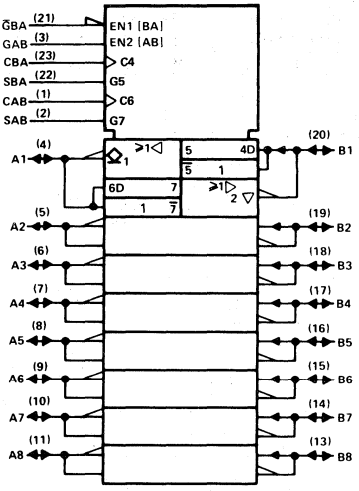
'ALS651, 'AS651



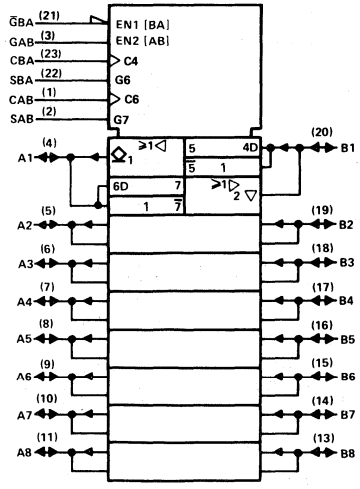
'ALS652, 'AS652



'ALS653



'ALS654



Pin numbers shown are for JT and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: Control inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS651, SN54ALS652 . . . . . −55 °C to 125 °C
SN74ALS651, SN74ALS652 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54ALS651 SN54ALS652			SN74ALS651 SN74ALS652			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				12			24	mA
								48†	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	CBA or CAB high							ns
		CBA or CAB low							
t_{su}	Setup time before CAB↑ or CBA↑	A or B							ns
t_h	Hold time after CAB↑ or CBA↑	A or B							ns
T_A	Operating free-air temperature		−55		125	0		70	°C

†The extended condition applies if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS651-1 and SN74ALS652-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS651 SN54ALS652			SN74ALS651 SN74ALS652			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports§					−0.2			−0.2	
I_O¶		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS651	V_{CC} = 5.5 V	Outputs high		52			52		mA
			Outputs low		57			57		
			Outputs disabled		58			58		
	'ALS652		Outputs high		60			60		
			Outputs low		68			68		
			Outputs disabled		68			68		

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS651 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS651			SN74ALS651			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}									MHz
t_{PLH}	CBA or CAB	A or B		11			11		ns
t_{PHL}				13			13		
t_{PLH}	A or B	B or A		10			10		ns
t_{PHL}				12			12		
t_{PLH}	SBA or SAB‡ (with A or B high)	A or B		16			16		ns
t_{PHL}				16			16		
t_{PLH}	SBA or SAB‡ (with A or B low)	A or B		15			15		ns
t_{PHL}				15			15		
t_{PZH}	$\overline{G}$BA	A		17			17		ns
t_{PZL}				20			20		
t_{PHZ}	$\overline{G}$BA	A		10			10		ns
t_{PLZ}				12			12		
t_{PZH}	GAB	B		19			19		ns
t_{PZL}				22			22		
t_{PHZ}	GAB	B		12			12		ns
t_{PLZ}				14			14		

'ALS652 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS652			SN74ALS652			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}									MHz
t_{PLH}	CBA or CAB	A or B		11			11		ns
t_{PHL}				13			13		
t_{PLH}	A or B	B or A		8			8		ns
t_{PHL}				8			8		
t_{PLH}	SBA or SAB‡ (with A or B high)	A or B		16			16		ns
t_{PHL}				16			16		
t_{PLH}	SBA or SAB‡ (with A or B low)	A or B		15			15		ns
t_{PHL}				12			12		
t_{PZH}	$\overline{G}$BA	A		17			17		ns
t_{PZL}				20			20		
t_{PHZ}	$\overline{G}$BA	A		10			10		ns
t_{PLZ}				12			12		
t_{PZH}	GAB	B		19			19		ns
t_{PZL}				22			22		
t_{PHZ}	GAB	B		12			12		ns
t_{PLZ}				14			14		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

PRODUCT PREVIEW

This page contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs and A I/O ports . . . . . 7 V
B I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS653, SN54ALS654 . . . . . −55°C to 125°C
SN74ALS653, SN74ALS654 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS653 SN54ALS654			SN74ALS653 SN74ALS654			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{OH}	High-level output voltage	A ports			5.5			5.5	V
I_{OH}	High-level output current	B ports			−12			−15	mA
I_{OL}	Low-level output current				12			24	mA
								48†	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	CBA or CAB high							ns
		CBA or CAB low							
t_{su}	Setup time before CAB↑ or CBA↑	A or B							ns
t_h	Hold time after CAB↑ or CBA↑	A or B							ns
T_A	Operating free-air temperature		−55		125	0		70	°C

†The extended condition applies if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS653-1 and SN74ALS654-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS653 SN54ALS654			SN74ALS653 SN74ALS654			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	B ports	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
I_{OH}	A ports	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.75 V, (I_{OL} = 48 mA for −1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports§					−0.2			−0.2	
I_O¶	B ports	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS653	V_{CC} = 5.5 V	Outputs high		52			52		mA
			Outputs low		57			57		
			Outputs disabled		58			58		
	'ALS654		Outputs high		60			60		
			Outputs low		68			68		
			Outputs disabled		68			68		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

PRODUCT PREVIEW

'ALS653 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, (A outputs) R1 = R2 = 500 Ω, (B outputs) T_A = MIN to MAX						UNIT
			SN54ALS653			SN74ALS653			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}									MHz
t_{PLH}	CBA	A		24			24		ns
t_{PHL}				15			15		
t_{PLH}	CAB	B		11			11		ns
t_{PHL}				13			13		
t_{PLH}	A	B		10			10		ns
t_{PHL}				12			12		
t_{PLH}	B	A		24			24		ns
t_{PHL}				10			10		
t_{PLH}	SBA‡ (with B high)	A		26			26		ns
t_{PHL}				15			15		
t_{PLH}	SBA‡ (with B low)	A		26			26		ns
t_{PHL}				15			15		
t_{PLH}	SAB‡ (with A high)	B		16			16		ns
t_{PHL}				16			16		
t_{PLH}	SAB‡ (with A low)	B		15			15		ns
t_{PHL}				15			15		
t_{PLH}	$\overline{G}$BA	A		24			24		ns
t_{PHL}				17			17		
t_{PZH}	GAB	B		19			19		ns
t_{PZL}				22			22		
t_{PHZ}	GAB	B		12			12		ns
t_{PLZ}				14			14		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.
Additional information on these products can be obtained from the factory as it becomes available.

'ALS654 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, (A outputs) R1 = R2 = 500 Ω, (B outputs) T_A = MIN to MAX						UNIT
			SN54ALS654			SN74ALS654			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}									MHz
t_{PLH}	CBA	A		24			24		ns
t_{PHL}				15			15		
t_{PLH}	CAB	B		11			11		ns
t_{PHL}				13			13		
t_{PLH}	A	B		8			8		ns
t_{PHL}				8			8		
t_{PLH}	B	A		24			24		ns
t_{PHL}				10			10		
t_{PLH}	SBA‡ (with B high)	A		26			26		ns
t_{PHL}				15			15		
t_{PLH}	SBA‡ (with B low)	A		26			26		ns
t_{PHL}				15			15		
t_{PLH}	SAB‡ (with A high)	B		16			16		ns
t_{PHL}				16			16		
t_{PLH}	SAB‡ (with A low)	B		15			15		ns
t_{PHL}				12			12		
t_{PLH}	$\overline{G}$BA	A		24			24		ns
t_{PHL}				17			17		
t_{PZH}	GAB	B		19			19		ns
t_{PZL}				22			22		
t_{PHZ}	GAB	B		12			12		ns
t_{PLZ}				14			14		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.
Additional information on these products can be obtained from the factory as it becomes available.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: Control inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54AS651, SN54AS652 . . . . . −55 °C to 125 °C
SN74AS651, SN74AS652 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54AS651 SN54AS652			SN74AS651 SN74AS652			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				48			64	mA
f_{clock}			0		75	0		90	MHz
t_w	Pulse duration	CBA or CAB high	6			5			ns
		CBA or CAB low	7			6			
t_{su}	Setup time before CAB↑ or CBA↑	A or B	7			6			ns
t_h	Hold time after CAB↑ or CBA↑	A or B	0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			SN54AS651 SN54AS652			SN74AS651 SN74AS652			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA		V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA		2.4						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA					2.4			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA			0.35	0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA						0.35	0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V				0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V				0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V				20			20	μA
	A or B ports‡						50			50	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V				−0.5			−0.5	mA
	A or B ports‡						−0.5			−0.5	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V		−30		−112	−30		−112	mA
I_{CC}	'AS651	V_{CC} = 5.5 V		Outputs high		110	185		110	185	mA
				Outputs low		120	195		120	195	
				Outputs disabled		130	195		130	195	
	'AS652			Outputs high		120	195		120	195	
				Outputs low		130	211		130	211	
				Outputs disabled		130	211		130	211	

†All typical values are at V_{CC} = 5 V, T_A = 25 °C
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS651 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS651		SN74AS651		
			MIN	MAX	MIN	MAX	
f_{max}			75		90		MHz
t_{PLH}	CBA or CAB	A or B	2	9.5	2	8.5	ns
t_{PHL}			2	10	2	9	
t_{PLH}	A or B	B or A	2	9	2	8	ns
t_{PHL}			1	8	1	7	
t_{PLH}	SBA or SAB†	A or B	2	12	2	11	ns
t_{PHL}			2	10	2	9	
t_{PZH}	$\overline{G}$BA	A	2	11	2	10	ns
t_{PZL}			3	18	3	16	
t_{PHZ}	$\overline{G}$BA	A	2	10	2	9	ns
t_{PLZ}			2	10	2	9	
t_{PZH}	GAB	B	3	12	3	11	ns
t_{PZL}			3	20	3	16	
t_{PHZ}	GAB	B	2	11	2	10	ns
t_{PLZ}			2	12	2	11	

'AS652 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS652		SN74AS652		
			MIN	MAX	MIN	MAX	
f_{max}			75		90		MHz
t_{PLH}	CBA or CAB	A or B	2	9.5	2	8.5	ns
t_{PHL}			2	10	2	9	
t_{PLH}	A or B	B or A	2	11	2	9	ns
t_{PHL}			1	8	1	7	
t_{PLH}	SBA or SAB†	A or B	2	12	2	11	ns
t_{PHL}			2	10	2	9	
t_{PZH}	$\overline{G}$BA	A	2	11	2	10	ns
t_{PZL}			3	18	3	16	
t_{PHZ}	$\overline{G}$BA	A	2	10	2	9	ns
t_{PHL}			2	10	2	9	
t_{PZH}	GAB	B	3	12	3	11	ns
t_{PZL}			3	20	3	16	
t_{PHZ}	GAB	B	2	11	2	10	ns
t_{PLZ}			2	12	2	11	

†These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D2661, JUNE 1982—REVISED MARCH 1984

- **'ALS677 is a 16-bit Address Comparator with Enable**
- **'ALS678 is a 16-bit Address Comparator with Latch**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

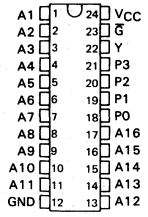
description

The 'ALS677 and 'ALS678 address comparators simplify addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input information applied to the 16 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A1 through A7 must be low and that inputs A8 through A16 must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

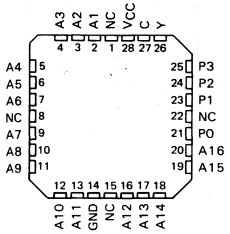
The 'ALS677 features an enable input (G). When G is low, the device is enabled. When G is high, the device is disabled and the output is high regardless of the A and P inputs. The 'ALS678 features a transparent latch and a latch enable input (C). When C is high, the device is in the transparent mode. When C is low, the previous logic state of Y is latched.

The SN54ALS677 and SN54ALS678 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN54ALS677 and SN74ALS678 are characterized for operation from 0°C to 70°C.

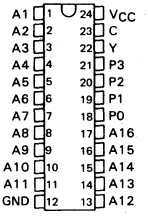
SN54ALS677 . . . JT PACKAGE
SN74ALS677 . . . NT PACKAGE
SN74ALS677 . . . DW PACKAGE
(TOP VIEW)



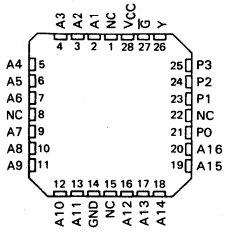
SN54ALS677 . . . FH OR FK PACKAGE
SN74ALS677 . . . FN PACKAGE
(TOP VIEW)



SN54ALS678 . . . JT PACKAGE
SN74ALS678 . . . NT PACKAGE
SN74ALS678 . . . DW PACKAGE
(TOP VIEW)



SN54ALS678 . . . FH OR FK PACKAGE
SN74ALS678 . . . FN PACKAGE
(TOP VIEW)

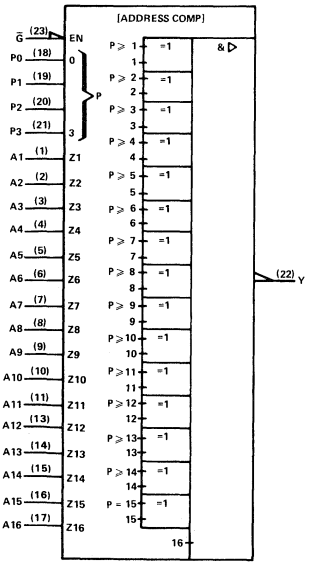


FUNCTION TABLE

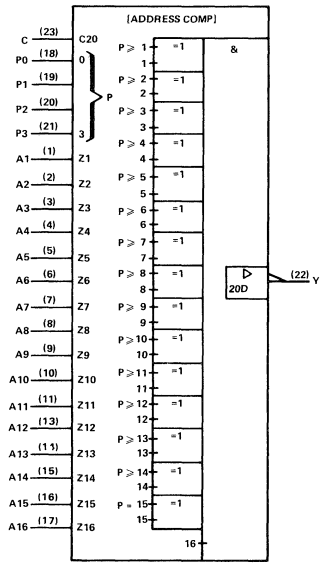
'ALS677	'ALS678	INPUTS COMMON TO 'ALS677 AND 'ALS678																				OUTPUT
$\overline{G}$	C	P3	P2	P1	P0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	Y
L	H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	L	H	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	L
L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L
L	H	H	L	L	H	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	L
L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	L
L	H	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	L
L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L
L	H	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	L
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	L
L	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	All other combinations																				H
H		'ALS677: Any combination																				H
	L	'ALS678: Any combination																				Latched

logic symbols

'ALS677



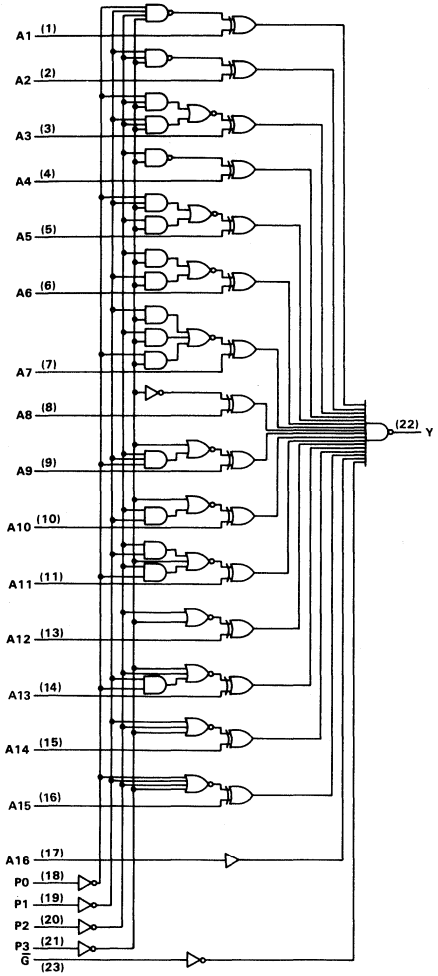
'ALS678



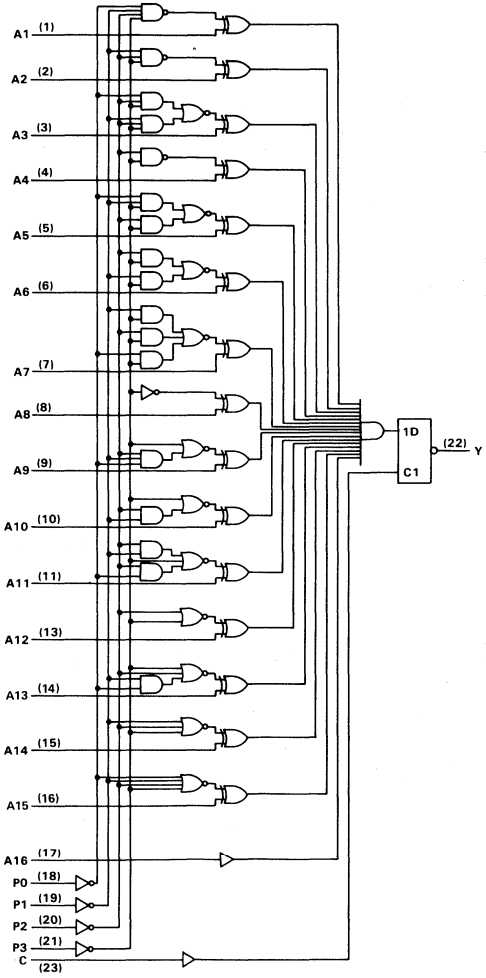
Pin numbers shown are for JT and NT packages.

logic diagrams (positive logic)

'ALS677



'ALS678



Pin numbers shown are for JT and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS677, SN54ALS678 . . . . . −55°C to 125°C
SN74ALS677, SN74ALS678 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS677 SN54ALS678			SN74ALS677 SN74ALS678			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS677 SN54ALS678			SN74ALS677 SN74ALS678			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS677	V_{CC} = 5.5 V			21	33		21	33	mA
	'ALS678				21	35		21	35	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS677 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS677		SN74ALS677		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any P	Y	4	28	4	25	ns
t_{PHL}			8	40	8	35	
t_{PLH}	Any A	Y	5	26	5	22	ns
t_{PHL}			5	40	5	35	
t_{PLH}	$\overline{G}$	Y	3	15	3	13	ns
t_{PHL}			5	30	5	25	

'ALS678 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS678		SN74ALS678		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any P	Y	6	27	6	22	ns
t_{PHL}			10	52	10	43	
t_{PLH}	Any A	Y	5	25	5	21	ns
t_{PHL}			5	40	5	35	
t_{PLH}	C	Y	3	25	3	20	ns
t_{PHL}			15	54	15	48	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

TYPICAL APPLICATION INFORMATION

The 'ALS677 and 'ALS678 can be wired to recognize any one of $2^{16} - 1$ addresses. The number of "lows" in the address determines the input pattern for the P inputs. Then those system address lines that are low in the address to be recognized are connected to the lowest numbered A inputs of the address comparator and the system address lines that are high are connected to the highest numbered A inputs.

For example, assume the comparator is to enable a device when the 16-bit system address is:

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
H	H	L	L	H	H	L	L	H	H	L	L	H	H	H	H

Since the address contains 6 lows and 10 highs, the following connections are made:

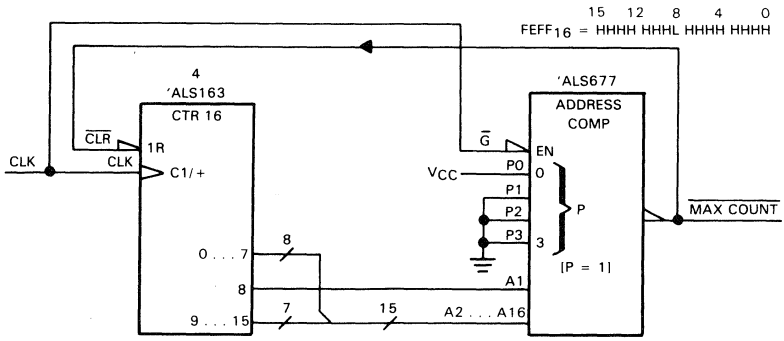
P3 to 0 V, P2 to V_{CC}, P1 to V_{CC}, and P0 to 0 V.

System address lines A13, A12, A9, A8, A5, and A4 to comparator inputs A1 through A6 in any convenient order.

The remaining ten system address lines to comparator inputs A7 through A16 in any convenient order.

The output provides an active-low enabling signal.

The following circuit is a modulo-N synchronous counter. The 'ALS163 is connected to provide a low-level clear signal when $N = FEFF_{16}$.



MODULO-N SYNCHRONOUS COUNTER

D2661, JUNE 1982—REVISED MARCH 1984

- **'ALS679 is a 12-Bit Address Comparator With Enable**
- **'ALS680 is a 12-Bit Address Comparator With Latch**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

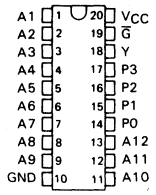
description

The 'ALS679 and 'ALS680 address comparators simplify addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input information applied to the 12 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A1 through A7 must be low and that inputs A8 through A12 must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

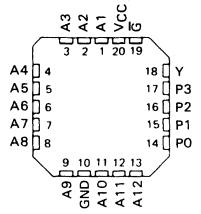
The 'ALS679 features an enable input ($\overline{G}$). When $\overline{G}$ is low, the device is enabled. When $\overline{G}$ is high, the device is disabled and the output is high regardless of the A and P inputs. The 'ALS680 features a transparent latch and a latch enable input (C). When C is high, the device is in the transparent mode. When C is low, the previous logical state of Y is latched.

The SN54ALS679 and SN54ALS680 are characterized for operation over the full military temperature of −55°C to 125°C. The SN74ALS679 and SN74ALS680 are characterized for operation from 0°C to 70°C.

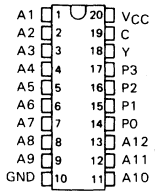
SN54ALS679 . . . J PACKAGE
SN74ALS679 . . . N PACKAGE
SN74ALS679 . . . DW PACKAGE
(TOP VIEW)



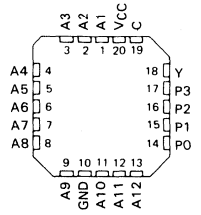
SN54ALS679 . . . FH OR FK PACKAGE
SN74ALS679 . . . FN PACKAGE
(TOP VIEW)



SN54ALS680 . . . J PACKAGE
SN74ALS680 . . . N PACKAGE
SN74ALS680 . . . DW PACKAGE
(TOP VIEW)



SN54ALS680 . . . FH OR FK PACKAGE
SN74ALS680 . . . FN PACKAGE
(TOP VIEW)

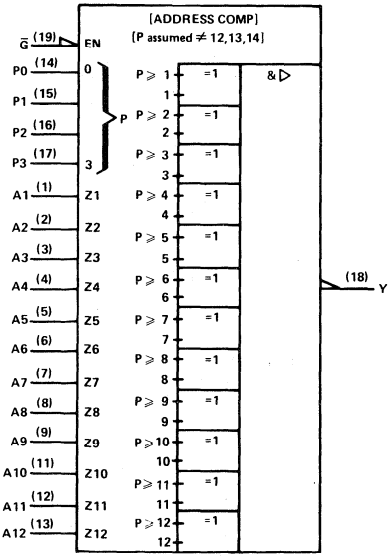


FUNCTION TABLE

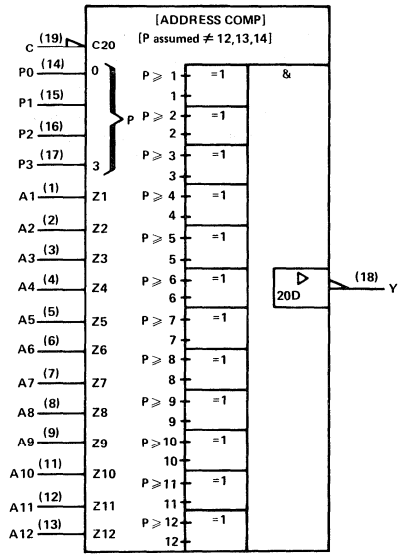
'ALS679	'ALS680	INPUTS COMMON TO 'ALS679 AND 'ALS680																OUTPUT
$\overline{G}$	C	P3	P2	P1	P0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	Y
L	H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	L
L	H	L	H	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L
L	H	L	H	L	H	L	L	L	L	L	H	H	H	H	H	H	H	L
L	H	L	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	L
L	H	H	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	L
L	H	H	L	L	H	L	L	L	L	L	L	L	L	H	H	H	H	L
L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	H	H	H	L
L	H	H	L	H	H	L	L	L	L	L	L	L	L	L	L	H	H	L
L	H	H	H	L	L	L	L	L	L	L	L	L	H	H	H	H	L	L*
L	H	H	H	L	H	L	L	L	L	L	L	L	L	H	H	H	L	L*
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	H	H	L	L*
L	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	All other combinations																H
H		'ALS679: Any combination																H
	L	'ALS680: Any combination																Latched

logic symbols

'ALS679



'ALS680

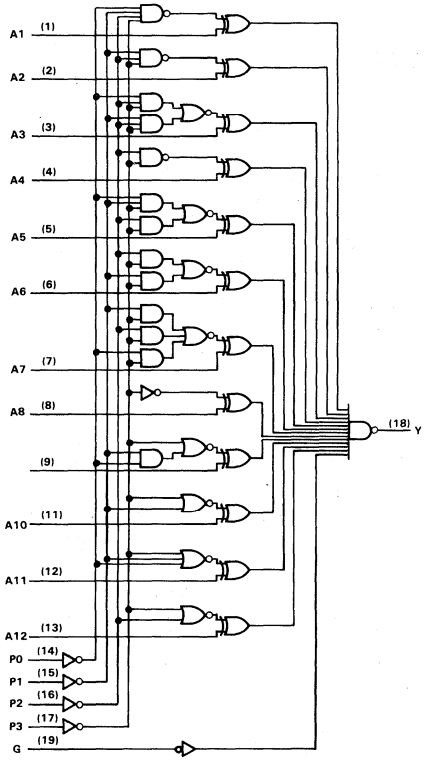


*The three shaded rows of the function table show combinations that would normally not be used in address comparator applications. The logic symbols above are not valid for these combinations in which P = 12, 13, and 14. If symbols valid for all combinations are required, starting with the fourth Exclusive-OR from the bottom, change P ≥ 9 to P = 9...11/13...15, P ≥ 10 to P = 10/11/14/15, and P ≥ 11 to P = 11/15.

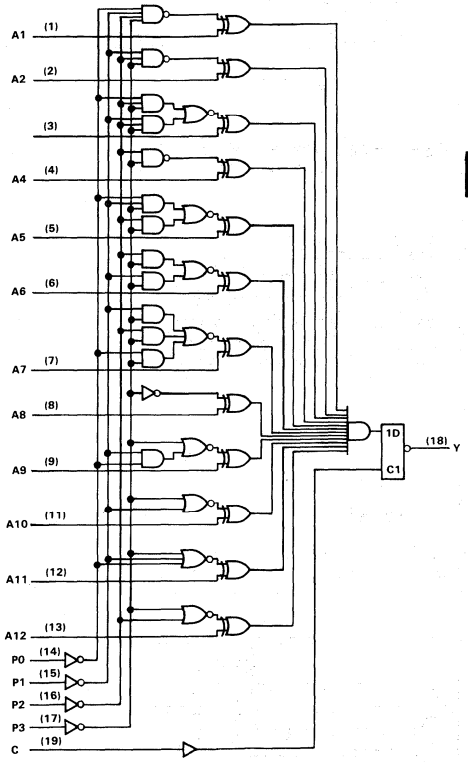
Pin numbers shown are for J and N packages.

logic diagrams (positive logic)

'ALS680



'ALS679



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS679, SN54ALS680 . . . . . −55 °C to 125 °C
SN74ALS679, SN74ALS680 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS679 SN54ALS680			SN74ALS679 SN74ALS680			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS679 SN54ALS680			SN74ALS679 SN74ALS680			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS679	V_{CC} = 5.5 V			17	28		17	28	mA
	'ALS680				18	27		18	27	

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS679 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS679		SN74ALS679		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any P	Y	4	28	4	25	ns
t_{PHL}			8	40	8	35	
t_{PLH}	Any A	Y	5	26	5	22	ns
t_{PHL}			5	35	5	30	
t_{PLH}	$\overline{G}$	Y	3	15	3	13	ns
t_{PHL}			5	30	5	25	

'ALS680 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V C_L = 50 pF R_L = 500 Ω T_A = MIN to MAX				UNIT
			SN54ALS680		SN74ALS680		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any P	Y	6	27	6	22	ns
t_{PHL}			10	43	10	38	ns
t_{PLH}	Any A	Y	5	25	5	21	ns
t_{PHL}			5	28	5	25	
t_{PLH}	C	Y	3	25	3	20	ns
t_{PHL}			15	48	15	42	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

TYPICAL APPLICATION INFORMATION

The 'ALS679 and 'ALS680 can be wired to recognize any one of 2^{12} addresses. The number of "lows" in the address determines the input pattern for the P inputs. Then those system address lines that are low in the address to be recognized are connected to the lowest numbered A inputs of the address comparator and the system address lines that are high are connected to the highest numbered A inputs.

For example, assume the comparator is to enable a device when the 12-bit system address is:

A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
H	H	L	L	H	H	L	L	H	H	H	H

Since the address contains 4 lows and 8 highs, the following connections are made:

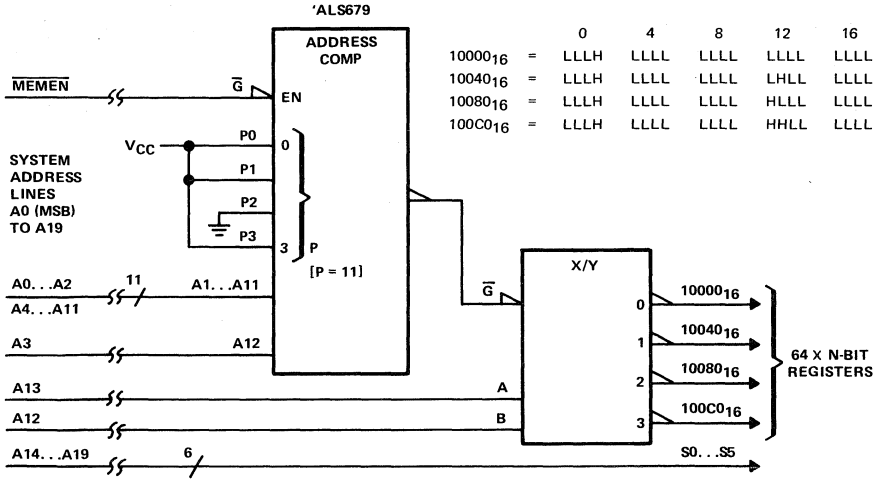
P3 to 0 V, P2 to V_{CC}, P1 to 0 V, and P0 to 0 V.

System address lines A9, A8, A5, and A4 to comparator inputs A1 through A4 in any convenient order.

The remaining eight system address lines to comparator inputs A5 through A12 in any convenient order.

The output provides an active-low enabling signal.

The following circuit is a register bank decoder that examines the 14 most significant bits (A0 through A13) of a 20-bit address to select banks corresponding to the hex addresses 10000, 10040, 10080, and 100C0.



REGISTER BANK DECODER

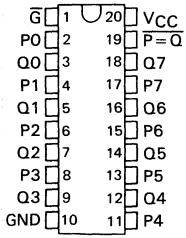
D2661, JUNE 1982-REVISED DECEMBER 1983

- **Compares Two Eight-Bit Words**
- **Choice of Totem-Pole or Open-Collector Outputs**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliablility**

TYPE	OUTPUT FUNCTION AND CONFIGURATION
'ALS688†	$\overline{P=Q}$ totem-pole
'ALS689	$\overline{P=Q}$ open-collector

†'ALS688 is identical to 'ALS521

SN54ALS688, SN54ALS689 . . . J PACKAGE
SN74ALS688, SN74ALS689 . . . N PACKAGE
SN74ALS688, SN74ALS689 . . . DW PACKAGE
(TOP VIEW)



2

description

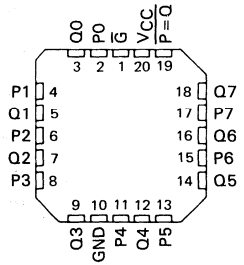
These identity comparators perform comparisons of two eight-bit binary or BCD words. The 'ALS688 and 'ALS689 provide $\overline{P=Q}$ outputs. The 'ALS688 has totem-pole outputs, while 'ALS689 has open-collector outputs.

The SN54ALS688 and SN54ALS689 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS688 and SN74ALS689 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

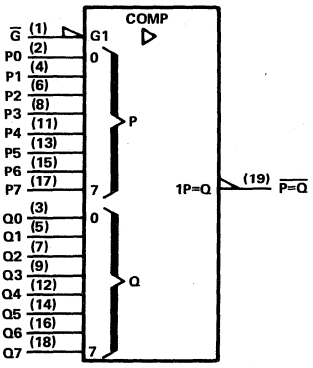
INPUTS		OUTPUT
DATA P,Q	ENABLE $\overline{G}$	$\overline{P=Q}$
P=Q	L	L
P>Q	L	H
P<Q	L	H
X	H	H

SN54ALS688, SN54ALS689 . . . FH OR FK PACKAGE
SN74ALS688, SN74ALS689 . . . FN PACKAGE
(TOP VIEW)

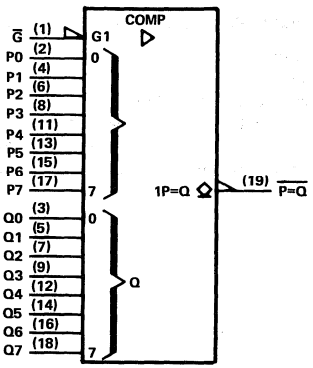


logic symbols

'ALS688

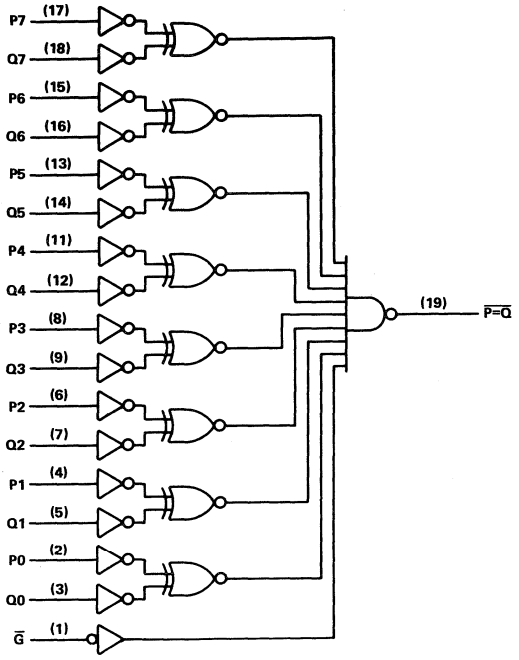


'ALS689



Pin numbers shown are for J and N packages.

logic diagram (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: . . . . . 7 V
Off-state output voltage: 'ALS689 . . . . . 7 V
Operating free-air temperature range: SN54ALS688, SN54AS689 . . . . . −55 °C to 125 °C
SN74ALS688, SN74AS689 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS688			SN74ALS688			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS688			SN74ALS688			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	See Note 1		12	19		12	19	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with G grounded, P and Q at 4.5 V.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS688		SN74ALS688		
			MIN	MAX	MIN	MAX	
t_{PLH}	P	$\overline{P=Q}$	3	16	3	12	ns
t_{PHL}			5	25	5	20	
t_{PLH}	Q	$\overline{P=Q}$	3	16	3	12	ns
t_{PHL}			5	25	5	20	
t_{PLH}	$\overline{G}$	$\overline{P=Q}$	3	15	3	12	ns
t_{PHL}			5	25	5	22	

NOTE 2: For load circuit and voltage waveforms, see page 1-12.

recommended operating conditions

		SN54ALS689			SN74ALS689			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS689			SN74ALS689			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CC}	V_{CC} = 5.5 V,	See Note 1		12	19		12	19	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: I_{CC} is measured with G grounded, P and Q at 4.5 V.

switching characteristics (see Note 2)

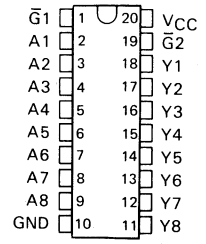
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS689		SN74ALS689		
			MIN	MAX	MIN	MAX	
t_{PLH}	P	$\overline{P=Q}$	10	30	10	25	ns
t_{PHL}			5	25	5	23	
t_{PLH}	Q	$\overline{P=Q}$	10	30	10	25	ns
t_{PHL}			5	25	5	23	
t_{PLH}	$\overline{G}$	$\overline{P=Q}$	8	30	8	25	ns
t_{PHL}			8	30	8	25	

NOTE 2: For load circuit and voltage waveforms, see page 1-12.

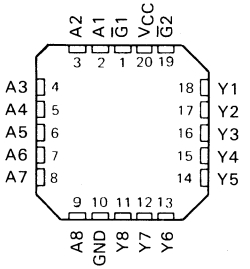
AUGUST 1984—REVISED DECEMBER 1984

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Input Pull-Up resistors Added for Data Bus Termination**
- **Data Flow-Thru Pinout (All Inputs on Opposite Side from Outputs)**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS746, SN54ALS747 . . . J PACKAGE
SN74ALS746, SN74ALS747 . . . N PACKAGE
SN74ALS746, SN74ALS747 . . . DW PACKAGE
(TOP VIEW)



SN54ALS746, SN54ALS747 . . . FH OR FK PACKAGE
SN74ALS746, SN74ALS747 . . . FN PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed to have the performance of the popular SN54ALS240A/SN74ALS240A series and, at the same time, offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout. In addition, 20 kilohm resistors have been added between all inputs and V_{CC}. This eliminates adding external resistors in applications where the data bus must be at a high level whenever all other connecting devices are at a high impedance state.

The three-state control gate is a 2-input NOR such that if either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high-impedance state.

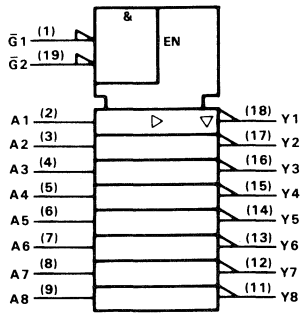
The 'ALS746 provides inverted data and the 'ALS747 provides true data at the outputs.

The -1 versions of the SN74ALS746 and SN74ALS747 parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliampers. There are no -1 versions of the SN54ALS746 and SN54ALS747.

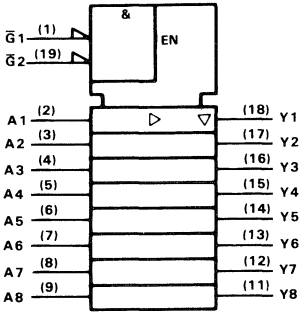
The SN54ALS746 and SN54ALS747 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN54ALS746 and SN74ALS747 are characterized for operation from 0°C to 70°C.

logic symbols†

'ALS746



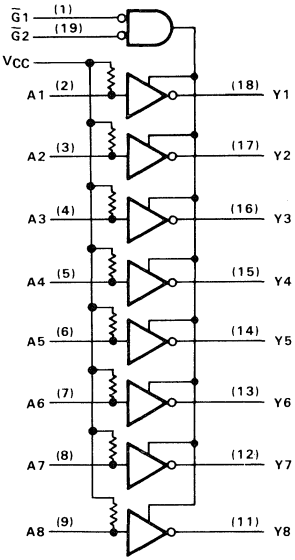
'ALS747



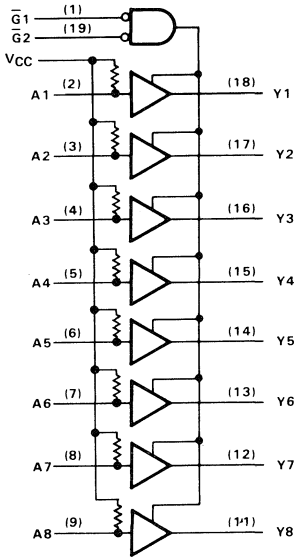
Pin numbers shown are for J and N packages
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

'ALS746



'ALS747



All input pull-up resistors are 20 kΩ

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS746, SN54ALS747 . . . . . −55°C to 125°C
SN74ALS746, SN74ALS747 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS746 SN54ALS747			SN74ALS746 SN74ALS747			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limit applies only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48 mA limit applies for the SN74ALS746-1 and SN74ALS747-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS746 SN54ALS747			SN74ALS746 SN74ALS747			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA¶					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	A	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
	$\overline{G}1$, $\overline{G}2$	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	
I_{IH}	A	V_{CC} = 5.5 V,	V_I = 2.7 V			−0.2			−0.2	mA
	$\overline{G}1$, $\overline{G}2$					20			20	μA
I_{IL}	A	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.6			−0.6	mA
	$\overline{G}1$, $\overline{G}2$					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS746	V_{CC} = 5.5 V,	Outputs high		7	12		7	12	mA
			Outputs low		13	22		13	22	
			Outputs disabled		11	19		11	19	
	'ALS747	V_{CC} = 5.5 V,	Outputs high		6	14		6	14	mA
			Outputs low		18	30		18	30	
			Outputs disabled		12.5	22		12.5	22	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely aproximates one half of the true short-circuit output current, I_{OS}.
¶I_{OL} = 48 mA for -1 versions.

'ALS746 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54/74ALS746			SN54ALS746		SN74ALS746		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y		7.5	10	3	14	3	12	ns
t_{PHL}				5.6	8	2	11	2	9	
t_{PZH}	$\overline{G}$	Y		9	12	5	18	5	15	ns
t_{PZL}				12.5	16	8	24	8	20	
t_{PHZ}	$\overline{G}$	Y		4	6	1	12	1	10	ns
t_{PLZ}				7	9	2	14	2	12	

'ALS747 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54/74ALS747			SN54ALS747		SN74ALS747		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y		8.7	11	4	17	4	14	ns
t_{PHL}				7.4	10	2	12	2	10	
t_{PZH}	$\overline{G}$	Y		9	12	5	18	5	15	ns
t_{PZL}				12.5	16	8	24	8	20	
t_{PHZ}	$\overline{G}$	Y		4	6	1	12	1	10	ns
t_{PLZ}				7	9	2	14	2	12	

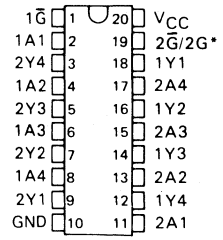
NOTE 1. For load circuit and voltage waveforms, see page 1-12

OCTAL BUFFERS AND LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS

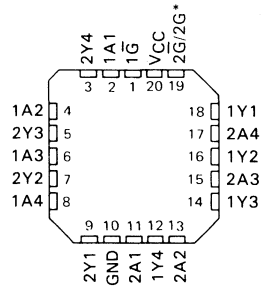
D2261, DECEMBER 1983—REVISED NOVEMBER 1984

- **Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Eliminates the Need for 3-State Overlap Protection**
- **P-N-P Inputs Reduce DC Loading**
- **Dependable Texas Instruments Quality and Reliability**
- **Open-Collector Versions of 'ALS240A, 'ALS241A, and 'AS240, 'AS241**

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . N PACKAGE
SN74ALS', SN74AS' . . . DW PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FH OR FK PACKAGE
SN74ALS', SN74AS' . . . FN PACKAGE
(TOP VIEW)



*2$\overline{G}$ for 'ALS756, 'AS756 or 2G for 'ALS757, 'AS757.

description

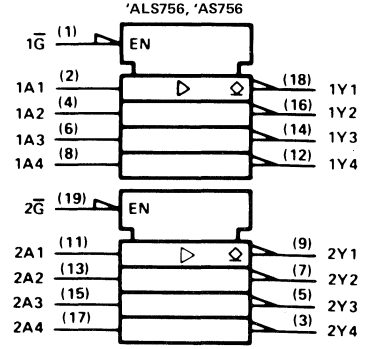
These octal bus transceivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters by eliminating the need for three-state overlap protection. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out and improved fan-in.

The -1 versions of the SN74ALS756 and SN74ALS757 parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS756 and SN54ALS757.

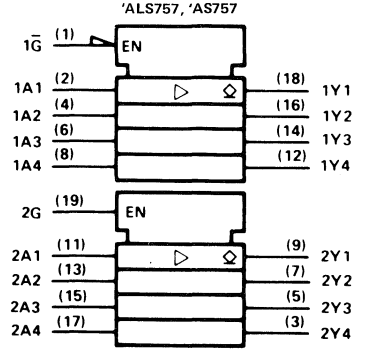
The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

logic symbols

'ALS756, 'AS756



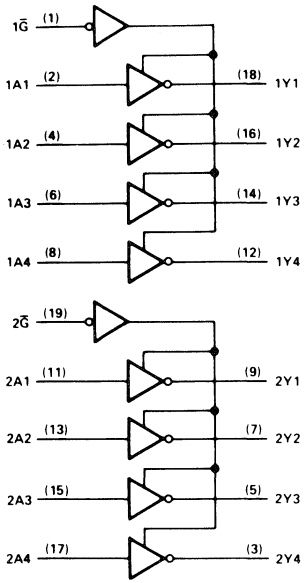
'ALS757, 'AS757



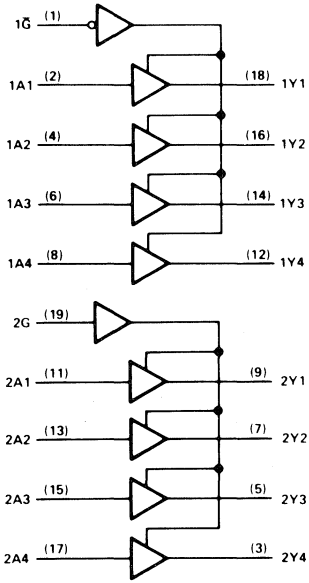
Pin numbers shown are for J and N packages.

logic diagrams (positive logic)

'ALS756, 'AS756



'ALS757, 'AS757



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS756, SN54ALS757 . . . . . −55°C to 125°C
SN74ALS756, SN74ALS757 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS756 SN54ALS757			SN74ALS756 SN74ALS757			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limit applies only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48 mA limit applies for the SN74ALS756-1 and SN74ALS757-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS756 SN54ALS757			SN74ALS756 SN74ALS757			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA§					0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CC}	'ALS756	V_{CC} = 5.5 V,	Output high		7	11		7	11	mA
			Output low		13	22		13	22	
	'ALS757	V_{CC} = 5.5 V,	Output high		7			7		
			Output low		11			11		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§I_{OL} = 48 mA for -1 versions.

'ALS756 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C, SN54/74ALS756			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX, SN54ALS756		SN74ALS756		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y		14	20	8	29	8	24	ns
t_{PHL}				5	12	2	12	2	10	
t_{PLH}	$\overline{G}$	Y		16	21	8	29	8	24	ns
t_{PHL}				12	16	6	23	6	20	

'ALS757 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C, SN54/74ALS757			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX, SN54ALS757		SN74ALS757		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y		7						ns
t_{PHL}				6						
t_{PLH}	$\overline{G}$ or G	Y		18						ns
t_{PHL}				11						

NOTE 1: For load circuit and voltage waveforms, see page 1-12

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54AS756, SN54AS757 . . . . . −55°C to 125°C
SN74AS756, SN74AS757 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS756 SN54AS757			SN74AS756 SN74AS757			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS756 SN54AS757			SN74AS756 SN74AS757			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA				−1.2			−1.2	V
I_{OH}		V_{CC} = 4.5 V, V_{OH} = 5.5 V				0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V, I_{OL} = 48 mA			0.55					V
		V_{CC} = 4.5 V, I_{OL} = 64 mA							0.55	
I_I		V_{CC} = 5.5 V, V_I = 7 V				0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V, V_I = 2.7 V				20			20	μA
I_{IL}	'AS757 A inputs only	V_{CC} = 5.5 V, V_I = 0.4 V				−1			−1	mA
	All other				−0.5			−0.5		
I_{CC}	'AS756	V_{CC} = 5.5 V,	Output high		9	15		9	15	mA
			Output low		51	80		51	80	
	'AS757		Output high		21	33		21	33	
			Output low		61	95		61	95	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

'AS756 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS756		SN74AS756		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	20	3	19	ns
t_{PHL}			1	7	1	6	
t_{PLH}	$\overline{G}$	Y	3	22	3	19.5	ns
t_{PHL}			1	8.5	1	7.5	

'AS757 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS757		SN74AS757		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	19.5	3	18.5	ns
t_{PHL}			1	7	1	6	
t_{PLH}	$1\overline{G}$	Y	3	21	3	20	ns
t_{PHL}			1	8	1	7	
t_{PLH}	2G	Y	3	22.5	3	21	ns
t_{PHL}			1	8.5	1	7.5	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

TYPES SN54AS758, SN54AS759, SN74AS758, SN74AS759
QUADRUPLE BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

DECEMBER 1983 – REVISED FEBRUARY 1984

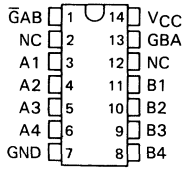
- **2-Way Asynchronous Communication Between Data Buses**
- **P-N-P Inputs Reduce Loading**
- **Dependable Texas Instruments Quality and Reliability**
- **Open-Collector Versions of 'AS242, 'AS243**

description

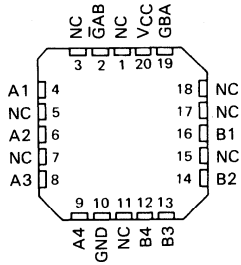
These four-data-line transceivers are designed for asynchronous two-way communications between data buses.

The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

SN54' . . . J PACKAGE
SN74' . . . N PACKAGE
SN74' . . . D PACKAGE
(TOP VIEW)

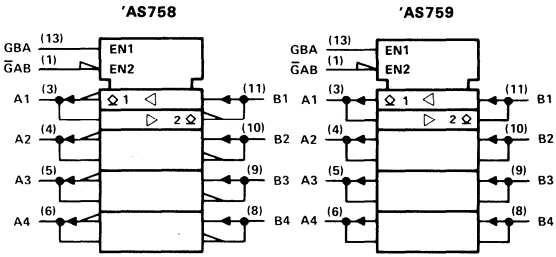


SN54' . . . FH OR FK PACKAGE
SN74' . . . FN PACKAGE
(TOP VIEW)

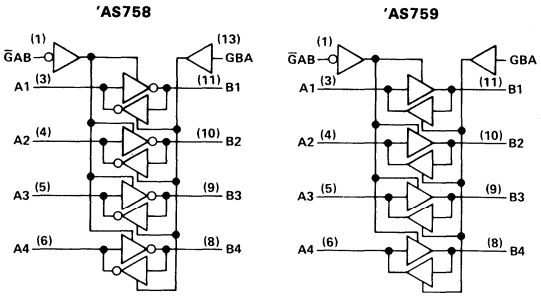


NC—No Internal connection

logic symbol



logic diagrams (positive logic)



Pin numbers shown are for J and N packages.

FUNCTION TABLE

INPUTS		'AS758	'AS759
GAB	GBA		
L	L	A to B	A to B
H	H	B to A	B to A
H	L	Isolation	Isolation
L	H	Latch A and B (A = B)	Latch A and B (A = B)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs and I/O ports . . . . . 7 V
Operating free-air temperature range: SN54AS758, SN54AS759 . . . . . −55 °C to 125 °C
SN74AS758, SN74AS759 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS758 SN54AS759			SN74AS758 SN74AS759			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS758 SN54AS759			SN74AS758 SN74AS759			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA			0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA						0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports					50			50	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	'AS758 A or B ports‡					−0.5			−0.5	
	'AS759 A or B ports‡					−1			−1	
I_{CC}	'AS758	V_{CC} = 5.5 V	Outputs high		17	27		17	27	mA
			Outputs low		38	60		38	60	
	'AS759		Outputs high		27	43		27	43	
			Outputs low		47	74		47	74	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

'AS758 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS758		SN74AS758		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	3	20.5	3	19.5	ns
t_{PHL}			1	7	1	6	
t_{PLH}	GBA	A	3	22	3	19.5	ns
t_{PHL}			1	8.5	1	7.5	
t_{PLH}	$\overline{G}AB$	B	3	22	3	21	ns
t_{PHL}			1	8.5	1	8	

'AS759 switching characteristics (see Note 1)

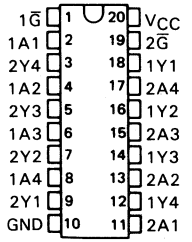
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS759		SN74AS759		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	3	21	3	20	ns
t_{PHL}			1	7	1	6	
t_{PLH}	GBA	A	3	21	3	20	ns
t_{PHL}			1	8	1	7	
t_{PLH}	$\overline{G}AB$	B	3	22.5	3	21	ns
t_{PHL}			1	8.5	1	7.5	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

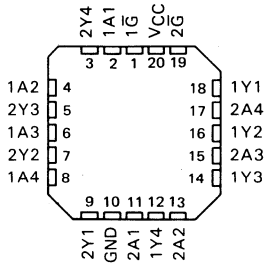
DECEMBER 1983 – REVISED FEBRUARY 1984

- **Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Eliminates the Need For 3-State Overlap Protection**
- **P-N-P Inputs Reduce DC Loading**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**
- **Open-Collector Version of 'AS244**

SN54AS760 . . . J PACKAGE
SN74AS760 . . . N PACKAGE
SN74AS760 . . . DW PACKAGE
(TOP VIEW)



SN54AS760 . . . FH OR FK PACKAGE
SN74AS760 . . . FN PACKAGE
(TOP VIEW)

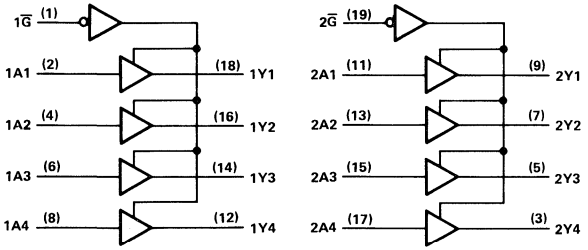


description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters by eliminating the need for 3-state overlap protection. Taken together with the 'AS756 and 'AS757, these devices provide the choice of selected combinations of inverting outputs, symmetrical $\overline{G}$ (active-low input control) inputs, and complementary G and $\overline{G}$ inputs.

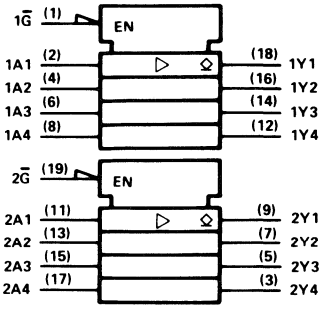
The SN54AS760 is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74AS760 is characterized for operation from 0 °C to 70 °C.

functional block diagram (positive logic)



Pin numbers shown are for J and N packages

logic symbol



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54AS760 . . . . . −55 °C to 125 °C
SN74AS760 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS760			SN74AS760			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS760			SN74AS760			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA			0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA						0.55	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	$\overline{G}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A					−1			−1	
I_{CC}		V_{CC} = 5.5 V	Outputs high		20	32		20	32	mA
			Outputs low		60	94		60	94	

'AS760 switching characteristics (see Note 1)

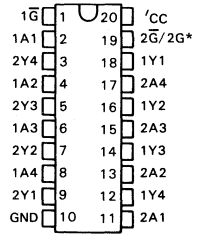
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS760		SN74AS760		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	19.5	3	18.5	ns
t_{PHL}			1	7	1	6	
t_{PLH}	$\overline{G}$	Y	3	19.5	3	18.5	ns
t_{PHL}			1	8	1	7	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

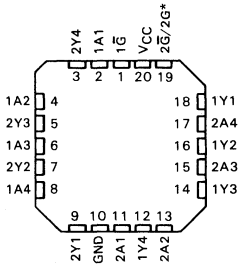
DECEMBER 1983—REVISED FEBRUARY 1984

- **Included Among the Package Options Are Small 20-Pin DIPs and Small Outline (SO) and Plastic and Ceramic Chip Carriers**
- **'AS762 Has True and Complementary Outputs**
- **'AS763 Has Complementary G and $\overline{G}$ Inputs**
- **Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Eliminates the Need for 3-State Overlap Protection**
- **Current Sinking Capability Up to 64 mA**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS'... J PACKAGE
SN74AS'... N PACKAGE
SN74AS'... DW PACKAGE
(TOP VIEW)



SN54AS'... FH OR FK PACKAGE
SN74AS'... FN PACKAGE
(TOP VIEW)



*$2\overline{G}$ for 'AS762 or 2G for 'AS763

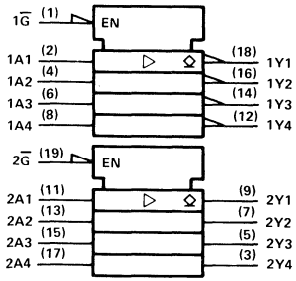
description

These octal buffers and line drivers are designed specifically to improve the performance of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters by eliminating the need for 3-state overlap protection. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs.

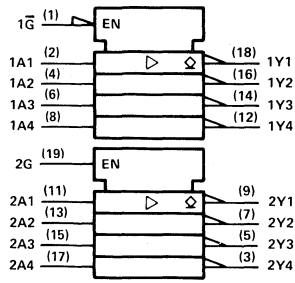
The SN54AS762 and SN54AS763 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS762 and SN74AS763 are characterized for operation from 0°C to 70°C.

logic symbols

'AS762



'AS763



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54AS762, SN54AS763 . . . . . −55°C to 125°C
SN74AS762, SN74AS763 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS762 SN54AS763			SN74AS762 SN74AS763			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS762 SN54AS763			SN74AS762 SN74AS763			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA			0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA						0.55	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	'AS762 2A inputs only	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	All other					−0.5			−0.5	
I_{CC}	'AS762	V_{CC} = 5.5 V	Output high		15	23		15	23	mA
			Output low		55	87		55	87	
	'AS763	V_{CC} = 5.5 V	Output high		10	16		10	16	
			Output low		52	82		52	82	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

'AS762 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS762		SN74AS762		
			MIN	MAX	MIN	MAX	
t_{PLH}	1A	1Y	3	20	3	19	ns
t_{PHL}			1	7	1	6	
t_{PLH}	2A	2Y	3	19.5	3	18.5	ns
t_{PHL}			1	7	1	6	
t_{PLH}	$\overline{G}$	1Y	3	22	3	19.5	ns
t_{PHL}			1	8	1	7.5	
t_{PLH}	$\overline{G}$	2Y	3	20	3	19	ns
t_{PHL}			1	8	1	7	

'AS763 switching characteristics (see Note 1)

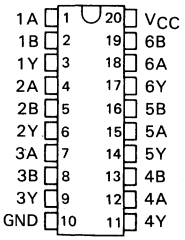
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS763		SN74AS763		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	20	3	19	ns
t_{PHL}			1	7	1	6	
t_{PLH}	$\overline{G}$	Y	3	22	3	19.5	ns
t_{PHL}			1	8.5	1	7.5	
t_{PLH}	G	Y	3	22	3	20	ns
t_{PHL}			1	8.5	1	8	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

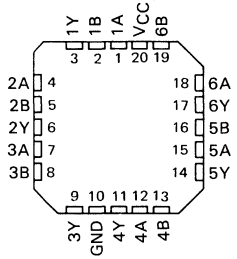
D2661, DECEMBER 1982—REVISED JUNE 1984

- **High Capacitive Drive Capability**
- **'ALS804 Has Typical Delay Time of 4 ns (C_L = 50 pF) and Typical Power Dissipation of 3.4 mW per Gate**
- **'AS804B has Typical Delay Time of 2.6 ns (C_L = 50 pF) and Typical Power Dissipation of Less than 9 mW per gate**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS804, SN54AS804B . . . J PACKAGE
SN74ALS804, SN74AS804B . . . N PACKAGE
SN74ALS804, SN74AS804B . . . DW PACKAGE
(TOP VIEW)



SN54ALS804, SN54AS804B . . . FH OR FK PACKAGE
SN74ALS804, SN74ALS804B . . . FN PACKAGE
(TOP VIEW)



description

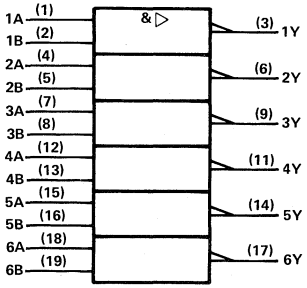
These devices contain six independent 2-input NAND drivers. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54ALS804 and SN54AS804B are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS804 and SN74AS804B are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each driver)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS804 . . . . . −55 °C to 125 °C
SN74ALS804 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS804			SN74ALS804			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS804			SN74ALS804			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} −12 mA	2						
	V_{CC} = 4.5 V,	I_{OH} −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.9	2.5		0.9	2.5	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		7	12		7	12	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS804		SN74ALS804		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2	8	2	6	ns
t_{PHL}			2	9	2	7	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS804B . . . . . −55 °C to 125 °C
SN74AS804B . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS804B			SN74AS804B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS804B			SN74AS804B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V		−135			−135		mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		3.5	5		3.5	5	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		16	27		16	27	mA

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

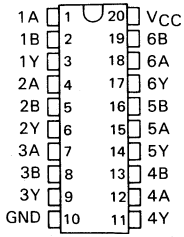
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS804B		SN74AS804B		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	5	1	4	ns
t_{PHL}			1	5	1	4	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

D2661, DECEMBER 1982—REVISED JUNE 1984

- **High Capacitive Drive Capability**
- **'ALS805 Has Typical Delay Time of 4.2 ns (C_L = 50 pF) and Typical Power Dissipation of 4.2 mW per Gate**
- **'AS805B Has Typical Delay Time of 2.6 ns (C_L = 50 pF) and Typical Power Dissipation of 12 mW per Gate**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS805, SN54AS805B . . . J PACKAGE
SN74ALS805, SN74AS805B . . . N PACKAGE
SN74ALS805, SN74AS805B . . . DW PACKAGE
(TOP VIEW)



2

description

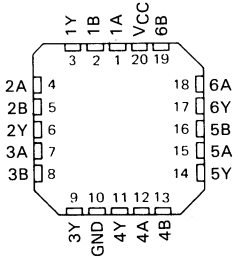
These devices contain six independent 2-input NOR drivers. They perform the Boolean functions $Y = \overline{A+B}$ or $Y = \overline{A \cdot B}$ in positive logic.

The SN54ALS805 and SN54AS805B are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS805 and SN74AS805B are characterized for operation from 0°C to 70°C.

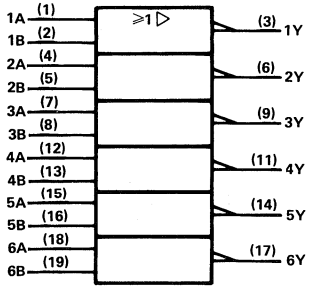
FUNCTION TABLE (each driver)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

SN54ALS805, SN54AS805B . . . FH OR FK PACKAGE
SN74ALS805, SN74AS805B . . . FN PACKAGE
(TOP VIEW)



logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS805 . . . . . −55 °C to 125 °C
SN74ALS805 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS805			SN74ALS805			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS805			SN74ALS805			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		2	4		2	4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		8	14		8	14	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS805		SN74ALS805		
			MIN	MAX	MIN	MAX	
t_{PLH}	Aor B	Y	2	8	2	6	ns
t_{PHL}			2	9	2	7	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS805B . . . . . −55 °C to 125 °C
SN74AS805B . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS805B			SN74AS805B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS805B			SN74AS805B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V		−135			−135		mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		6.5	10		6.5	10	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		20	32		20	32	mA

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

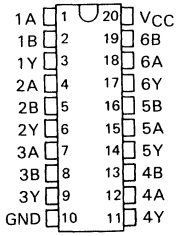
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS805B		SN74AS805B		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	4.8	1	4.3	ns
t_{PHL}			1	4.8	1	4.3	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

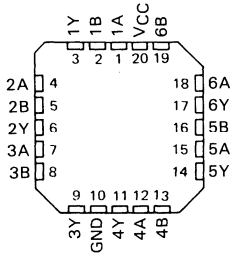
D2661, DECEMBER 1982–REVISED JUNE 1984

- **High Capacitive Drive Capability**
- **'ALS808 Has Typical Delay Time of 4.8 ns (C_L = 50 pF) and Typical Power Dissipation of 4.5 mW per Gate**
- **'AS808B Has Typical Delay Time of 3.2 ns (C_L = 50 pF) and Typical Power Dissipation of Less than 13 mW per Gate**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS808, SN54AS808B . . . J PACKAGE
SN74ALS808, SN74AS808B . . . N PACKAGE
SN74ALS808, SN74AS808B . . . DW PACKAGE
(TOP VIEW)



SN54ALS808, SN54AS808B . . . FH OR FK PACKAGE
SN74ALS808, SN74AS808B . . . FN PACKAGE
(TOP VIEW)



description

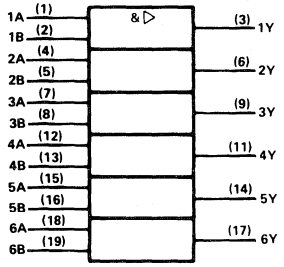
These devices contain six independent 2-input AND drivers. They perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

The SN54ALS808 and SN54AS808B are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS808 and SN74AS808B are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each driver)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS808 . . . . . −55 °C to 125 °C
SN74ALS808 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS808			SN74ALS808			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS808			SN74ALS808			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
	V_{CC} = 4.5 V,	I_{OL} = 15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4 5		3	6		3	6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		8	16		8	16	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS808		SN74ALS808		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2	10	2	8	ns
t_{PHL}			2	10	2	8	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS808B . . . . . −55 °C to 125 °C
SN74AS808B . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS808B			SN74AS808B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS808B			SN74AS808B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V		−135			−135		mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		8	13		8	13	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		20	33		20	33	mA

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

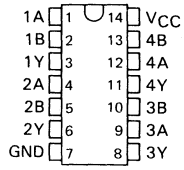
switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS808B		SN74AS808B		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	6.5	1	6	ns
t_{PHL}			1	6.5	1	6	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS810 . . . J PACKAGE
SN74ALS810 . . . N PACKAGE
SN74ALS810 . . . D PACKAGE
(TOP VIEW)



2

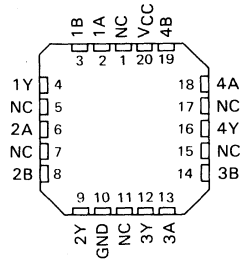
description

These devices contain four independent Exclusive-NOR gates. They perform the Boolean functions $Y = \overline{A \oplus B} = (A+\overline{B})\cdot(\overline{A}+B)$ in positive logic.

A common application is a true/complement element. If one of the inputs is high, the other input will be reproduced in true form at the output. If one of the inputs is low, the signal on the other input will be reproduced inverted at the output.

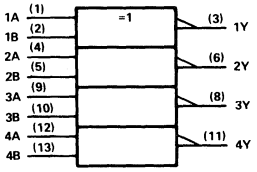
The SN54ALS810 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS810 is characterized for operation from 0°C to 70°C.

SN54ALS810 . . . FH OR FK PACKAGE
SN74ALS810 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

logic symbol



Pin numbers shown are for J and N packages.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

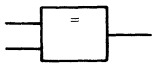
exclusive-NOR logic

An exclusive-NOR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE-NOR

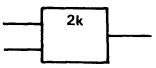
These are five equivalent Exclusive-NOR symbols valid for an 'ALS810 gate in positive logic; negation may be shown at any one port, or at all three of them.

LOGIC IDENTITY ELEMENT



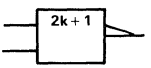
The output is active (High) if all inputs stand at the same logic level (i.e., A = B).

EVEN-PARITY



The output is active (High) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (Low) if an odd number of inputs (i.e., only 1 of the 2) are active.

PRODUCT PREVIEW
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS810 . . . . . −55°C to 125°C
SN74ALS810 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS810			SN74ALS810			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS810			SN74ALS810			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V,	A at 4.5 V, B at 0 V		5	7.5		5	7.5	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

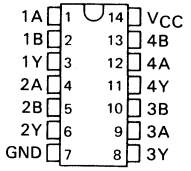
switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS810		SN74ALS810		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	5	23	5	20	ns
t_{PHL}	(other input low)		3	17	3	14	
t_{PLH}	A or B	Y	5	21	5	18	ns
t_{PHL}	(other input high)		3	17	3	14	

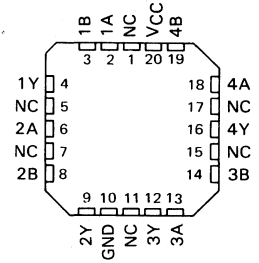
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS811 . . . J PACKAGE
SN74ALS811 . . . N PACKAGE
SN74ALS811 . . . D PACKAGE
(TOP VIEW)



SN54ALS811 . . . FH OR FK PACKAGE
SN74ALS811 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

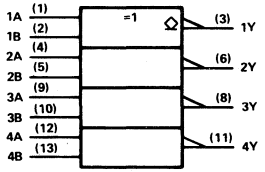
description

These devices contain four independent Exclusive-NOR gates with open-collector outputs. They perform the Boolean functions $Y = \overline{A \oplus B} = (A+\overline{B})\cdot(\overline{A}+B)$ in positive logic.

A common application is a true/complement element. If one of the inputs is high, the other input will be reproduced in true form at the output. If one of the inputs is low, the signal on the other input will be reproduced inverted at the output.

The SN54ALS811 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS811 is characterized for operation from 0°C to 70°C.

logic symbol



Pin numbers shown are for J and N packages.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

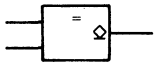
exclusive-NOR logic

An exclusive-NOR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE-NOR

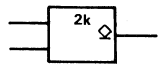
These are five equivalent Exclusive-NOR symbols valid for an 'ALS811 gate in positive logic; negation may be shown at any one port, or at all three of them.

LOGIC IDENTITY ELEMENT



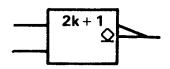
The output is active (high) if all inputs stand at the same logic level (i.e., A = B).

EVEN-PARITY



The output is active (high) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (low) if an odd number of inputs (i.e., only 1 of the 2) are active.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS811 . . . . . −55°C to 125°C
SN74ALS811 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS811			SN74ALS811			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS811			SN74ALS811			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CC}	V_{CC} = 5.5 V,	A at 4.5 V, B at 0 V		5	7.5		5	7.5	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = MIN to MAX				UNIT
			SN54ALS811		SN74ALS811		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	25	60	25	55	ns
t_{PHL}	(other input low)		5	30	5	28	
t_{PLH}	A or B	Y	20	55	20	50	ns
t_{PHL}	(other input high)		5	28	5	23	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

D2825, DECEMBER 1983

- 10-Bit Versions of 'AS574 and 'AS576 with Improved I_{OH} Specifications
- Ideal for Data Synchronization of Wider Data Paths
- Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity
- Outputs Have Undershoot Protection Circuitry
- Power-Up High-Impedance State
- Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Buffered Control Inputs to Reduce DC Loading Effects
- Dependable Texas Instruments Quality and Reliability

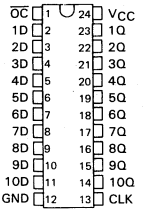
description

These 10-bit flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

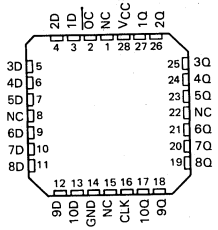
The ten flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock the Q outputs on the 'AS821 will be true, and on the 'AS822 will be complementary, to the data input.

A buffered output-control input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

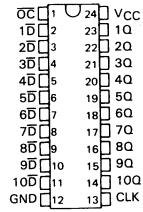
SN54AS821 . . . JT PACKAGE
SN74AS821 . . . NT PACKAGE
SN74AS821 . . . DW PACKAGE
(TOP VIEW)



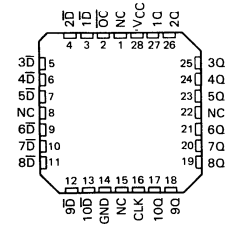
SN54AS821 . . . FH OR FK PACKAGE
SN74AS821 . . . FN PACKAGE
(TOP VIEW)



SN54AS822 . . . JT PACKAGE
SN74AS822 . . . NT PACKAGE
SN74AS822 . . . DW PACKAGE
(TOP VIEW)



SN54AS822 . . . FH OR FK PACKAGE
SN74AS822 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

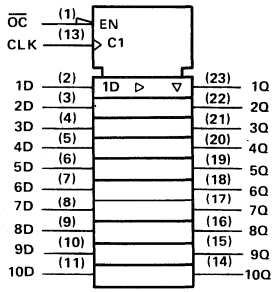
The output control ($\overline{OC}$) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AS821 and SN54AS822 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74AS821 and SN74AS822 are characterized for operation from 0 °C to 70 °C.

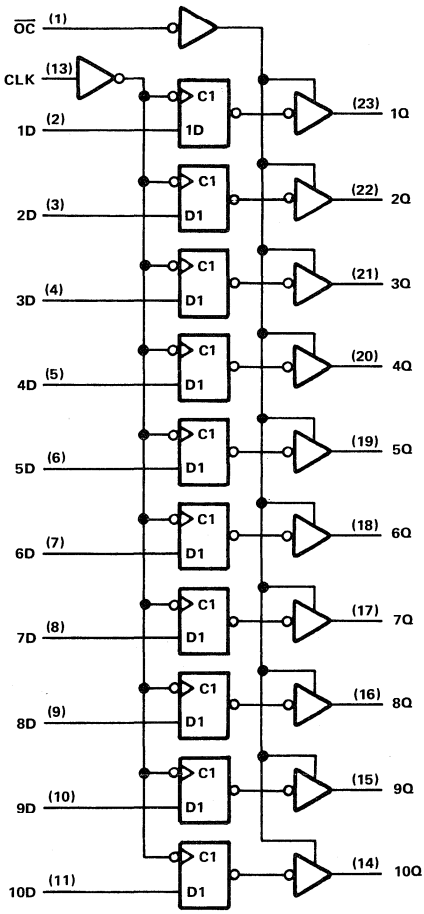
'AS821 FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

'AS821 logic symbol



'AS821 logic diagram (positive logic)

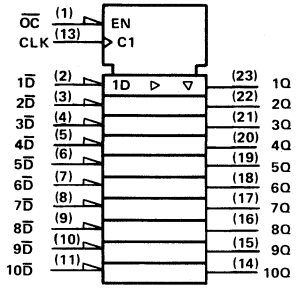


Pin numbers shown are for JT and NT packages.

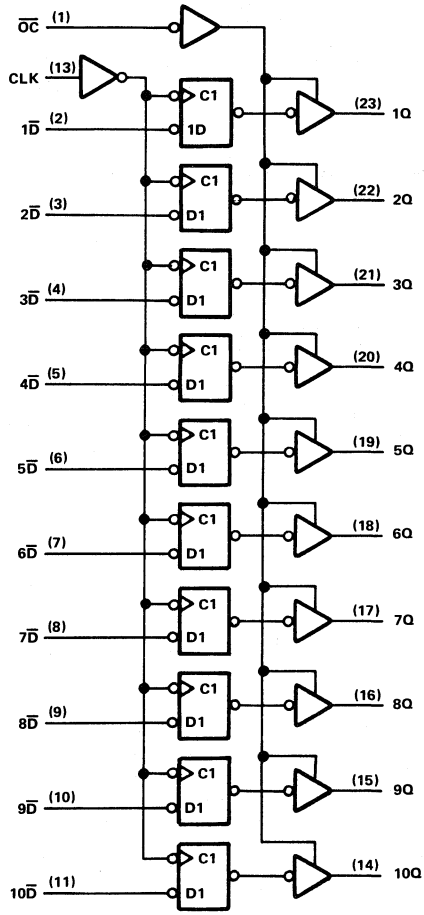
'AS822 FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	$\overline{D}$	Q
L	↑	H	L
L	↑	L	H
L	L	X	Q_0
H	X	X	Z

'AS822 logic symbol



'AS822 logic diagram (positive logic)



Pin numbers shown are for JT and NT packages

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS821, SN54AS822 . . . . . −55°C to 125°C
SN74AS821, SN74AS822 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS821 SN54AS822			SN74AS821 SN74AS822			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−24			−24	mA
I_{OL}	Low-level output current			32			48	mA
t_w	Pulse duration, CLK high or low	9			8			ns
t_{su}	Setup time, data before CLK↑	7			6			ns
t_h	Hold time, data after CLK↑	0			0			ns
T_A	Operating free-air temperature	−55		−125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS821 SN54AS822			SN74AS821 SN74AS822			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −24 mA	2			2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS821	V_{CC} = 5.5 V	Outputs high		55	88		55	88	mA
			Outputs low		68	109		68	109	
			Outputs disabled		70	113		70	113	
	'AS822		Outputs high		55	88		55	88	
			Outputs low		68	109		68	109	
			Outputs disabled		70	113		70	113	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS821 SN54AS822		SN74AS821 SN74AS822		
			MIN	MAX	MIN	MAX	
t_{PLH}	CLK	Any Q	3.5	9	3.5	7.5	ns
t_{PHL}			3.5	11.5	3.5	10.5	
t_{PZH}	$\overline{OC}$	Any Q	4	12	4	11	ns
t_{PZL}			4	13	4	12	
t_{PHZ}	$\overline{OC}$	Any Q	2	10	2	8	ns
t_{PZL}			2	10	2	8	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

D2825, JUNE 1984

- Similar to 'AS574 and 'AS576 with Clock Enable and Clear and Improved I_{OH} Specifications
- Ideal for Data Synchronization of Wider Data Paths
- Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity
- Outputs Have Undershoot Protection Circuitry
- Power-Up High-Impedance State
- Buffered Control Inputs to Reduce DC Loading Effects
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- Dependable Texas Instruments Quality and Reliability

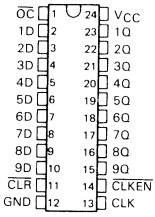
description

These 9-bit flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing and working registers.

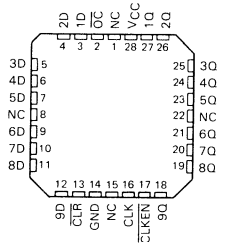
With the clock enable ($\overline{CLKEN}$) low, the nine D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{CLKEN}$ high will disable the clock buffer, thus latching the outputs. The 'AS823 has noninverting D inputs and the 'AS824 has inverting $\overline{D}$ inputs. Taking the $\overline{CLR}$ input low causes the nine Q outputs to go low independently of the clock.

A buffered output-control input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

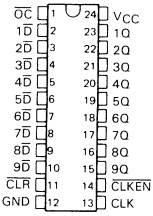
SN54AS823 . . . JT PACKAGE
SN74AS823 . . . NT PACKAGE
SN74AS823 . . . DW PACKAGE
(TOP VIEW)



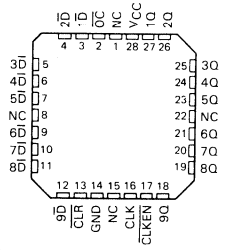
SN54AS823 . . . FH OR FK PACKAGE
SN74AS823 . . . FN PACKAGE
(TOP VIEW)



SN54AS824 . . . JT PACKAGE
SN74AS824 . . . NT PACKAGE
SN74AS824 . . . DW PACKAGE
(TOP VIEW)



SN54AS824 . . . FH OR FK PACKAGE
SN74AS824 . . . FN PACKAGE
(TOP VIEW)



The output control ($\overline{OC}$) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AS823 and SN54AS824 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS823 and SN74AS824 are characterized for operation from 0°C to 70°C.

FUNCTION TABLES

'AS823

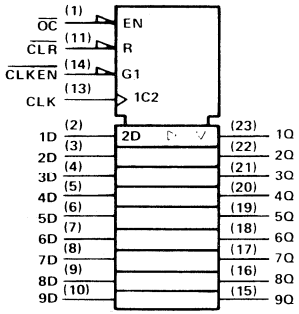
INPUTS					OUTPUT
$\overline{OC}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

'AS824

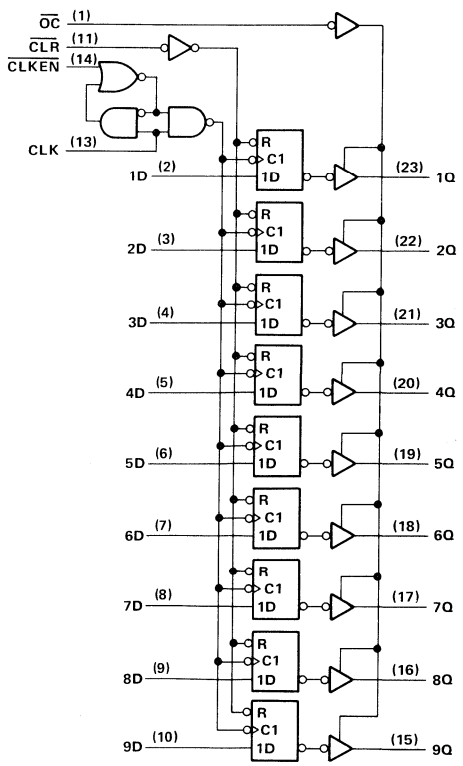
INPUTS					OUTPUT
$\overline{OC}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	$\overline{D}$	Q
L	L	X	X	X	L
L	H	L	↑	H	L
L	H	L	↑	L	H
L	H	H	X	X	Q_0
H	X	X	X	X	Z

2

'AS823 logic symbol

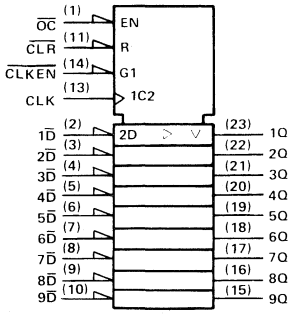


'AS823 logic diagram (positive logic)

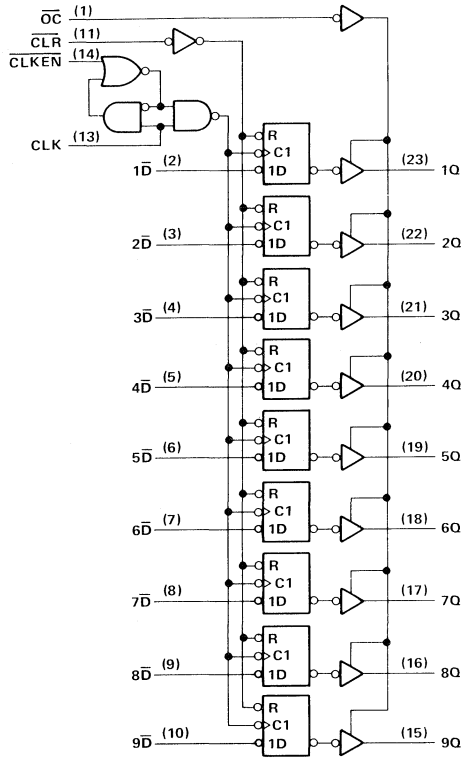


Pin numbers shown are for JT and NT packages.

'AS824 logic symbol



'AS824 logic diagram (positive logic)



Pin numbers shown are for JT and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS823, SN54AS824 . . . . . −55°C to 125°C
SN74AS823, SN74AS824 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS823 SN54AS824			SN74AS823 SN74AS824			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−24			−24	mA
I_{OL}	Low-level output current				32			48	mA
t_w	Pulse duration	$\overline{CLR}$ low	5			4			ns
		CLK high	9			8			
		CLK low	9			8			
		$\overline{CLKEN}$	7			6			
t_{su}	Setup time before CLK↑	$\overline{CLR}$ inactive	8			8			ns
		Data	7			6			
		$\overline{CLKEN}$	7			6			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS823 SN54AS824			SN74AS823 SN74AS824			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −24 mA	2			2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.3	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS823	V_{CC} = 5.5 V	Outputs high		49	80		49	80	mA
			Outputs low		61	100		61	100	
			Outputs disabled		64	103		64	103	
	'AS824	V_{CC} = 5.5 V	Outputs high		49	80		49	80	mA
			Outputs low		61	100		61	100	
			Outputs disabled		64	103		64	103	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS823 SN54AS824		SN74AS823 SN74AS824		
			MIN	MAX	MIN	MAX	
t_{PLH}	CLK	Any Q	3.5	9	3.5	7.5	ns
t_{PHL}			3.5	12	3.5	11	
t_{PHL}	$\overline{CLR}$	Any Q	3.5	14	3.5	13	ns
t_{PZH}	$\overline{OC}$	Any Q	4	12	4	11	ns
t_{PZL}			4	13	4	12	
t_{PHZ}	$\overline{OC}$	Any Q	2	10	2	8	ns
t_{PLZ}			2	10	2	8	

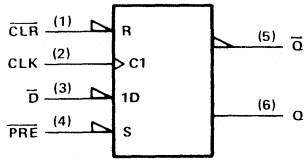
NOTE 1: For load circuit and voltage waveforms, see page 1-12, of The TTL Data Book, Volume 3, 1984.

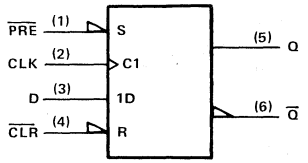
D flip-flop signal conventions

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active-low.

The devices on this data sheet are second-source designs and the pin-name convention used by the original manufacturer has been retained. That makes it necessary to designate the inputs and outputs of the inverting circuit $\overline{D}$ and Q. In some applications it may be advantageous to redesignate the inputs and outputs as D and $\overline{Q}$. In that case, outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.

Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (▷) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 (Q) is still in phase with the data input D, but now both are considered active high.





D2825, JUNE 1984

- Similar to 'AS574 and 'AS576 with Clock Enable, Clear, and Multiple Output Controls
- Improved I_{OH} Specifications
- Multiple Output Enables Allow Multiuser Control of the Interface
- Outputs Have Undershoot Protection Circuitry
- Power-Up High-Impedance State
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- Buffered Control Inputs to Reduce DC Loading Effect
- Dependable Texas Instruments Quality and Reliability

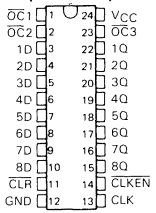
description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing multiuser registers, I/O ports, bidirectional bus drivers, and working registers.

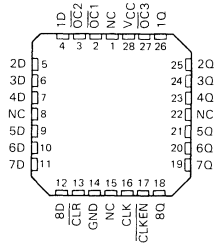
With the clock enable ($\overline{CLKEN}$) low, the eight D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{CLKEN}$ high will disable the clock buffer, thus latching the outputs. The 'AS825 has noninverting D inputs and the 'AS826 has inverting $\overline{D}$ inputs. Taking the $\overline{CLR}$ input low causes the eight Q outputs to go low independently of the clock.

A multiuser buffered output-control input can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

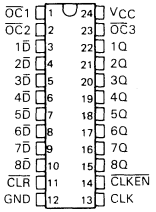
SN54AS825 . . . JT PACKAGE
SN74AS825 . . . NT PACKAGE
SN74AS825 . . . DW PACKAGE
(TOP VIEW)



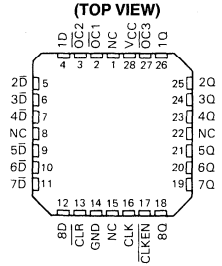
SN54AS825 . . . FH OR FK PACKAGE
SN74AS825 . . . FN PACKAGE
(TOP VIEW)



SN54AS826 . . . JT PACKAGE
SN74AS826 . . . NT PACKAGE
SN74AS826 . . . DW PACKAGE
(TOP VIEW)



SN54AS826 . . . FH OR FK PACKAGE
SN74AS826 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

The output controls ($\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$) do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AS825 and SN54AS826 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS825 and SN74AS826 are characterized for operation from 0°C to 70°C.

FUNCTION TABLES

'AS825

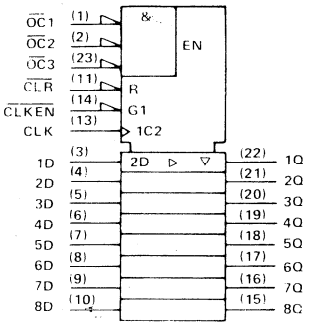
INPUTS					OUTPUT
$\overline{OC}$*	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

'AS826

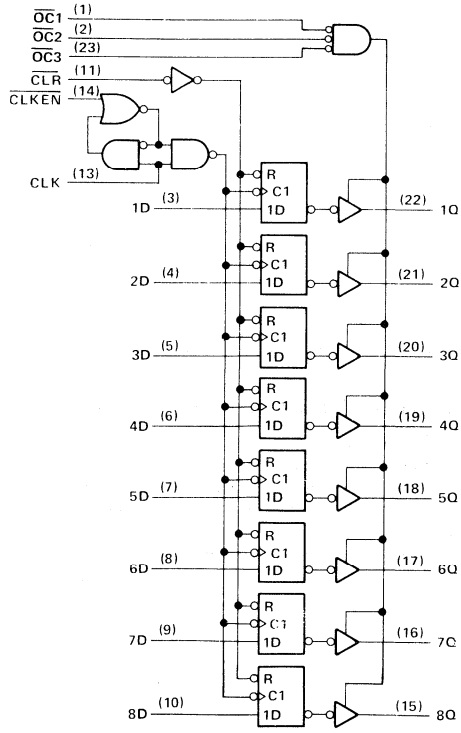
INPUTS					OUTPUT
$\overline{OC}$*	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	L
L	H	L	↑	L	H
L	H	H	X	X	Q_0
H	X	X	X	X	Z

$\overline{OC}$* $\overline{OC}1 \cdot \overline{OC}2 \cdot \overline{OC}3$

'AS825 logic symbol

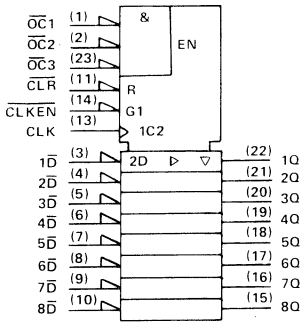


'AS825 logic diagram (positive logic)

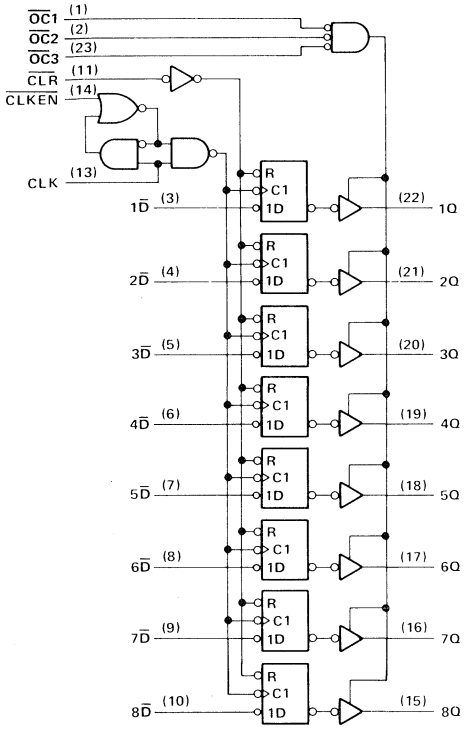


Pin numbers shown are for JT and NT packages.

'AS826 logic symbol



'AS826 logic diagram (positive logic)



Pin numbers shown are for NT and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS825, SN54AS826 . . . . . −55°C to 125°C
SN74AS825, SN74AS826 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65 to 150°C

recommended operating conditions

			SN54AS825 SN54AS826			SN74AS825 SN74AS826			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−24			−24	mA
I_{OL}	Low-level output current				32			48	mA
t_w	Pulse duration	$\overline{CLR}$ low	5			4			ns
		CLK high	9			8			
		CLK low	9			8			
		$\overline{CLKEN}$	7			6			
t_{su}	Setup time before CLK↑	$\overline{CLR}$ inactive	8			8			ns
		Data	7			6			
		$\overline{CLKEN}$	7			6			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS825 SN54AS826			SN74AS825 SN74AS826			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −24 mA	2			2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.3	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS825	V_{CC} = 5.5 V	Outputs high		45	73		45	73	mA
			Outputs low		56	90		56	90	
			Outputs disabled		59	95		59	95	
	'AS826	V_{CC} = 5.5 V	Outputs high		45	73		45	73	mA
			Outputs low		56	90		56	90	
			Outputs disabled		59	95		59	95	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS825 SN54AS826		SN74AS825 SN74AS826		
			MIN	MAX	MIN	MAX	
t_{PLH}	CLK	Any Q	3.5	9	3.5	7.5	ns
t_{PHL}			3.5	11.5	3.5	11	
t_{PHL}	$\overline{CLR}$	Any Q	3.5	14	3.5	13	ns
t_{PZH}	$\overline{OC}$	Any Q	4	12	4	11	ns
t_{PZL}			4	13	4	12	
t_{PHZ}	$\overline{OC}$	Any Q	2	10	2	8	ns
t_{PLZ}			2	10	2	8	

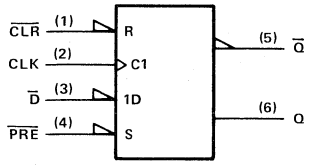
NOTE 1: For load circuit and voltage waveforms, see page 1-12

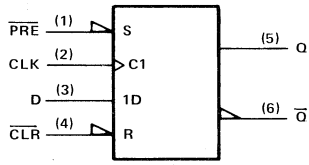
D flip-flop signal conventions

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active-low.

The devices on this data sheet are second-source designs and the pin-name convention used by the original manufacturer has been retained. That makes it necessary to designate the inputs and outputs of the inverting circuit $\overline{D}$ and Q. In some applications it may be advantageous to redesignate the inputs and outputs as D and $\overline{Q}$. In that case, outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.

Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (◺) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 (Q) is still in phase with the data input D, but now both are considered active high.

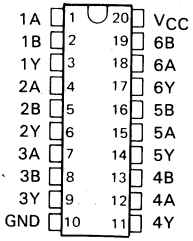




D2661, DECEMBER 1982—REVISED JUNE 1984

- **High Capacitive Drive Capability**
- **'ALS832 Has Typical Delay Time of 5 ns (C_L = 50 pF) and Typical Power Dissipation of 5.3 mW per Gate**
- **'AS832B Has Typical Delay Time of 3.9 ns (C_L = 50 pF) and Typical Power Dissipation of Less than 17 mW per Gate**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS832, SN54AS832B . . . J PACKAGE
SN74ALS832, SN74AS832B . . . N PACKAGE
SN74ALS832, SN74AS832B . . . DW PACKAGE
(TOP VIEW)



2

description

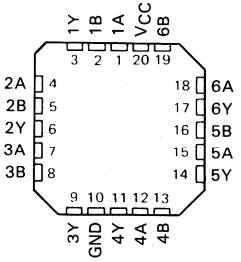
These devices contain six independent 2-input OR drivers. They perform the Boolean functions $Y = A+B$ or $Y = \overline{\overline{A} \cdot \overline{B}}$ in positive logic.

The SN54ALS832 and SN54AS832B are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS832 and SN74AS832B are characterized for operation from 0°C to 70°C.

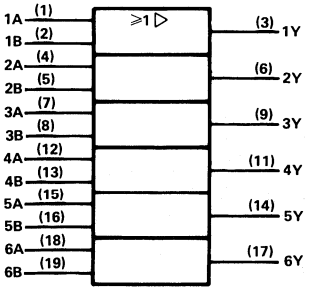
FUNCTION TABLE (each driver)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

SN54ALS832, SN54AS832B . . . FH OR FK PACKAGE
SN74ALS832, SN74AS832B . . . FN PACKAGE
(TOP VIEW)



logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS832 . . . . . −55 °C to 125 °C
SN74ALS832 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS832			SN74ALS832			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS832			SN74ALS832			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		4	8		4	8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		9.5	16		9.5	16	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS832		SN74ALS832		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2	10	2	8	ns
t_{PHL}			2	10	2	8	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS832B . . . . . −55 °C to 125 °C
SN74AS832B . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS832B			SN74AS832B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS832B			SN74AS832B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V		−135			−135		mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		11	17		11	17	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		22	36		22	36	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS832B		SN74AS832B		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	7	1	6.3	ns
t_{PHL}			1	7	1	6.3	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

TYPES SN54ALS841, SN54AS841, SN54ALS842, SN54AS842
SN74ALS841, SN74AS841, SN74ALS842, SN74AS842
10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

DECEMBER 1983 – REVISED FEBRUARY 1984

- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **Provide Extra Bus Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity**
- **Buffered Control Inputs to Reduce DC Loading**
- **Power-Up High-Impedance State**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 10-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

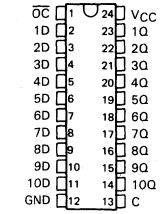
The ten latches are transparent D-type. The 'ALS841 and 'AS841 have noninverting data (D) inputs. The 'ALS842 and 'AS842 have inverting $\overline{D}$ inputs.

A buffered output control ($\overline{OC}$) input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

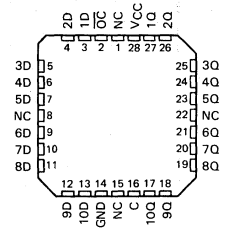
The output control does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN54ALS841, SN54AS841, SN54ALS842, and SN54AS842 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS841, SN74ALS842, and SN74AS842 are characterized for operation from 0°C to 70°C.

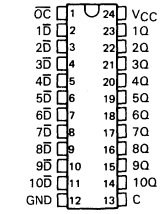
SN54ALS841, SN54AS841 . . . JT PACKAGE
SN74ALS841, SN74AS841 . . . NT PACKAGE
SN74ALS841, SN74AS841 . . . DW PACKAGE
(TOP VIEW)



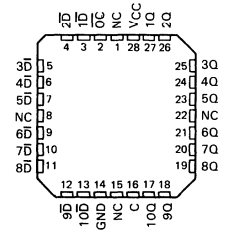
SN54ALS841, SN54AS841 . . . FH OR FK PACKAGE
SN74ALS841, SN74AS841 . . . FN PACKAGE
(TOP VIEW)



SN54ALS842, SN54AS842 . . . JT PACKAGE
SN74ALS842, SN74AS842 . . . NT PACKAGE
SN74ALS842, SN74AS842 . . . DW PACKAGE
(TOP VIEW)



SN54ALS842, SN54AS842 . . . FH OR FK PACKAGE
SN74ALS842, SN74AS842 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

FUNCTION TABLES

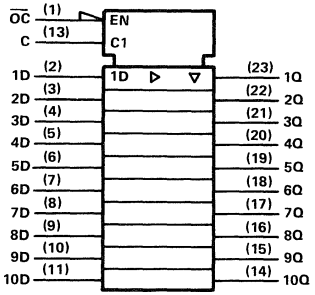
'ALS841, 'AS841

INPUTS			OUTPUT
$\overline{OC}$	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

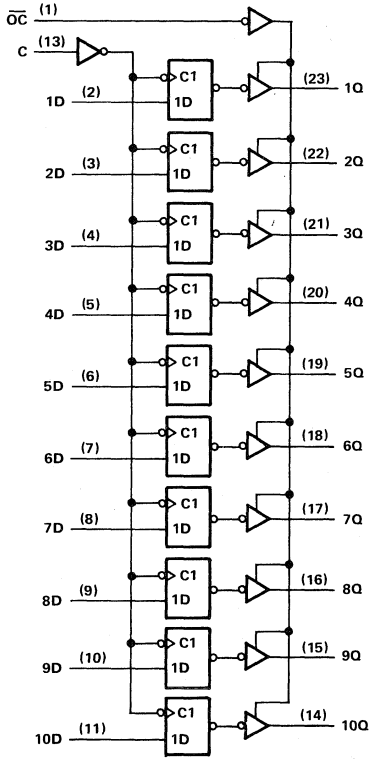
'ALS842, 'AS842

INPUTS			OUTPUT
$\overline{OC}$	C	$\overline{D}$	Q
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

'ALS841, 'AS841 logic symbol

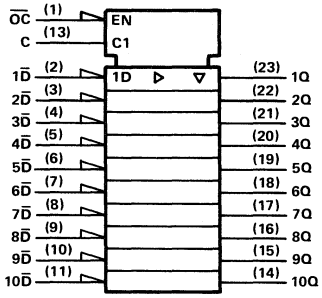


'ALS841, 'AS841 logic diagram (positive logic)

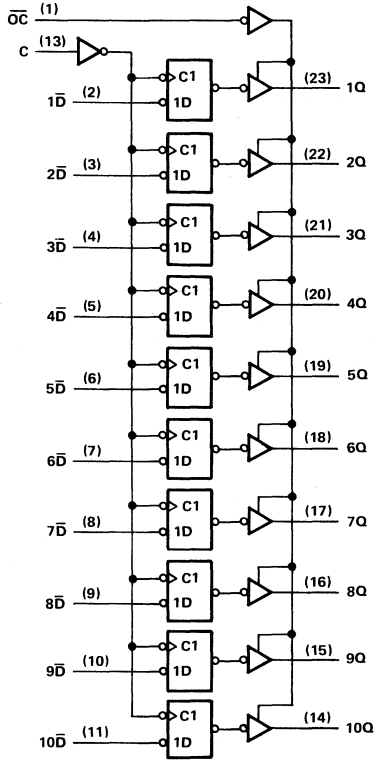


Pin numbers shown are for JT and NT packages.

'ALS842, 'AS842 logic symbol



'ALS842, 'AS842 logic diagram (positive logic)



Pin numbers shown are for JT and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range:
SN54ALS841, SN54AS841, SN54ALS842, SN54AS842 . . . . . −55°C to 125°C
SN74ALS841, SN74AS841, SN74ALS842, SN74AS842 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS841 SN54ALS842			SN74ALS841 SN74ALS842			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
t_w	Pulse duration, enable C high	'ALS841							ns
		'ALS842							
t_{su}	Setup time, data before enable C↓								ns
t_h	Hold time, data after enable C↓	'ALS841							ns
		'ALS842							
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS841 SN54ALS842			SN74ALS841 SN74ALS842			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}	'ALS841	V_{CC} = 5.5 V	Outputs high							mA
			Outputs low							
			Outputs disabled		25			25		
	'ALS842		Outputs high							
			Outputs low							
			Outputs disabled		28			28		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

'ALS841 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS841			SN74ALS841			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	D	Q		7			7		ns
t_{PHL}				9			9		
t_{PLH}	C	Q							ns
t_{PHL}									
t_{PZH}	$\overline{OC}$	Q							ns
t_{PZL}									
t_{PHZ}	$\overline{OC}$	Q							ns
t_{PLZ}									

'ALS842 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS842			SN74ALS842			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	$\overline{D}$	Q		11			11		ns
t_{PHL}				9			9		
t_{PLH}	C	Q							ns
t_{PHL}									
t_{PZH}	$\overline{OC}$	Q							ns
t_{PZL}									
t_{PHZ}	$\overline{OC}$	Q							ns
t_{PLZ}									

†All typical values are at T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12

Additional information on these products can be obtained from the factory as it becomes available.

recommended operating conditions

		SN54AS841 SN54AS842			SN74AS841 SN74AS842			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−24			−24	mA
I_{OL}	Low-level output current			32			48	mA
t_w	Pulse duration, enable C high	5			4			ns
t_{su}	Setup time, data before enable C↓	3.5			2.5			ns
t_h	Hold time, data after enable C↓	3.5			2.5			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS841 SN54AS842			SN74AS841 SN74AS842			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA				−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V, I_{OH} = −2 mA		V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V, I_{OH} = −15 mA		2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V, I_{OH} = −24 mA		2			2			
V_{OL}		V_{CC} = 4.5 V, I_{OL} = 32 mA			0.25	0.5				V
		V_{CC} = 4.5 V, I_{OL} = 48 mA						0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V, V_O = 2.7 V				50			50	μA
I_{OZL}		V_{CC} = 5.5 V, V_O = 0.4 V				−50			−50	μA
I_I		V_{CC} = 5.5 V, V_I = 7 V				0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V, V_I = 2.7 V				20			20	μA
I_{IL}		V_{CC} = 5.5 V, V_I = 0.4 V				−0.5			−0.5	mA
I_O‡		V_{CC} = 5.5 V, V_O = 2.25 V		−30		−112	−30		−112	mA
I_{CC}	'AS841	V_{CC} = 5.5 V	Outputs high		36	60		36	60	mA
			Outputs low		58	94		58	94	
			Outputs disabled		56	92		56	92	
	'AS842		Outputs high		38	62		38	62	
			Outputs low		60	97		60	97	
			Outputs disabled		58	95		58	95	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS841 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS841		SN74AS841		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1	8.5	1	6.5	ns
t_{PHL}			1	10	1	9	
t_{PLH}	C	Q	2	13	2	12	ns
t_{PHL}			2	13	2	12	
t_{PZH}	$\overline{OC}$	Q	2	13.5	2	10.5	ns
t_{PZL}			2	14.5	2	11.5	
t_{PHZ}	$\overline{OC}$	Q	1	10	1	8	ns
t_{PLZ}			1	10	1	8	

'AS842 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS842		SN74AS842		
			MIN	MAX	MIN	MAX	
t_{PLH}	$\overline{D}$	Q	1	11	1	8.5	ns
t_{PHL}			1	10	1	9	
t_{PLH}	C	Q	2	13	2	12	ns
t_{PHL}			2	13	2	12	
t_{PZH}	$\overline{OC}$	Q	2	14.5	2	12	ns
t_{PZL}			2	15	2	12.5	
t_{PHZ}	$\overline{OC}$	Q	1	10	1	8	ns
t_{PLZ}			1	10	1	8	

NOTE 1: For load circuits and voltage waveforms, see page 1-12

DECEMBER 1983—REVISED FEBRUARY 1984

- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **Provide Extra Bus Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity**
- **Buffered Control Inputs to Reduce DC Loading**
- **Power-Up High Impedance**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 9-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

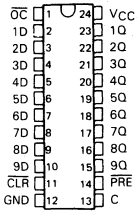
The nine latches are transparent D-type. The 'ALS843 and 'AS843 have noninverting data (D) inputs. The 'ALS844 and 'AS844 have inverting D inputs.

A buffered output control ($\overline{OC}$) input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

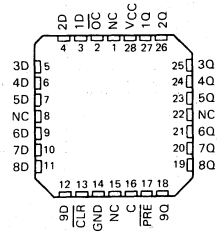
The output control ($\overline{OC}$) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN54ALS843, SN54AS843, SN54ALS844, and SN54AS844 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS843, SN74AS843, SN74ALS844, and SN74AS844 are characterized for operation from 0°C to 70°C.

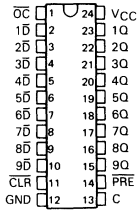
SN54ALS843, SN54AS843 . . . JT PACKAGE
SN74ALS843, SN74AS843 . . . NT PACKAGE
SN74ALS843, SN74AS843 . . . DW PACKAGE
(TOP VIEW)



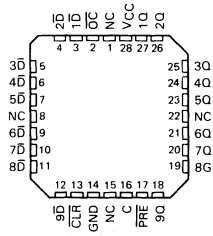
SN54ALS843, SN54AS843 . . . FH OR FK PACKAGE
SN74ALS843, SN74AS843 . . . FN PACKAGE
(TOP VIEW)



SN54ALS844, SN54AS844 . . . JT PACKAGE
SN74ALS844, SN74AS844 . . . NT PACKAGE
SN74ALS844, SN74AS844 . . . DW PACKAGE
(TOP VIEW)



SN54ALS844, SN54AS844 . . . FH OR FK PACKAGE
SN74ALS844, SN74AS844 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

2

FUNCTION TABLES

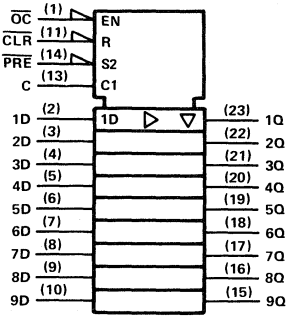
'ALS843, 'AS843

INPUTS					OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC}$	C	D	Q
L	H	L	X	X	H
H	L	L	X	X	L
L	L	L	X	X	H
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Q_O
X	X	H	X	X	Z

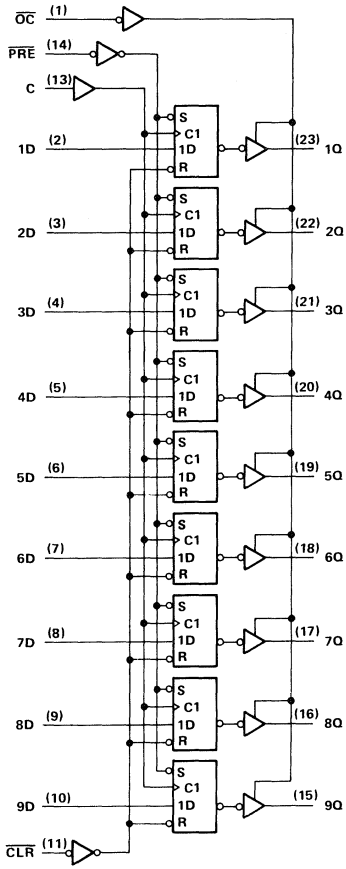
'ALS844, 'AS844

INPUTS					OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC}$	C	$\overline{D}$	Q
L	H	L	X	X	H
H	L	L	X	X	L
L	L	L	X	X	H
H	H	L	H	L	H
H	H	L	H	H	L
H	H	L	L	X	Q_O
X	X	H	X	X	Z

logic symbol

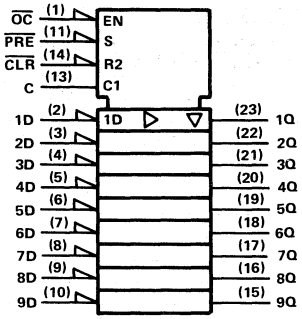


'ALS843, 'AS843 logic diagram (positive logic)

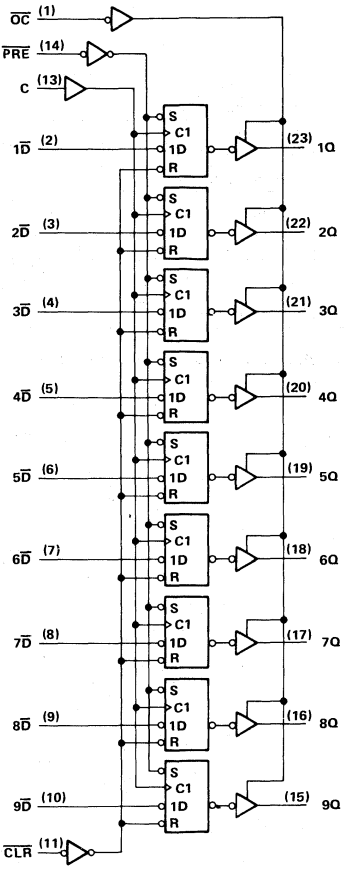


Pin numbers shown are for JT and NT packages.
This symbol is in accordance with IEEE Std 9 and recent decisions of IEEE.

logic symbol



'ALS844, 'AS844 logic diagram (positive logic)



Pin numbers shown are for JT and NT packages.
This symbol is in accordance with IEEE Std 9 and recent decisions of IEEE.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS843, SN54AS844 . . . . . −55°C to 125°C
SN74AS843, SN74AS844 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS843 SN54ALS844			SN74ALS843 SN74ALS844			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	55	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
t_w	Pulse duration, enable C high	'ALS843							ns
		'ALS844							
t_{su}	Setup time, data before enable C↓								ns
t_h	Hold time, data after enable C↓	'ALS843							ns
		'ALS844							
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS843 SN54ALS844			SN74ALS843 SN74ALS844			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}	'ALS843	V_{CC} = 5.5 V	Outputs high							mA
			Outputs low							
			Outputs disabled		25			25		
	'ALS844		Outputs high							
			Outputs low							
			Outputs disabled		28			28		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

'ALS843 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS843			SN74ALS843			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	D	Q		7			7		ns
t_{PHL}				9			9		
t_{PLH}	C	Q							ns
t_{PHL}									
t_{PLH}	$\overline{PRE}$	Q							ns
t_{PHL}	$\overline{CLR}$	Q							ns
t_{PZH}	$\overline{OC}$	Q							ns
t_{PZL}									
t_{PHZ}	$\overline{OC}$	Q							ns
t_{PLZ}									

'ALS844 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS844			SN74ALS844			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	$\overline{D}$	Q		7			7		ns
t_{PHL}				9			9		
t_{PLH}	C	Q							ns
t_{PHL}									
t_{PLH}	$\overline{PRE}$	Q							ns
t_{PHL}	$\overline{CLR}$	Q							ns
t_{PZH}	$\overline{OC}$	Q							ns
t_{PZL}									
t_{PHZ}	$\overline{OC}$	Q							ns
t_{PLZ}									

†All typical values are at T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12

Additional information on these products can be obtained from the factory as it becomes available.

recommended operating conditions

			SN54AS843 SN54AS844			SN74AS843 SN74AS844			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	55	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−24			−24	mA
I_{OL}	Low-level output current				32			48	mA
t_w	Pulse duration, enable C high	$\overline{CLR}$ or $\overline{PRE}$ low	5			4			ns
		C high	5			4			
t_{su}	Setup time, data before enable C↓		3.5			2.5			ns
t_h	Hold time, data after enable C↓		3.5			2.5			ns
t_r	Recovery time	$\overline{PRE}$	17			15			ns
		$\overline{CLR}$	16			14			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS843 SN54AS844			SN74AS843 SN74AS844			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} −24 mA	2						
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS843	V_{CC} = 5.5 V,	Outputs high		37	62		37	62	mA
			Outputs low		56	92		56	92	
			Outputs disabled		56	92		56	92	
	'AS844		Outputs high		39	64		39	64	
			Outputs low		58	95		58	95	
			Outputs disabled		58	95		58	95	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS843 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS843		SN74AS843		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1	8.5	1	6.5	ns
t_{PHL}			1	10	1	9	
t_{PLH}	C	O	2	13	2	12	ns
t_{PHL}			2	13	2	12	
t_{PLH}	$\overline{PRE}$	Q	2	12	2	10	ns
t_{PHL}	$\overline{CLR}$	Q	2	14	2	13	ns
t_{PZH}	$\overline{OC}$	Q	2	13.5	2	10.5	ns
t_{PZL}			2	14.5	2	11.5	
t_{PHZ}	$\overline{OC}$	Q	1	10	1	8	ns
t_{PLZ}			1	10	1	8	

'ALS844 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS844		SN74AS844		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1	11	1	8.5	ns
t_{PHL}			1	11	1	10	
t_{PLH}	C	O	2	14	2	12.5	ns
t_{PHL}			2	14	2	13	
t_{PLH}	$\overline{PRE}$	Q	2	12	2	10	ns
t_{PHL}	$\overline{CLR}$	Q	2	14.5	2	13.5	ns
t_{PZH}	$\overline{OC}$	Q	2	14.5	2	12	ns
t_{PZL}			2	15	2	13.5	
t_{PHZ}	$\overline{OC}$	Q	1	10	1	8	ns
t_{PLZ}			1	10	1	8	

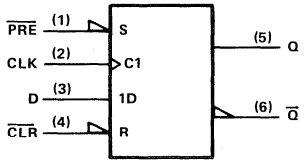
NOTE 1: For load circuit and voltage waveforms, see page 1-12

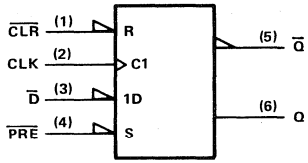
D flip-flop signal conventions

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called $\overline{Q}$ and those producing complementary data are called Q. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active-low.

The devices on this data sheet are second-source designs and the pin-name convention used by the original manufacturer has been retained. That makes it necessary to designate the inputs and outputs of the inverting circuit $\overline{D}$ and Q. In some applications it may be advantageous to redesignate the inputs and outputs as D and $\overline{Q}$. In that case, outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.

Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (▷) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 (Q) is still in phase with the data input D, but now both are considered active high.





8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

D2825, DECEMBER 1983—REVISED JUNE 1984

- 3-State Buffer-Type Outputs Drive Bus-Lines Directly
- Bus-Structured Pinout
- Provides Extra Bus Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity
- Buffered Control Inputs to Reduce DC Loading
- Power-Up High-Impedance State
- Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

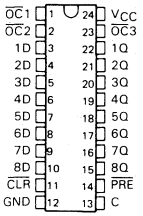
description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

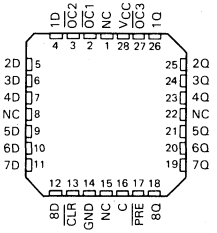
The eight latches are transparent D-type. The 'ALS845 and 'AS845 have noninverting data (D) inputs. The 'ALS846 and 'AS846 have inverting $\overline{D}$ inputs. Since $\overline{CLR}$ and $\overline{PRE}$ are independent of the clock, taking the $\overline{CLR}$ input low will cause the eight Q outputs to go low. Taking the $\overline{PRE}$ input low will cause the eight Q outputs to go high. When both $\overline{PRE}$ and $\overline{CLR}$ are taken low, the outputs will follow the preset condition.

A buffered output control ($\overline{OC}$) input can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

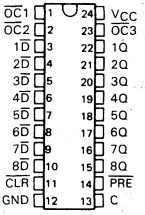
SN54ALS845, SN54AS845 . . . JT PACKAGE
SN74ALS845, SN74AS845 . . . NT PACKAGE
SN74ALS845, SN74AS845 . . . DW PACKAGE
(TOP VIEW)



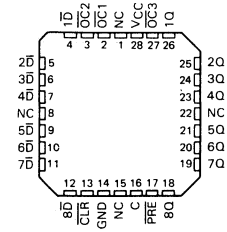
SN54ALS845, SN54AS845 . . . FH OR FK PACKAGE
SN74ALS845, SN74AS845 . . . FN PACKAGE
(TOP VIEW)



SN54ALS846, SN54AS846 . . . JT PACKAGE
SN74ALS846, SN74AS846 . . . NT PACKAGE
SN74ALS846, SN74AS846 . . . DW PACKAGE
(TOP VIEW)



SN54ALS846, SN54AS846 . . . FH OR FK PACKAGE
SN74ALS846, SN74AS846 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

The output controls ($\overline{OC1}$, $\overline{OC2}$, $\overline{OC3}$) do not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS845, SN54AS845, SN54ALS846, and SN54AS846 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS845, SN74AS845, SN74ALS846, and SN74AS846 are characterized for operation from 0°C to 70°C.

FUNCTION TABLES

'ALS845, 'AS845

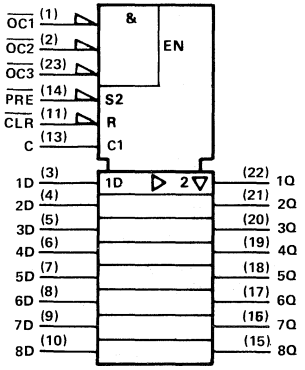
INPUTS							OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC1}$	$\overline{OC2}$	$\overline{OC3}$	C	D	Q
L	H	L	L	L	X	X	H
H	L	L	L	L	X	X	L
L	L	L	L	L	X	X	H
H	H	L	L	L	H	L	L
H	H	L	L	L	H	H	H
H	H	L	L	L	L	X	Q_0
X	X	L	L	H	X	X	Z
X	X	L	H	L	X	X	Z
X	X	L	H	H	X	X	Z
X	X	H	L	L	X	X	Z
X	X	H	L	H	X	X	Z
X	X	H	H	L	X	X	Z
X	X	H	H	H	X	X	Z

'ALS846, 'AS846

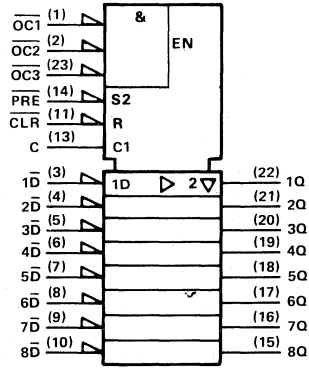
INPUTS							OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC1}$	$\overline{OC2}$	$\overline{OC3}$	C	$\overline{D}$	Q
L	H	L	L	L	X	X	H
H	L	L	L	L	X	X	L
L	L	L	L	L	X	X	H
H	H	L	L	L	H	L	H
H	H	L	L	L	H	H	L
H	H	L	L	L	L	X	Q_0
X	X	L	L	H	X	X	Z
X	X	L	H	L	X	X	Z
X	X	L	H	H	X	X	Z
X	X	H	L	L	X	X	Z
X	X	H	L	H	X	X	Z
X	X	H	H	L	X	X	Z
X	X	H	H	H	X	X	Z

logic symbols

'ALS845, 'AS845



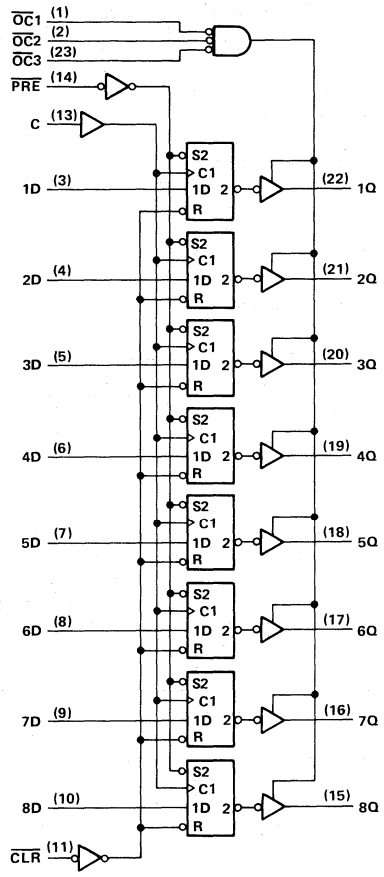
'ALS846, 'AS846



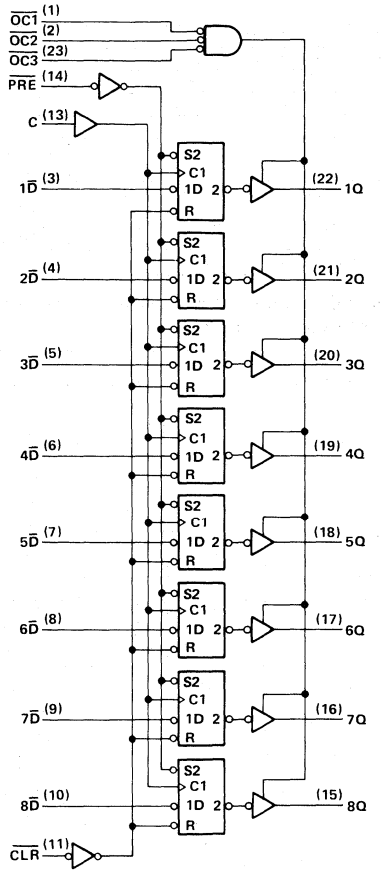
Pin numbers shown are for JT and NT packages.
These symbols are in accordance with IEEE Std 9 and recent decisions of IEEE.

logic diagrams (positive logic)

'ALS845, 'AS845



'ALS846, 'AS846



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range:
SN54ALS845, SN54AS845, SN54ALS846, SN54AS846 . . . . . −55°C to 125°C
SN74ALS845, SN74AS845, SN74ALS846, SN74AS846 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS845 SN54ALS846			SN74ALS845 SN74ALS846			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
t_w	Pulse duration	$\overline{CLR}$ or $\overline{PRE}$ low							ns
		C high							
t_{su}	Setup time, data before enable C↓								ns
t_h	Hold time, data after enable C↓	'ALS845							ns
		'ALS846							
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS845 SN54ALS846			SN74ALS845 SN74ALS846			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}	'ALS845	V_{CC} = 5.5 V	Outputs high							mA
			Outputs low							
			Outputs disabled		25			25		
	'ALS846		Outputs high							
			Outputs low							
			Outputs disabled		28			28		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

'ALS845 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS845			SN74ALS845			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	D	Q		7			7		ns
t_{PHL}				9			9		
t_{PLH}	C	Q							ns
t_{PHL}									
t_{PLH}	$\overline{PRE}$	Q							ns
t_{PHL}	$\overline{CLR}$	Q							ns
t_{PZH}	$\overline{OC}$	Q							ns
t_{PZL}									
t_{PHZ}	$\overline{OC}$	Q							ns
t_{PLZ}									

'ALS846 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS846			SN74ALS846			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	$\overline{D}$	Q		7			7		ns
t_{PHL}				9			9		
t_{PLH}	C	Q							ns
t_{PHL}									
t_{PLH}	$\overline{PRE}$	Q							ns
t_{PHL}	$\overline{CLR}$	Q							ns
t_{PZH}	$\overline{OC}$	Q							ns
t_{PZL}									
t_{PHZ}	$\overline{OC}$	Q							ns
t_{PLZ}									

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: For load circuit and voltage waveforms, see page 1-12

Additional information on these products can be obtained from the factory as it becomes available.

recommended operating conditions

			SN54AS845 SN54AS846			SN74AS845 SN74AS846			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−24			−24	mA
I_{OL}	Low-level output current.				32			48	mA
t_w	Pulse duration	$\overline{CLR}$ or $\overline{PRE}$ low	5			4			ns
		C high	5			4			
t_{su}	Setup time, data before enable C↑		3.5			2.5			ns
t_h	Hold time, data after enable C↑		3.5			2.5			ns
t_r	Recovery time	$\overline{PRE}$	17			15			ns
		$\overline{CLR}$	16			14			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS845 SN54AS846			SN74AS845 SN74AS846			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −24 mA	2			2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS845	V_{CC} = 5.5 V	Outputs high		35	58		35	58	mA
			Outputs low		52	85		52	85	
			Outputs disabled		52	85		52	85	
	'AS846		Outputs high		36	59		36	59	
			Outputs low		53	87		53	87	
			Outputs disabled		53	87		53	87	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS845 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS845		SN74AS845		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1	8.5	1	6.5	ns
t_{PHL}			1	10	1	9	
t_{PLH}	C	Q	2	13	2	12	ns
t_{PHL}			2	13	2	12	
t_{PLH}	$\overline{PRE}$	Q	2	12	2	10	ns
t_{PHL}	$\overline{CLR}$	Q	2	14	2	13	ns
t_{PZH}	$\overline{OC}$	Q	2	13.5	2	10.5	ns
t_{PZL}			2	14.5	2	11.5	
t_{PHZ}	$\overline{OC}$	Q	1	10	1	8	ns
t_{PLZ}			1	10	1	8	

'AS846 switching characteristicse (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS846		SN74AS846		
			MIN	MAX	MIN	MAX	
t_{PLH}	$\overline{D}$	Q	1	11	1	8.5	ns
t_{PHL}			1	11	1	10	
t_{PLH}	C	Q	2	14	2	12.5	ns
t_{PHL}			2	14	2	13	
t_{PLH}	$\overline{PRE}$	Q	2	12	2	10	ns
t_{PHL}	$\overline{CLR}$	Q	2	14.5	2	13.5	ns
t_{PZH}	$\overline{OC}$	O	2	14.5	2	12	ns
t_{PZL}			2	15	2	13.5	
t_{PHZ}	$\overline{OC}$	O	1	10	1	8	ns
t_{PLZ}			1	10	1	8	

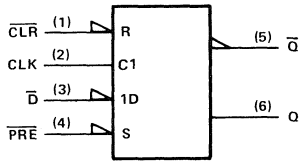
NOTE 1: For load circuit and voltage waveforms, see page 1-12

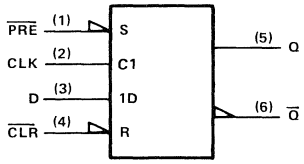
D flip-flop signal conventions

It is normal TI practice to name the outputs and other inputs of a D-type latch and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active-low.

The devices on this data sheet are second-source designs and the pin name convention used by the original manufacturer has been retained. That makes it necessary to designate the inputs and outputs of the inverting circuit $\overline{D}$ and Q. In some applications it may be advantageous to redesignate the inputs and outputs as D and $\overline{Q}$. In that case, outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.

Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators ( ) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 (Q) is still in phase with the data input D, but now both are considered active high.





TYPES SN54AS850, SN54AS851, SN74AS850, SN74AS851
1 OF 16 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

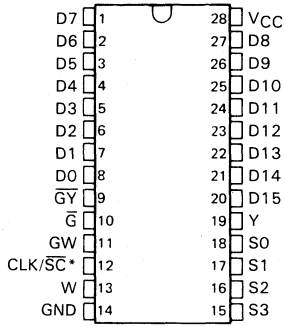
DECEMBER 1983 – REVISED APRIL 1984

- **4-Line to 1-Line Data Selectors/Multiplexers That Can Select 1 of 16 Data Inputs. Typical Applications:**

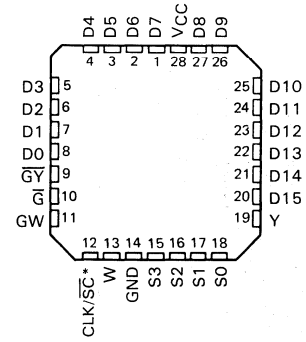
  Boolean Function Generators
  Parallel-to-Serial Converters
  Data Source Selectors

- **Cascadable to n-Bits**
- **3-State Bus Driver Outputs**
- **'AS850 Offers Clocked Selects; 'AS851 Offers Enable-Controlled Selects**
- **Has a Master Output Control ($\overline{G}$) for Cascading and Individual Output Controls ($\overline{GY}$, GW) for Each Output**
- **Package Options Include both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS850, SN54AS851 . . . JD PACKAGE
SN74AS850, SN74AS851 . . . N PACKAGE
(TOP VIEW)



SN54AS850, SN54AS851 . . . FH OR FK PACKAGE
SN74AS850, SN74AS851 . . . FN PACKAGE
(TOP VIEW)



*CLK for 'AS850 or $\overline{SC}$ for 'AS851

description

These four-line to one-line data selectors/multiplexers provide full binary decoding to select one-of-sixteen data sources with complementary Y and W outputs. The 'AS850 has a clock-controlled select register allowing for a symmetrical presentation of the select inputs to the decoder while the 'AS851 has an enable-controlled select register allowing the user to select and hold one particular data line.

A buffered group of output controls ($\overline{G}$, $\overline{GY}$, GW) can be used to place the two outputs in either a normal logic (high or low logic level) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without the need for interface or pull-up components.

The output controls do not affect the internal operations of the data selector/multiplexer. New data can be setup while the outputs are in the high-impedance state.

The SN54AS850 and SN54AS851 are characterized for operation over the full military temperature range from −55°C to 125°C. The SN74AS850 and SN74AS851 are characterized for operation from 0°C to 70°C.

INPUT SELECTION TABLE

SELECT INPUTS				'AS850	'AS851	INPUT
S3	S2	S1	S0	CLK	$\overline{SC}$	SELECTED
L	L	L	L	↑	L	D0
L	L	L	H	↑	L	D1
L	L	H	L	↑	L	D2
L	L	H	H	↑	L	D3
L	H	L	L	↑	L	D4
L	H	L	H	↑	L	D5
L	H	H	L	↑	L	D6
L	H	H	H	↑	L	D7
H	L	L	L	↑	L	D8
H	L	L	H	↑	L	D9
H	L	H	L	↑	L	D10
H	L	H	H	↑	L	D11
H	H	L	L	↑	L	D12
H	H	L	H	↑	L	D13
H	H	H	L	↑	L	D14
H	H	H	H	↑	L	D15
X	X	X	X	H or L	H	Dn

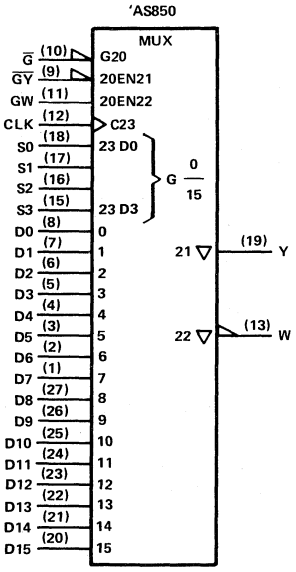
Dn = the input selected before the most-recent low-to-high transition of CLK or SC.

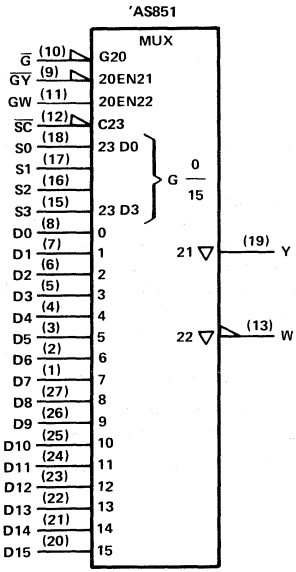
OUTPUT FUNCTION TABLE

$\overline{G}$	$\overline{GY}$	GW	OUTPUTS	
			Y	W
H	X	X	Z	Z
L	H	L	Z	Z
L	L	L	D	Z
L	H	H	Z	$\overline{D}$
L	L	H	D	$\overline{D}$

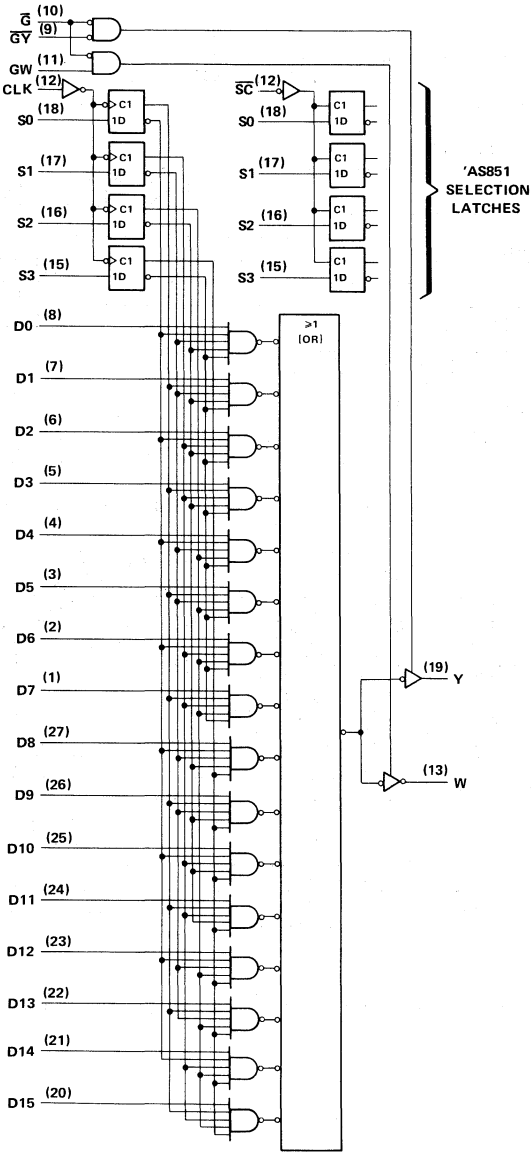
D = level of selected input D0–D15

logic symbols





'AS850 logic diagram (positive logic) (see inset for 'AS851)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS850, SN54AS851 . . . . . −55°C to 125°C
SN74AS850, SN74AS851 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS850			SN74AS850			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				32			48	mA
f_{clock}	Clock frequency					0		60	MHz
t_w	Pulse duration	CLK high				8			ns
		CLK low				8			
t_{su}	Setup time, select inputs before CLK↑					10			ns
t_h	Hold time, select inputs after CLK↑					0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS850			SN74AS850			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	D, $\overline{G}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	All others					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs active		50			50	81	mA
			Outputs disabled		52			52	85	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS850			SN74AS850	
			MIN	TYP†	MAX	MIN	MAX	
f_{max}						60		MHz
t_{PLH}	Any D	Y		5		3	10.5	ns
t_{PHL}				7		3	11	
t_{PLH}	Any D	W		5		3	8	ns
t_{PHL}				3.5		1	6	
t_{PLH}	CLK	Y		10.5		3	14.5	ns
t_{PHL}				12		3	17.5	
t_{PLH}	CLK	W		10		3	15	ns
t_{PHL}				9		3.5	13	
t_{PZH}	$\overline{G}$	Y		5		2	8	ns
t_{PZL}				6		3	11	
t_{PHZ}	$\overline{G}$	Y		5		1	6	ns
t_{PLZ}				5.5		2	8	
t_{PZH}	$\overline{G}$	W		5		2	8	ns
t_{PZL}				11		3	21	
t_{PHZ}	$\overline{G}$	W		5		1	6	ns
t_{PLZ}				5.5		2	8	
t_{PZH}	$\overline{GY}$	Y		5		2	8	ns
t_{PZL}				6		3	11	
t_{PHZ}	$\overline{GY}$	Y		5		1	6	ns
t_{PLZ}				5.5		2	8	
t_{PZH}	GW	W		6		2	10	ns
t_{PZL}				11		3	25	
t_{PHZ}	GW	W		3.5		1	6	ns
t_{PLZ}				7.5		2	11	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12

recommended operating conditions

			SN54AS851			SN74AS851			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				32			48	mA
t_w	Pulse duration	$\overline{SC}$ low				10			ns
t_{su}	Setup time, select inputs before $\overline{SC}$ ↑					4.5			ns
t_h	Hold time, select inputs after $\overline{SC}$ ↑					0			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS851			SN74AS851			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	D, $\overline{G}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	All others					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs active		50			50	81	mA
			Outputs disabled		52			52	85	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS851			SN74AS851	
			MIN	TYP†	MAX	MIN	MAX	
t_{PLH}	Any D	Y		5		3	10.5	ns
t_{PHL}				7		3	11	
t_{PLH}	Any D	W		5		3	8	ns
t_{PHL}				3.5		1	6	
t_{PLH}	S0, S1, S2, S3	Y		12		3	18	ns
t_{PHL}				15		3	19	
t_{PLH}	S0, S1, S2, S3	W		12		3	16	ns
t_{PHL}				10		3	15	
t_{PLH}	$\overline{SC}$	Y		12		3	18	ns
t_{PHL}				15		3	20	
t_{PLH}	$\overline{SC}$	W		12		3	16	ns
t_{PHL}				11		3	15	
t_{PZH}	$\overline{G}$	Y		5.5		2	8	ns
t_{PZL}				7		3	11	
t_{PHZ}	$\overline{G}$	Y		3.5		1	6	ns
t_{PLZ}				5		2	8	
t_{PZH}	$\overline{G}$	W		5.5		2	8	ns
t_{PZL}				11		3	21	
t_{PHZ}	$\overline{G}$	W		3.5		1	6	ns
t_{PLZ}				5		2	8	
t_{PZH}	$\overline{GY}$	Y		5.5		2	8	ns
t_{PZL}				7		3	11	
t_{PHZ}	$\overline{GY}$	Y		3.5		1	6	ns
t_{PZL}				6		2	8	
t_{PZH}	GW	W		6		2	10	ns
t_{PZL}				12		3	25	
t_{PHZ}	GW	W		4		1	6	ns
t_{PLZ}				8		2	11	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12

TYPICAL APPLICATION DATA

The 'AS850 or 'AS851 can be used as a 1-of-16 Boolean function generator. Figure 1 shows the 'AS850 in one example.

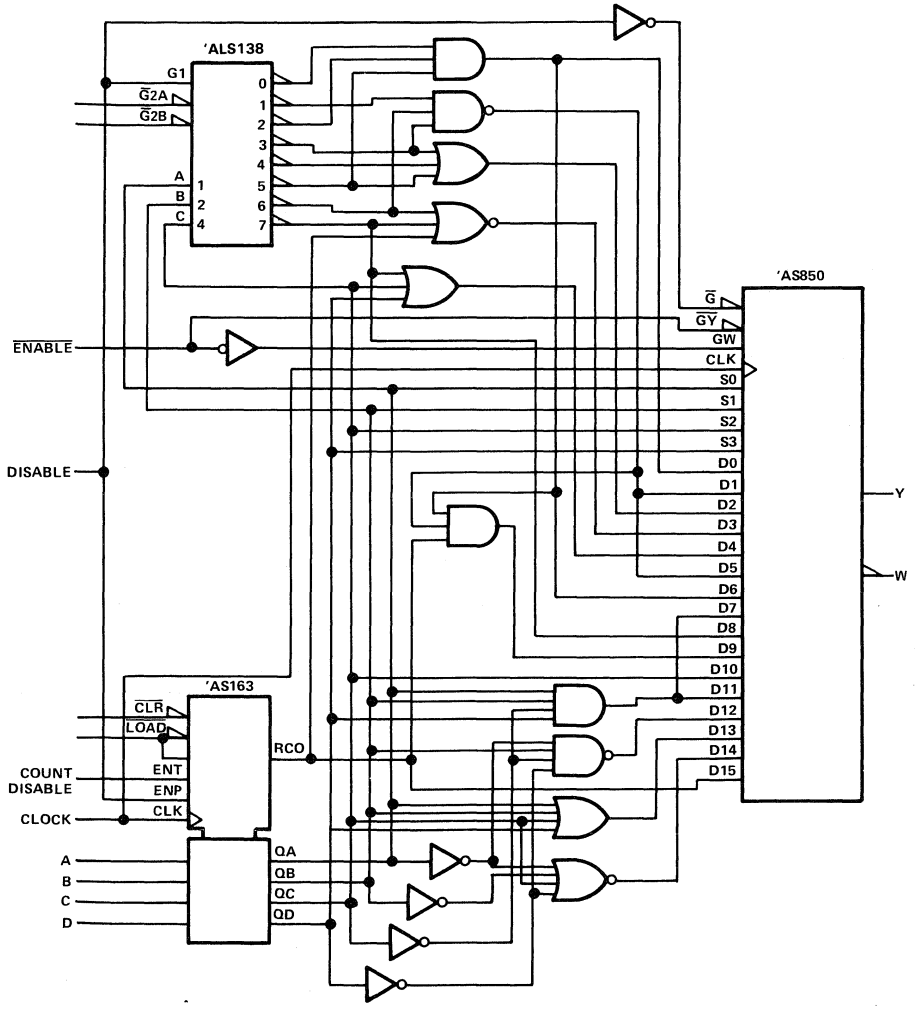


FIGURE 1—1-OF-16 BOOLEAN FUNCTION GENERATOR

TYPICAL APPLICATION DATA

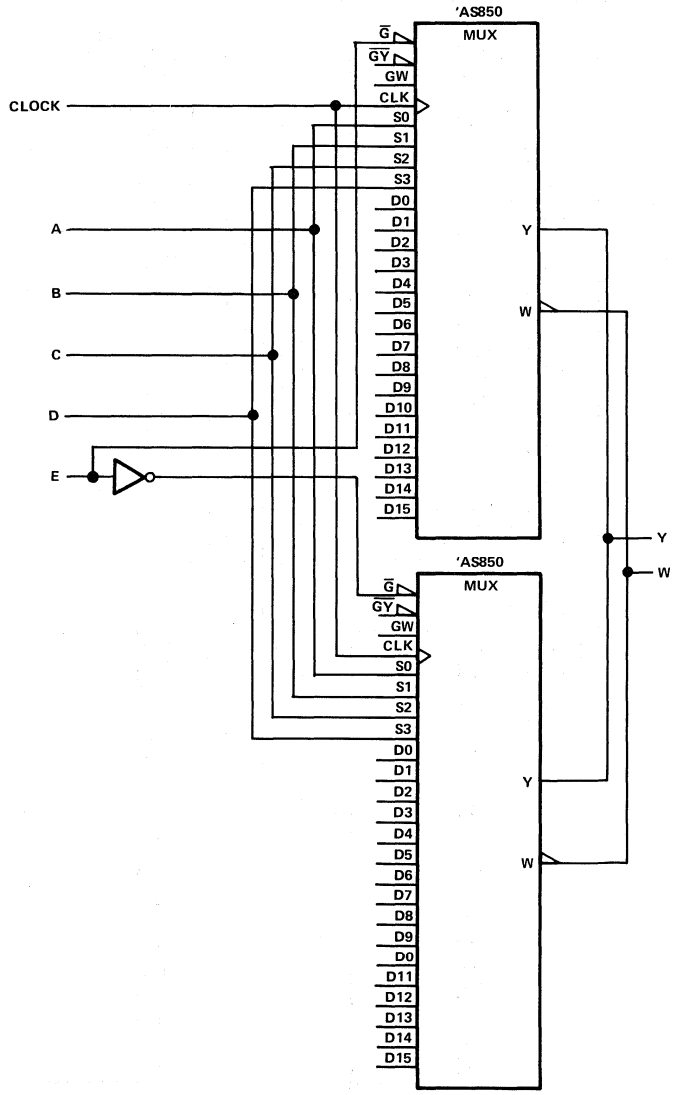


FIGURE 2–1-OF-32 DATA/SELECTOR/MULTIPLEXER

TYPICAL APPLICATION DATA

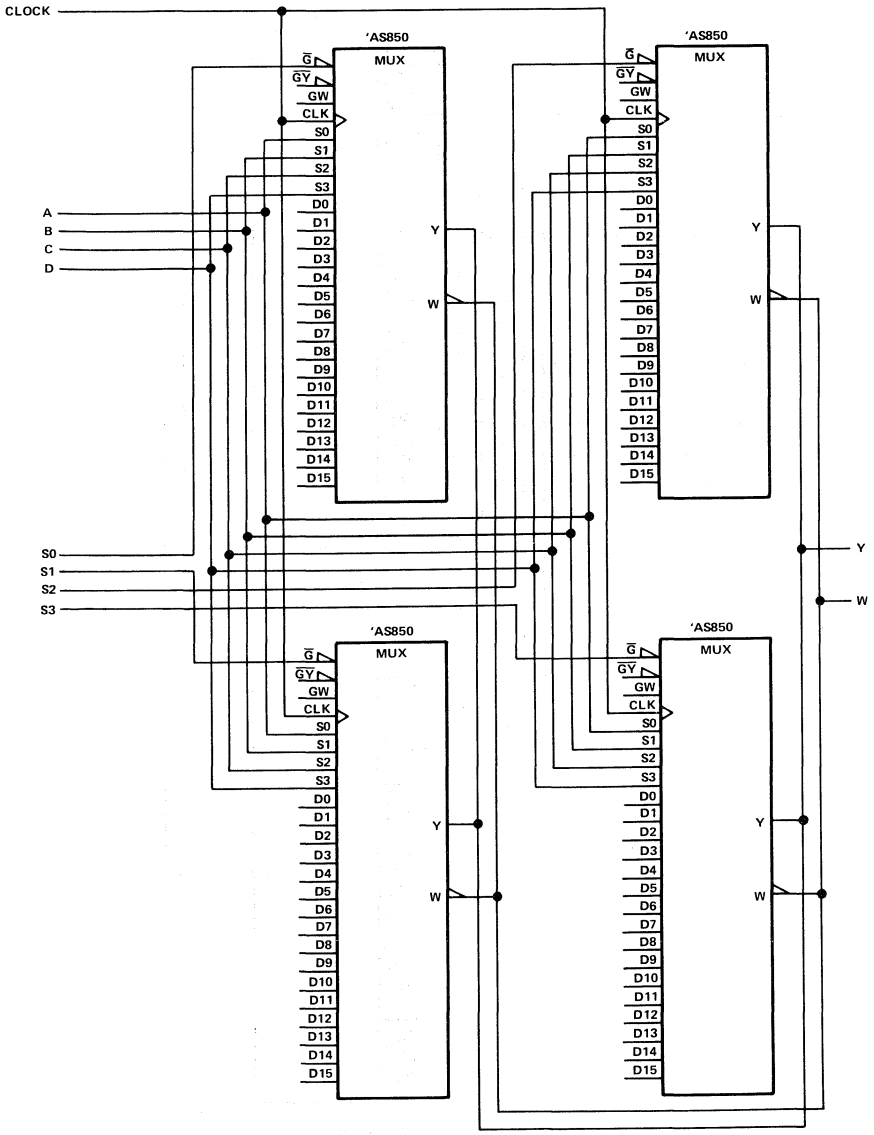
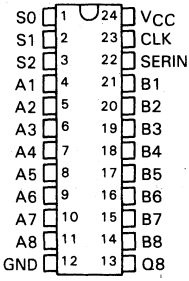


FIGURE 3–1-OF-64 DATA SELECTOR/MULTIPLEXER

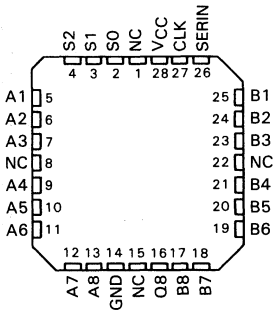
D2810, JUNE 1984 - REVISED MARCH 1985

- Included Among the Package Options are Compact, 24-Pin, 300-mil-Wide DIPs and Small Outline (SO) and 28-Pin Plastic and Ceramic Chip Carriers
- Buffered 3-State Outputs Drive Bus Lines Directly
- Cascadable to n-Bits
- Eight Selectable Transceiver/Port Functions:
  - A to B or B to A
  - Register to A or B
  - Shifted to A from B or Shifted to B from A
  - Off-Line Shifts (A and B Ports Transceiving or in High-Impedance State)
  - Register Clear
- Particularly Suitable for Use in Diagnostics Circuitry
- Serial Register Provides:
  - — Parallel Storage of Either A or B Input Data
  - — Serial Transmission of Data from Either A or B Port
- Dependable Texas Instruments Quality and Reliability

SN54AS852 . . . JT PACKAGE
SN74AS852 . . . NT PACKAGE
SN74AS852 . . . DW PACKAGE
(TOP VIEW)



SN54AS852 . . . FH OR FK PACKAGE
SN74AS852 . . . FN PACKAGE
(TOP VIEW)



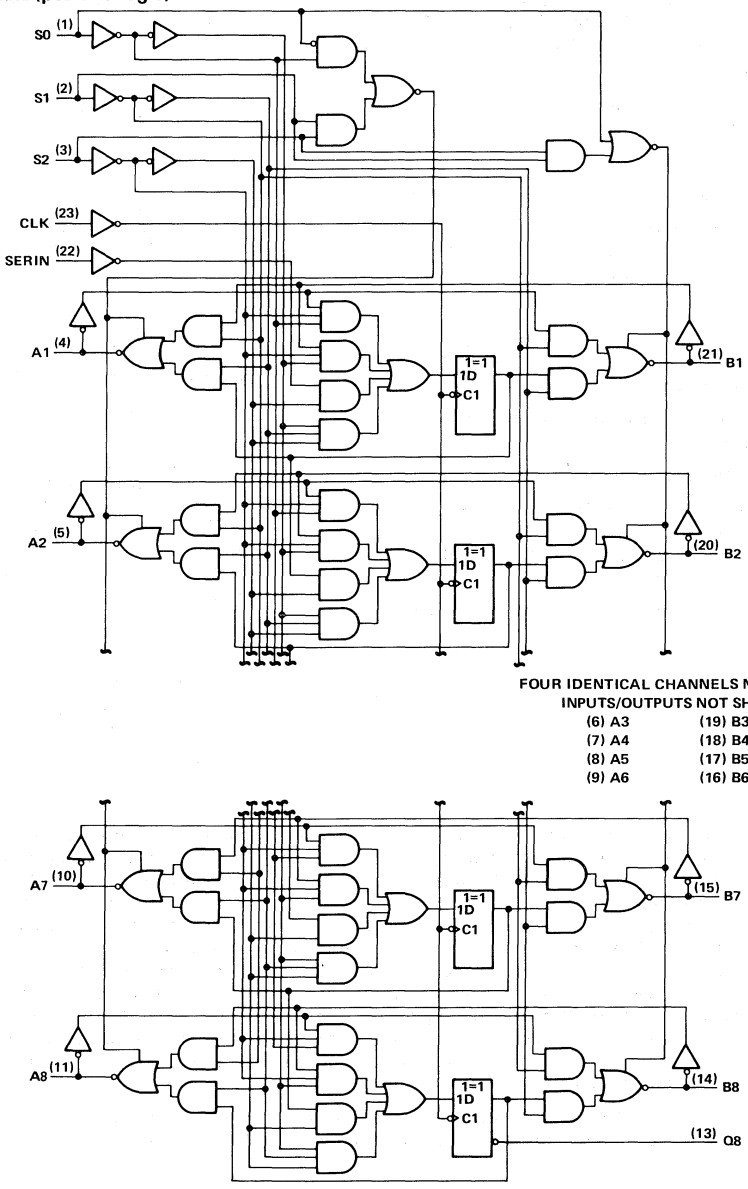
NC – No internal connection

description

The 'AS852 features two 8-bit I/O ports (A1-A8 and B1-B8), and 8-bit parallel-load, serial-in, parallel-out shift register, and control logic. With these features, this device is capable of performing eight selectable transceiver or port functions, depending on the state of the three select lines S0, S1, and S2. These functions include: transferring data from port A to port B or vice versa (i.e., the transceiver function), transferring data from the register to either port, serial shifting data to either port from the opposite port, performing off-line shifts (with A and B ports in high-impedance state), and clearing the register. The 'AS852 can simultaneously transfer data from A to B or B to A and perform an off-line serial shift of data in the register. Synchronous parallel loading of the internal register can be accomplished from either port on the positive transition of the clock while serially shifting data in via the SERIN input. The 'AS852 is ideally suited for applications implementing diagnostic circuitry to enhance system verification and/or fault analysis. All serial data is shifted right. All outputs are buffer-type outputs designed specifically to drive bus lines directly and all are 3-state except for Q8, which is a totem-pole output.

The SN54AS852 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS852 is characterized for operation from 0°C to 70°C.

logic diagram (positive logic)



FOUR IDENTICAL CHANNELS NOT SHOWN

INPUTS/OUTPUTS NOT SHOWN:

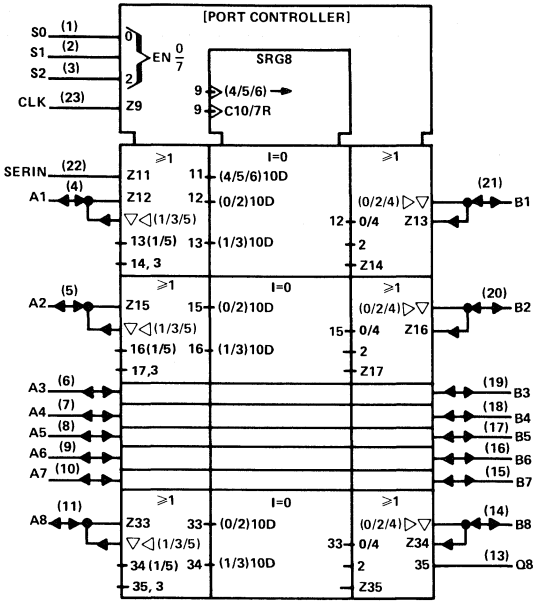
(6) A3	(19) B3
(7) A4	(18) B4
(8) A5	(17) B5
(9) A6	(16) B6

FUNCTION TABLE

MODE S2 S1 S0	CLOCK	SERIN	A1 Q1 B1	A2 Q2 B2	A3 Q3 B3	A4 Q4 B4	A5 Q5 B5	A6 Q6 B6	A7 Q7 B7	A8 Q8 B8	PORT FUNCTION
L L L	H or L	X	Z Q_n A1	Z Q_n A2	Z Q_n A3	Z Q_n A4	Z Q_n A5	Z Q_n A6	Z Q_n A7	Z Q_n A8	A TO B
L L L	↑	X	Z A1 A1	Z A2 A2	A A3 A3	Z A4 A4	Z A5 A5	Z A6 A6	Z A7 A7	Z A8 A8	
L L H	H or L	X	B1 Q_n Z	B2 Q_n Z	B3 Q_n Z	B4 Q_n Z	B5 Q_n Z	B6 Q_n Z	B7 Q_n Z	B8 Q_n Z	B TO A
L L H	↑	X	B1 B1 Z	B2 B2 Z	B3 B3 Z	B4 B4 Z	B5 B5 Z	B6 B6 Z	B7 B7 Z	B8 B8 Z	
L H L	H or L	X	X Q_n Q1	X Q_n Q2	X Q_n Q3	X Q_n Q4	X Q_n Q5	X Q_n Q6	X Q_n Q7	X Q_n Q8	Q_N TO B_N
L H L	↑	X	Z A1 A1	Z A2 A2	Z A3 A3	Z A4 A4	Z A5 A5	Z A6 A6	Z A7 A7	Z A8 A8	
L H H	H or L	X	Q1 Q_n X	Q2 Q_n X	Q3 Q_n X	Q4 Q_n X	Q5 Q_n X	Q6 Q_n X	Q7 Q_n X	Q8 Q_n X	Q_N TO A_N
L H H	↑	X	B1 B1 Z	B2 B2 Z	B3 B3 Z	B4 B4 Z	B5 B5 Z	B6 B6 Z	B7 B7 Z	B8 B8 Z	
H L L	H or L	X	Z Q_n A1	Z Q_n A2	Z Q_n A3	Z Q_n A4	Z Q_n A5	Z Q_n A6	Z Q_n A7	Z Q_n A8	SHIFT
H L L	↑	H	Z H A1	Z Q1 A2	Z Q2 A3	Z Q3 A4	Z Q4 A5	Z Q5 A6	Z Q6 A7	Z Q7 A8	AND
H L L	↑	L	Z L A1	Z Q1 A2	Z Q2 A3	Z Q3 A4	Z Q4 A5	Z Q5 A6	Z Q6 A7	Z Q7 A8	A TO B
H L H	H or L	X	B1 Q_n Z	B2 Q_n Z	B3 Q_n Z	B4 Q_n Z	B5 Q_n Z	B6 Q_n Z	B7 Q_n Z	B8 Q_n Z	SHIFT
H L H	↑	H	B1 H Z	B2 Q1 Z	B3 Q2 Z	B4 Q3 Z	B5 Q4 Z	B6 Q5 Z	B7 Q6 Z	B8 Q7 Z	AND
H L H	↑	L	B1 L Z	B2 Q1 Z	B3 Q2 Z	B4 Q3 Z	B5 Q4 Z	B6 Q5 Z	B7 Q6 Z	B8 Q7 Z	B TO A
H H L	H or L	X	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	SHIFT
H H H	↑	H	Z H Z	Z Q1 Z	Z Q2 Z	Z Q3 Z	Z Q4 Z	Z Q5 Z	Z Q6 Z	Z Q7 Z	
H H H	↑	L	Z L Z	Z Q1 Z	Z Q2 Z	Z Q3 Z	Z Q4 Z	Z Q5 Z	Z Q6 Z	Z Q7 Z	
H H H	H or L	X	Z Q_n Z	Z Q_n	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	CLEAR
H H H	↑	X	Z L Z	Z L Z	Z L Z	Z L Z	Z L Z	Z L Z	Z L Z	Z L Z	

n = level of Q_n(n = 1,2, . . . 8) established on most recent ↑ transition of CLK. Q1 through Q8 are the shift register outputs; only Q is available externally. The double inversions that take place as data travels from port to port are ignored in this table.

logic symbol



Pin numbers shown are JT and NT packages.

absolute maximum ratings over free-air temperature range

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS852 . . . . . −55°C to 125°C
SN74AS852 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS852			SN74AS852			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	A1-A8, B1-B8			−12			−15	mA
		Q8			−2			−2	
I_{OL}	Low-level output current	A1-A8, B1-B8			32			48	mA
		Q8			20			20	
f_{clock}	Clock frequency		0		45	0		50	MHz
t_w	Duration of clock pulse		11			10			ns
t_{su}	Setup time before CLK↑	A1-A8, B1-B8, SERIN	5.5			5.5			ns
		S0, S1, S2	5.5			5.5			
t_h	Hold-time, data after CLK↑	A1-A8, B1-B8, SERIN	0			0			ns
		S0, S1, S2	0			0			
T_A	Operating free-air temperture		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS852			SN74AS852			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	A1-A8, B1-B8	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					V
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			
V_{OL}	All outputs except Q8	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.3	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
	Q8	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	
I_I	S0, S1, S2	V_{CC} = 5.5 V,	V_I = 7 V			0.3			0.3	mA
	CLK and SERIN					0.1			0.1	
	A1-A8, B1-B8	V_{CC} = 5.5 V,	V_I = 5.5 V			0.2			0.2	
I_{IH}	S0, S1, S2	V_{CC} = 5.5 V,	V_I = 2.7 V			60			60	μA
	CLK and SERIN					20			20	
	A1-A8, B1-B8‡					70			70	
I_{IL}	S0, S1, S2	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	CLK and SERIN					−0.5			−0.5	
	A1-A8, B1-B8‡					−0.5			−0.5	
I_O§	Except Q8	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
	Q8			−20		−112	−20		−112	
I_{CC}		V_{CC} = 5.5 V			136	220		136	220	mA

†All tyical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the output currents I_{OZH} and I_{OZL}, respectively.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

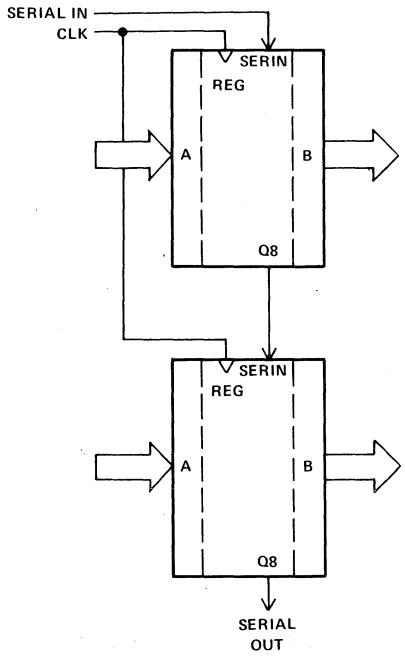
switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	R_L = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS852		SN74AS852		
			MIN	MAX	MIN	MAX	
f_{max}			45		50		MHz
t_{PLH}	Any A port	Any B port	2	9	2	7.5	ns
t_{PHL}			3	12.5	3	11	
t_{PLH}	Any B port	Any A port	2	9	2	7.5	ns
t_{PHL}			3	12.5	3	11	
t_{PLH}	S0, S1, S2	Any A or B port	3	11.5	3	10	ns
t_{PHL}			3	12	3	10.5	
t_{PLH}	CLK	Any A or B port	2	11	2	9	ns
t_{PHL}			3	14	3	12.5	
t_{PLH}	CLK	Q8	2	10.5	2	8	ns
t_{PHL}			3	11.5	3	10	
t_{PHZ}	S0, S1, S2	Any A or B port	2	9	2	7	ns
t_{PLZ}			3	13	3	10.5	
t_{PZH}			2	9	2	7	ns
t_{PZL}			3	13	3	10.5	

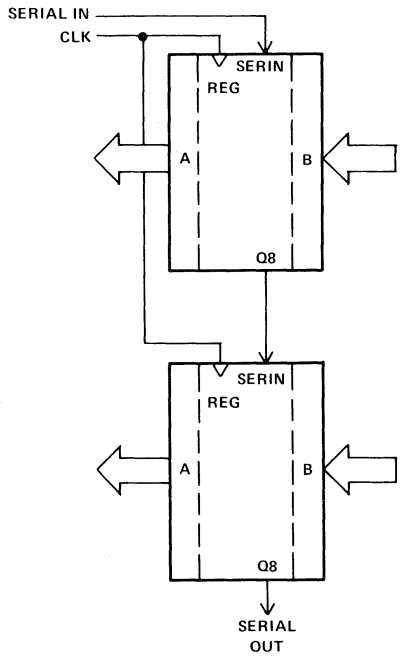
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

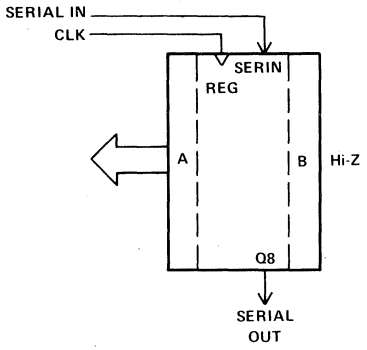
BUS A TO BUS B OR
SERIAL TRANSMISSION



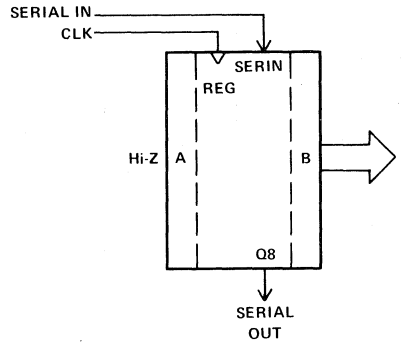
BUS B TO BUS A OR
SERIAL TRANSMISSION



SERIAL IN TO A PORT



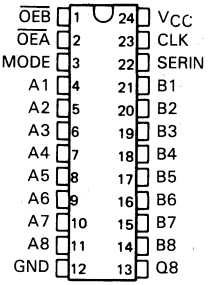
SERIAL IN TO B PORT



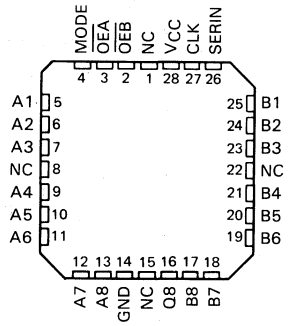
D2814, DECEMBER 1983 REVISED MARCH 1985

- Included Among the Package Options are Compact, 24-Pin, 300-mil-Wide DIPs and Small Outline (SO) and 28-Pin Plastic and Ceramic Chip Carriers
- Buffered 3-State Outputs Drive Bus Lines Directly
- Cascadable to n-Bits
- Eight Selectable Transceiver/Port Functions:
  - B to A
  - Register to A and/or B
  - Off-Line Shifts (A and B Ports in High-Impedance State)
  - Shifted to A and/or B
- Particularly Suitable for Use in Diagnostics Analysis Circuitry
- Serial Register Provides:
  - Parallel Storage of Either A or B Input Data
  - Serial Transmission of Data from Either A or B Port
  - Readback Mode B to A
- Dependable Texas Instruments Quality and Reliability

SN54AS856 . . . JT PACKAGE
SN74AS856 . . . NT PACKAGE
SN74AS856 . . . DW PACKAGE
(TOP VIEW)



SN54AS856 . . . FH OR FK PACKAGE
SN74AS856 . . . FN PACKAGE
(TOP VIEW)



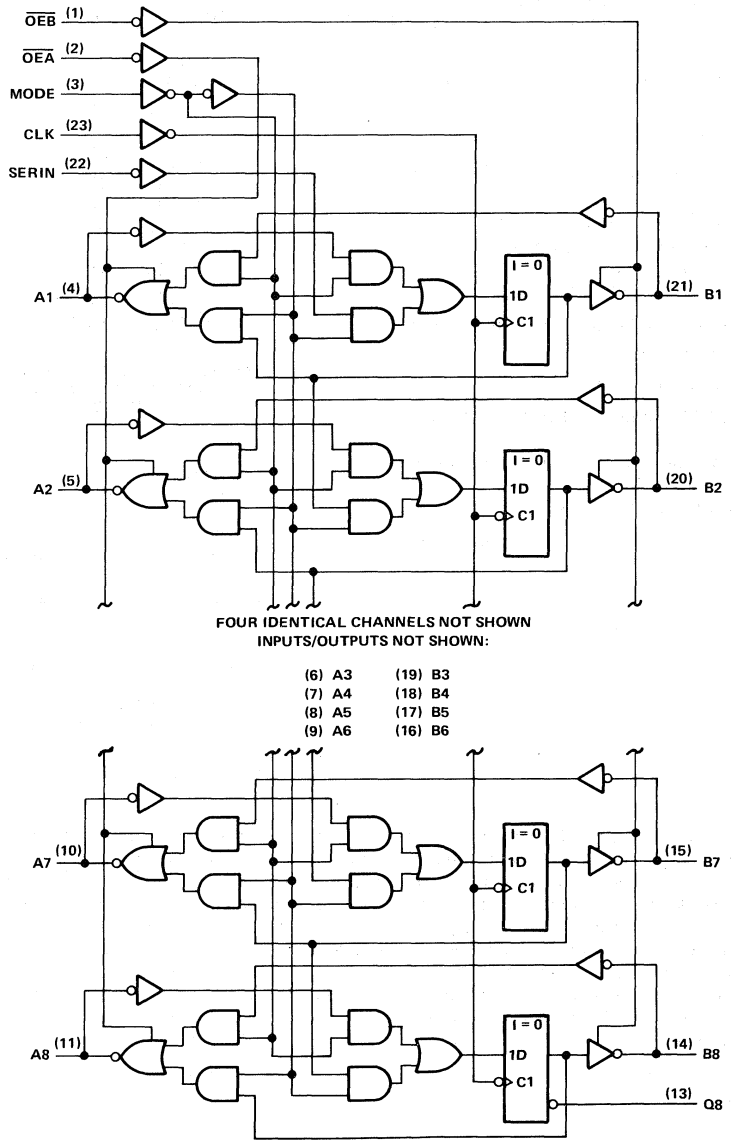
NC – No internal connection

description

The 'AS856 features two 8-bit I/O ports (A1-A8 and B1-B8), an 8-bit parallel-load, serial-in, parallel-out shift register, and control logic. With these features, this device is capable of performing eight selectable transceiver or port functions, depending on the state of the three control lines $\overline{OEA}$, $\overline{OEB}$, and MODE. These functions include: transferring data from port A to port B or vice versa (i.e., the transceiver function), serial shifting data to either or both ports, and performing off-line shifts (with A and B ports active as transceivers in a high-impedance state). Synchronous parallel loading of the internal register can be accomplished from either port on the positive transition of the clock while serially shifting data in via the SERIN input. The 'AS856 is ideally suited for applications needing signature-analysis circuitry to enhance system verification and/or fault analysis. All serial data is shifted right. All outputs are buffer-type outputs designed specifically to drive bus lines directly and all are 3-state except for Q8, which is a totem-pole output.

The SN54AS856 is characterized for operation over the full military temperaure range of −55°C to 125°C. The SN74AS856 is characterized for operation from 0°C to 70°C.

logic diagram (positive logic)



FOUR IDENTICAL CHANNELS NOT SHOWN
INPUTS/OUTPUTS NOT SHOWN:

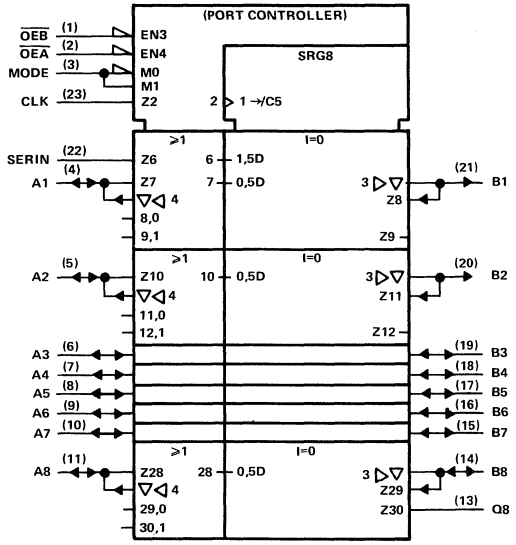
(6) A3	(19) B3
(7) A4	(18) B4
(8) A5	(17) B5
(9) A6	(16) B6

FUNCTION TABLE

MODE	$\overline{OEA}$	$\overline{OEB}$	CLOCK	SERIN	A1 Q1 B1	A2 Q2 B2	A3 Q3 B3	A4 Q4 B4	A5 Q5 B5	A6 Q6 B6	A7 Q7 B7	A8 Q8 B8	FUNCTION
L	L	L	H or L	X	Q1 Q1 Q1	Q2 Q2 Q2	Q3 Q3 Q3	Q4 Q4 Q4	Q5 Q5 Q5	Q6 Q6 Q6	Q7 Q7 Q7	Q8 Q8 Q8	FEEDBACK
L	L	L	↑	X	Q1 Q1 Q1	Q2 Q2 Q2	Q3 Q3 Q3	Q4 Q4 Q4	Q5 Q5 Q5	Q6 Q6 Q6	Q7 Q7 Q7	Q8 Q8 Q8	
L	L	H	H or L	X	B1 Q1 Z	B2 Q2 Z	B3 Q3 Z	B4 Q4 Z	B5 Q5 Z	B6 Q6 Z	B7 Q7 Z	B8 Q8 Z	B to A
L	L	H	↑	X	B1 B1 Z	B2 B2 Z	B3 B3 Z	B4 B4 Z	B5 B5 Z	B6 B6 Z	B7 B7 Z	B8 B8 Z	A to Q
L	H	L	H or L	X	Z Q1 Q1	Z Q2 Q2	Z Q3 Q3	Z Q4 Q4	Z Q5 Q5	Z Q6 Q6	Z Q7 Q7	Z Q8 Q8	A to Q
L	H	L	↑	X	Z A1 A1	Z A2 A2	Z A3 A3	Z A4 A4	Z A5 A5	Z A6 A6	Z A7 A7	Z A8 A8	Q to B
L	H	H	H or L	X	Z Q1 Z	Z Q2 Z	Z Q3 Z	Z Q4 Z	Z Q5 Z	Z Q6 Z	Z Q7 Z	Z Q8 Z	A to Q
L	H	H	↑	X	Z A1 Z	Z A2 Z	Z A3 Z	Z A4 Z	Z A5 Z	Z A6 Z	Z A7 Z	Z A8 Z	
H	L	L	H or L	X	Q1 Q_n Q1	Q2 Q_n Q2	Q3 Q_n Q3	Q4 Q_n Q4	Q5 Q_n Q5	Q6 Q_n Q6	Q7 Q_n Q7	Q8 Q_n Q8	SHIFT
H	L	L	↑	H	H H H	Q1 Q1 Q1	Q2 Q2 Q2	Q3 Q3 Q3	Q4 Q4 Q4	Q5 Q5 Q5	Q6 Q6 Q6	Q7 Q7 Q7	TO
H	L	L	↑	L	L L L	Q1 Q1 Q1	Q2 Q2 Q2	Q3 Q3 Q3	Q4 Q4 Q4	Q5 Q5 Q5	Q6 Q6 Q6	Q7 Q7 Q7	A and B
H	L	H	H or L	X	Q1 Q_n Z	Q2 Q_n Z	Q3 Q_n Z	Q4 Q_n Z	Q5 Q_n Z	Q6 Q_n Z	Q7 Q_n Z	Q8 Q_n Z	SHIFT
H	L	H	↑	H	H H Z	Q1 Q1 Z	Q2 Q2 Z	Q3 Q3 Z	Q4 Q4 Z	Q5 Q5 Z	Q6 Q6 Z	Q7 Q7 Z	TO
H	L	H	↑	L	L L Z	Q1 Q1 Z	Q2 Q2 Z	Q3 Q3 Z	Q4 Q4 Z	Q5 Q5 Z	Q6 Q6 Z	Q7 Q7 Z	A
H	H	L	H or L	X	Z Q_n Q1	Z Q_n Q2	Z Q_n Q3	Z Q_n Q4	Z Q_n Q5	Z Q_n Q6	Z Q_n Q7	Z Q_n Q8	SHIFT
H	H	L	↑	H	Z H H	Z Q1 Q1	Z Q2 Q2	Z Q3 Q3	Z Q4 Q4	Z Q5 Q5	Z Q6 Q6	Z Q7 Q7	TO
H	H	L	↑	L	Z L L	Z Q1 Q1	Z Q2 Q2	Z Q3 Q3	Z Q4 Q4	Z Q5 Q5	Z Q6 Q6	Z Q7 Q7	B
H	H	H	H or L	X	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	SHIFT
H	H	H	↑	H	Z H Z	Z Q1 Z	Z Q2 Z	Z Q3 Z	Z Q4 Z	Z Q5 Z	Z Q6 Z	Z Q7 Z	
H	H	H	↑	L	Z L H	Z Q1 Z	Z Q2 Z	Z Q3 Z	Z Q4 Z	Z Q5 Z	Z Q6 Z	Z Q7 Z	

n = level of Q_n(n = 1, 2 . . . 8) established on most recent ↑ transition of CLK. Q1 through Q8 are the shift register outputs; only Q8 is available externally. The double inversions that take place as data travels from port to port are ignored in this table.

logic symbol



Pin numbers shown are for JT and NT packages.

absolute maximum ratings over free-air temperature range

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS856 . . . . . −55°C to 125°C
SN74AS856 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS856			SN74AS856			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	A1-A8, B1-B8			−12			−15	mA
		Q8			−2			−2	
I_{OL}	Low-level output current	A1-A8, B1-B8			32			48	mA
		Q8			20			20	
f_{clock}	Clock frequency		0		45	0		50	MHz
t_w	Duration of clock pulse		11			10			ns
t_{su}	Setup time before CLK↑	A1-A8, B1-B8 SERIN	5.5			5.5			ns
		$\overline{OEB}$, $\overline{OEA}$, MODE	5.5			5.5			
t_h	Hold-time, data after CLK↑	A1-A8, B1-B8 SERIN	0			0			ns
		$\overline{OEB}$, $\overline{OEA}$, MODE	0			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS856			SN74AS856			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	A1-A8	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2	3.2					V
	B1-B8	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2	3.3		
	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC} −2			V_{CC} −2			
V_{OL}	All outputs except Q8	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
	Q8	V_{CC} = 4.5 V,	I_{OL} = 20 mA			0.5			0.5	
I_I	$\overline{OEB}$, $\overline{OEA}$, MODE	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	CLK and SERIN					0.1			0.1	
	A1-A8, B1-B8	V_{CC} = 5.5 V,	V_I = 5.5 V			0.2			0.2	
I_{IH}	$\overline{OEB}$, $\overline{OEA}$, MODE	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	CLK and SERIN					20			20	
	A1-A8, B1-B8‡					70			70	
I_{IL}	$\overline{OEB}$, $\overline{OEA}$, MODE	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	CLK and SERIN					−0.5			−0.5	
	A1-A8, B1-B8‡					−0.5			−0.5	
I_O§	Except Q8	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
	Q8			−20		−112	−20		−112	
I_{CC}		V_{CC} = 5.5 V			118	200		118	200	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the output currents I_{OZH} and I_{OZL}, respectively.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS856		SN74AS856		
			MIN	MAX	MIN	MAX	
f_{max}			45		50		MHz
t_{PLH}	Any B port	Any A port	2	8	2	7	ns
t_{PHL}			2	10.5	2	9.5	
t_{PLH}	↑MODE¶	Any A or B port	2	8.5	2	7.5	ns
t_{PHL}			5	20	5	19	
t_{PLH}	↓MODE	Any A or B port	2	8.5	2	7.5	ns
t_{PHL}			2	9.5	2	8	
t_{PLH}	CLK	Any A or B port	3	12	3	9	ns
t_{PHL}			3	12	3	11	
t_{PLH}	CLK	Q8	2	9	2	7.5	ns
t_{PHL}			2	10	2	9	
t_{PHZ}	$\overline{OEA}$ or $\overline{OEB}$	Any A or B port	2	9	2	7	ns
t_{PLZ}			2	12	2	9.5	
t_{PZH}			2	8	2	7	ns
t_{PZL}			2	11	2	10	

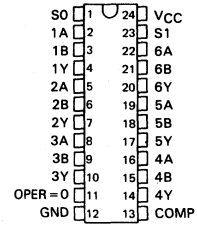
¶The positive transition of the MODE control will cause low-level data at the A output Bus or stored in Q to be invalid for 12 ns.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPES SN54ALS857, SN54AS857, SN74ALS857, SN74AS857
HEX 2-TO-1 UNIVERSAL MULTIPLEXERS

D2661, DECEMBER 1982—REVISED DECEMBER 1983

- **Selects True or Complementary Data**
- **Performs AND/NAND (masking) of A or B Operand**
- **Cascadable to Expand Number of Operands**
- **Detects Zeros on A or B Operands**
- **3-State Outputs Interface Directly with System Bus**
- **Included Among the Package Options Are 24-Pin, 300-Mil-Wide DIPs and Small Outline (SO) and 28-Pin Plastic and Ceramic Chip Carriers**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS857, SN54AS857 . . . JT PACKAGE
SN74ALS857, SN74AS857 . . . NT PACKAGE
SN74ALS857, SN74AS857 . . . DW PACKAGE
(TOP VIEW)



SN54ALS857, SN54AS857 . . . FH OR FK PACKAGE
SN74ALS857, SN74AS857 . . . FN PACKAGE
(TOP VIEW)

For chip carrier information contact factory

description

The 'ALS857 and 'AS857 are hextuple 2-line to 1-line multiplexers with three-state outputs. The devices can provide either true (COMP low) or inverted (COMP high) data at the Y outputs. In addition, the 'ALS857 and 'AS857 perform the logical AND function (A·B) and the clear function as well. The four modes of operation are:

Select A data inputs,
Select B data inputs,
AND A inputs with B inputs,
Clear

In either of the first two modes, OPER = 0 is high if all the selected A or B inputs are low.

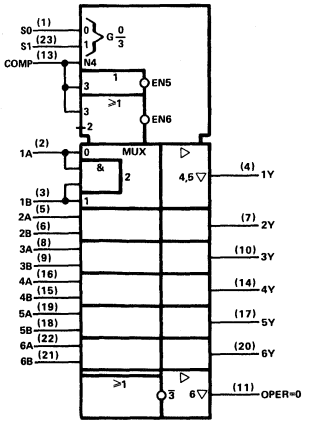
The six Y outputs and the OPER = 0 output are all three-state and rated at 12 mA and 24 mA I_{OL} for the SN54ALS857 and SN74ALS857, respectively, and at 32 mA and 48 mA I_{OL} for the SN54AS857 and SN74AS857, respectively. All outputs can be placed into the high-impedance state by applying a high level to the COMP, S0, and S1 inputs simultaneously. The complete function table is shown below.

The SN54ALS857 and SN54AS857 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS857 and SN74AS857 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE

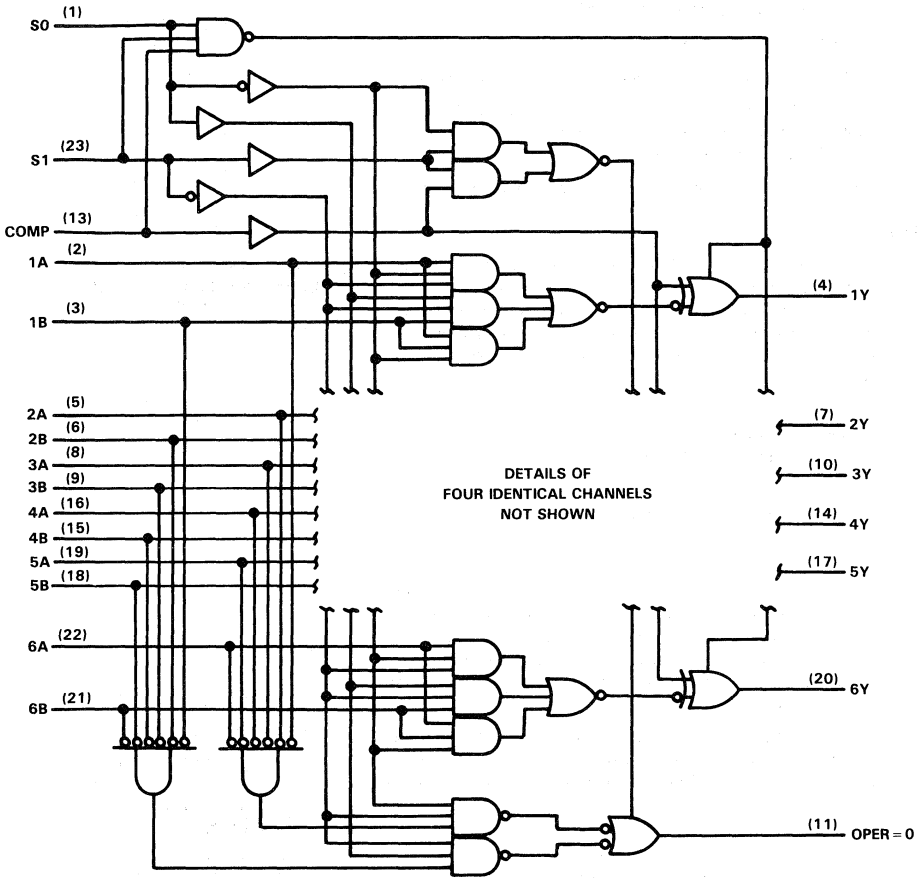
COMP	S1	S0	Y OUTPUTS	OPER = ZERO
L	L	L	A	H = all A inputs L
L	L	H	B	H = all B inputs L
L	H	L	A·B	Z
L	H	H	L	L
H	L	L	$\overline{A}$	H = all A inputs L
H	L	H	$\overline{B}$	H = all B inputs L
H	H	L	$\overline{A \cdot B}$	Z
H	H	H	Z	Z

logic symbol



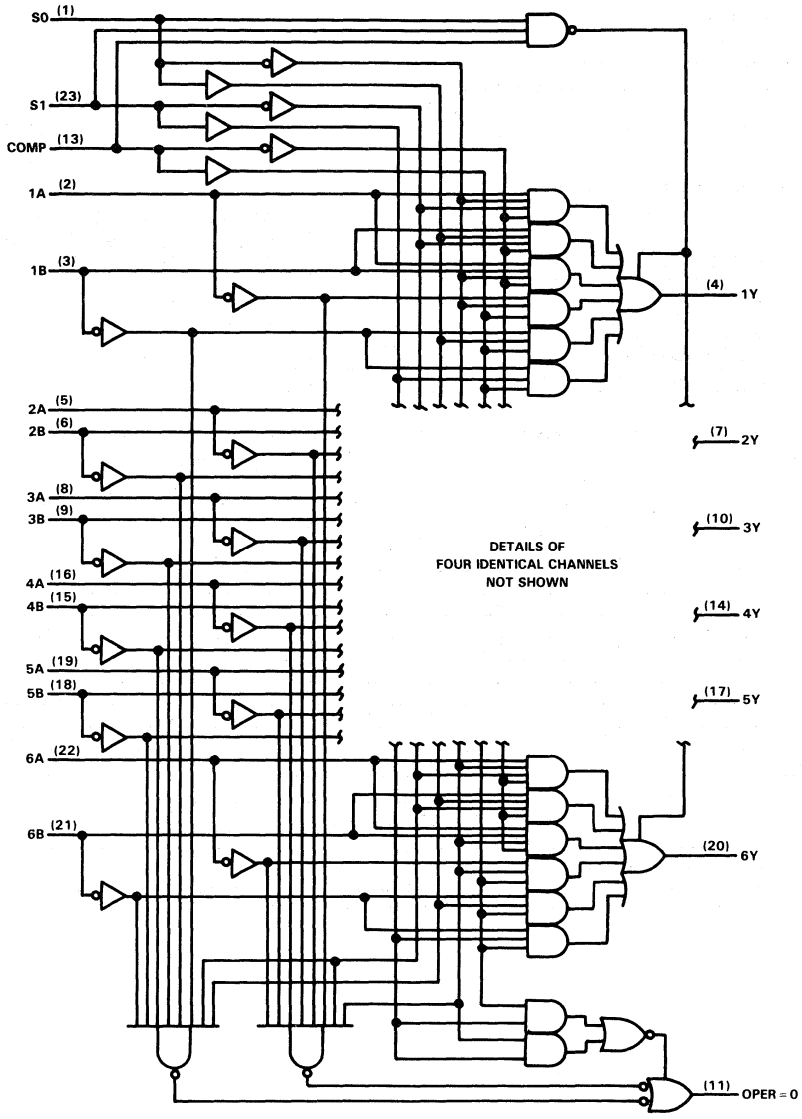
Pin numbers shown are for JT and NT packages.

'ALS857 logic diagram (positive logic)



Pin numbers shown are for JT and NT packages.

'AS857 logic diagram (positive logic)



Pin numbers shown are for JT and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS857 . . . . . −55°C to 125°C
SN74ALS857 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS857			SN74ALS857			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS857			SN74ALS857			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}	V_{CC} = 5.5 V, See Note 1	Outputs high		11	24		11	24	mA
		Outputs low		16	33		16	33	
		Outputs disabled		18	36		18	36	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with all possible inputs grounded while achieving the stated output conditions.

switching characterisitcs (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS857		SN74ALS857		
			MIN	MAX	MIN	MAX	
t_{pd}	A or B (COMP high)	Y (Inverting)	4	18	4	14	ns
t_{pd}	A or B (COMP low)	Y (Noninverting)	4	18	4	14	ns
t_{pd}	S0 or S1	Y	7	37	7	33	ns
t_{pd}	COMP	Y	6	22	6	18	
t_{pd}	A or B	OPER=0	5	45	5	37	
t_{pd}	S0 or S1	OPER=0	5	30	5	23	
t_{en}	S0 or S1	Y	7	38	7	35	ns
t_{dis}			2	29	2	23	
t_{en}	COMP	Y	8	27	8	24	ns
t_{dis}			6	27	6	21	
t_{en}	S0	OPER=0	6	24	6	20	ns
t_{dis}			11	34	11	27	
t_{en}	S1	OPER=0	6	28	6	25	ns
t_{dis}			3	23	3	19	
t_{en}	COMP	OPER=0	9	30	9	25	ns
t_{dis}			6	24	6	20	

t_{pd} = t_{PLH} or t_{PHL}
t_{en} = t_{PZH} or t_{PZL}
t_{dis} = t_{PHZ} or t_{PLZ}
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS857 . . . . . −55°C to 125°C
SN74AS857 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS857			SN74AS857			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	Y Outputs			−12			−15	mA
		OPER = 0			−2			−2	
I_{OL}	Low-level output current	Y Outputs			32			48	mA
		OPER = 0			20			20	
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS857			SN74AS857			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	Y Outputs	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					V
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
	All Outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			
V_{OL}	Y Outputs	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.35	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
	OPER = 0	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	
I_{OZH}		V_{CC} = 5.5 V,	I_{OL} = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−2			−2	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V, See Note 1	Outputs high		97	140		97	140	mA
			Outputs low		127	175		127	175	
			Outputs disabled		92	135		92	135	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with all possible inputs grounded while achieving the stated output conditions.

switching characteristics (see Note 1)

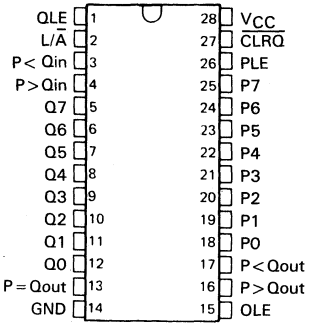
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V, to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS857		SN74AS857		
			MIN	MAX	MIN	MAX	
t_{pd}	A or B (COMP high)	Y (Inverting)	2	15	2	12	ns
t_{pd}	A or B (COMP low)	Y (Noninverting)	2	12	2	10	ns
t_{pd}	S0 or S1	Y	2	15	2	13	ns
t_{pd}	COMP	Y	2	15	2	13	
t_{pd}	A or B	OPER = 0	2	16	2	14	
t_{pd}	S0 to S1	OPER = 0	2	20	2	18	
t_{en}	S0 to S1	Y	2	14	2	12	ns
t_{dis}			2	13	2	11	
t_{en}	COMP	Y	2	14	2	12	ns
t_{dis}			2	10	2	9	
t_{en}	S0	OPER = 0	2	14	2	12	ns
t_{dis}			2	10	2	9	
t_{en}	S1	OPER = 0	2	14	2	12	ns
t_{dis}			2	10	2	9	
t_{en}	COMP	OPER = 0	2	10	2	13	ns
t_{dis}			2	10	2	9	

$t_{pd} = t_{PLH}$ or t_{PHL}
$t_{en} = t_{PZH}$ or t_{PAL}
$t_{dis} = t_{PHZ}$ or t_{PLZ}
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

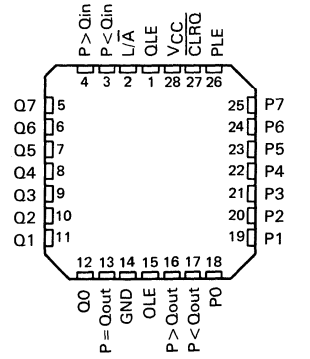
D2661, DECEMBER 1982—REVISED DECEMBER 1983

- **Included among the Package Options Are 28-Pin DIPs and Plastic and Ceramic Chip Carriers**
- **Input and Output Latches with Active-High Enables**
- **Fast Compare to Zero**
- **Arithmetic and Logical Comparison**
- **Open-Collector P = Q Output**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS866 . . . JD PACKAGE
SN74AS866 . . . N PACKAGE
(TOP VIEW)



SN54AS866 . . . FH OR FK PACKAGE
SN74AS866 . . . FN PACKAGE
(TOP VIEW)



description

These Advanced Schottky devices are capable of performing high-speed arithmetic or logical comparisons on two 8-bit binary or two's complement words. Three fully decoded decisions about words P and Q are externally available at the outputs. These devices are fully expandable to any word length by connecting the totem pole P > Q and P < Q outputs of each stage to the P > Q and P < Q inputs of the next higher-order stage. The cascading paths are implemented with only a two-gate-level delay to reduce overall comparison times for long words. The open-collector P = Q outputs may be wire-ANDed together.

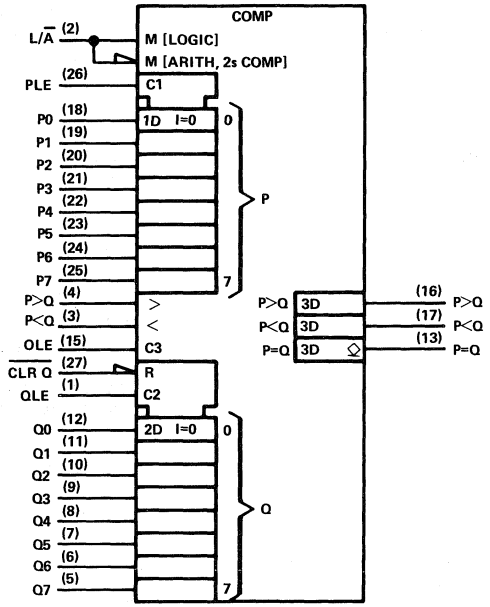
Both input words P and Q plus all three outputs (P > Q, P < Q, and P = Q) are equipped with latches to provide the designer with temporary data storage for avoiding race conditions. The enable circuitry is implemented with minimal delay times to enhance performance when the devices are cascaded for longer word lengths. Each latch is transparent when the appropriate latch enable, PLE, QLE, or OLE is high.

The enable inputs PLE and QLE and data inputs P and Q utilize p-n-p input transistors to reduce the low-level input current requirement to typically −0.25 mA, which minimizes loading effects.

The Q register may be cleared to zero for a fast comparison of the P word to zero.

The SN54AS866 is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74AS866 is characterized for operation from 0 °C to 70 °C.

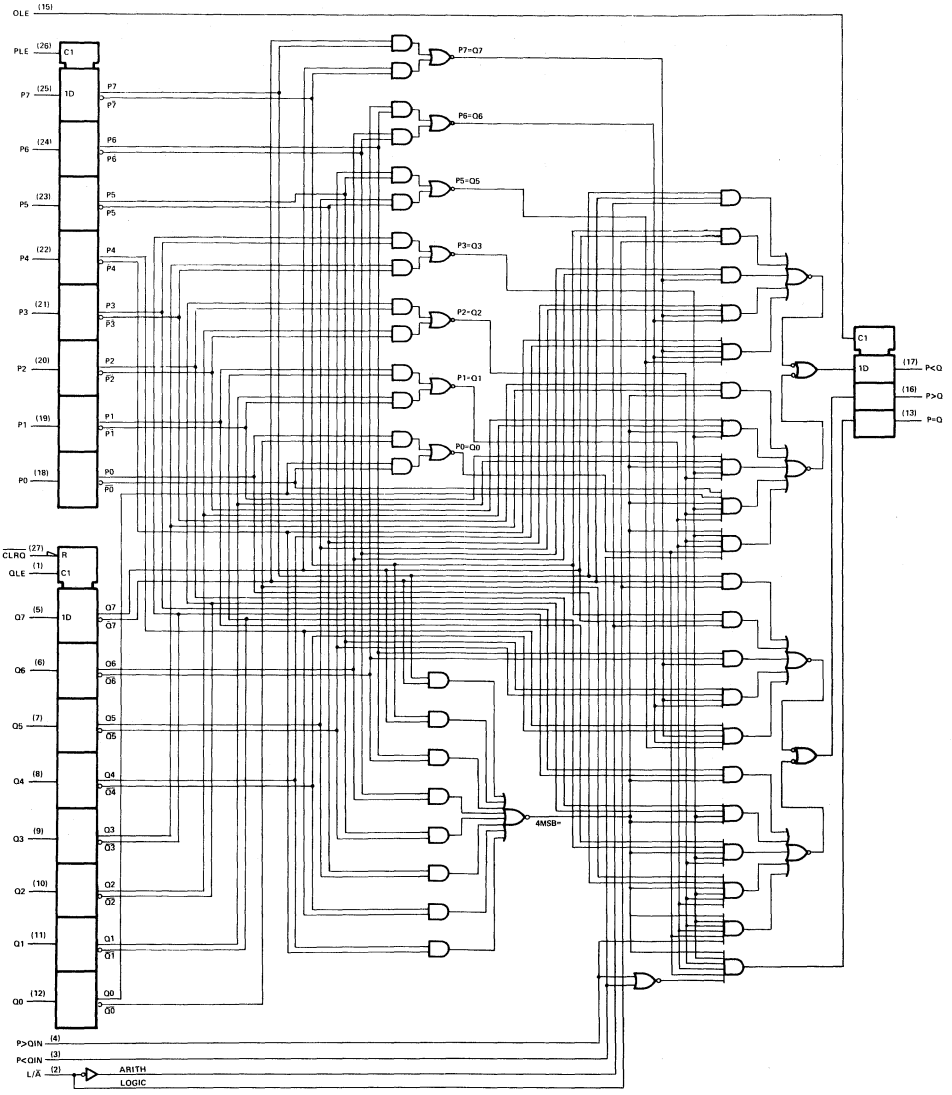
logic symbol



Pin numbers shown are for JD and N packages.

2

logic diagram (positive logic)



FUNCTION TABLE

COMPARISON	L/$\overline{A}$	DATA INPUTS P0-P7, Q0-Q7	INPUTS		OUTPUTS		
			P > Q	P < Q	P > Q	P < Q	P = Q
Logical	H	P > Q	X	X	H	L	L
Logical	H	P < Q	X	X	L	H	L
Logical	H	P = Q	L	L	L	L	H
Logical	H	P = Q	L	H	L	H	L
Logical	H	P = Q	H	L	H	L	L
Logical	H	P = Q	H	H	H	H	L
Arithmetic	L	P AG Q	X	X	H	L	L
Arithmetic	L	Q AG P	X	X	L	H	L
Arithmetic	L	P = Q	L	L	L	L	H
Arithmetic	L	P = Q	L	H	L	H	L
Arithmetic	L	P = Q	H	L	H	L	L
Arithmetic	L	P = Q	H	H	H	H	L

AG = arithmetically greater than

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage, P = Q output . . . . . 7 V
Operating free-air temperature range: SN54AS866 . . . . . −55 °C to 125 °C
SN74AS866 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

PARAMETER		SN54AS866			SN74AS866			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current, all outputs except P = Q			−2			−2	mA
V_{OH}	High-level output voltage, P = Q output			5.5			5.5	V
I_{OL}	Low-level output current			20			20	mA
t_{su}	Setup time to PLE, QLE, OLE↓	2			2			ns
t_h	Hold time after PLE, QLE, OLE↓	4			4			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS866			SN74AS866			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	P > Q, P < Q	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			
I_{OH}	P = Q only	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			250			250	μA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	L/$\overline{A}$, OLE	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	Others					20			20	
I_{IL}	L/$\overline{A}$, OLE, P > Qin, P < Qin	V_{CC} = 5.5 V,	V_I = 0.4 V			−4			−4	mA
	$\overline{CLRQ}$					−2			−2	
	P, Q, PLE, QLE				−0.25	−1		−0.25	−1	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−20		−112	−20		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		160	240		160	240	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit, I_{OS}.
NOTE 1: I_{CC} is measured with all inputs high except L/A, which is low.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4..5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS866			SN74AS866			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	L/$\overline{A}$	P < Q, P > Q	1	8.5	14	1	8.5	13	ns
t_{PHL}			1	7.5	14	1	7.5	13	
t_{PLH}	P < Q, P > Q		1	5	10	1	5	8	ns
t_{PLH}			1	5.5	10	1	5.5	8	
t_{PHL}	Any P or Q Data Input		1	13.5	21	1	13.5	17.5	ns
t_{PHL}			1	10	17	1	10	15	
t_{PLH}	$\overline{CLRQ}$		1	16	21	1	16	20	ns
t_{PHL}			1	12	17	1	12	16	

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_A = 280 Ω, T_A = MIN to MAX						UNIT
			SN54AS866			SN74AS866			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	P < Q, P > Q	P = Q	1	6.5	12	1	6.5	11	ns
t_{PHL}			1	8	14	1	8	13	
t_{PLH}	Any P or Q Data Input	P = Q	1	10	15	1	10	14	ns
t_{PHL}			1	9	14	1	9	13	
t_{PLH}	$\overline{CLRQ}$	P = Q	1	12	17	1	12	16	ns
t_{PHL}			1	13	18	1	13	17	

†All typical vallues ree at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: For load circuit and voltage waveforms, see page 1-12.

TYPICAL APPLICATION DATA

This sequence of comparisons illustrates how the $\overline{CLRQ}$ function can be used to perform dual comparisons of the varying P terms (P0, P1, etc). When $\overline{CLRQ}$ is high, the P term is compared to the Q term. When $\overline{CLRQ}$ is taken low, the P term is compared to zero. This or similar sequences can enhance performance and reduce package count to perform value range checks.

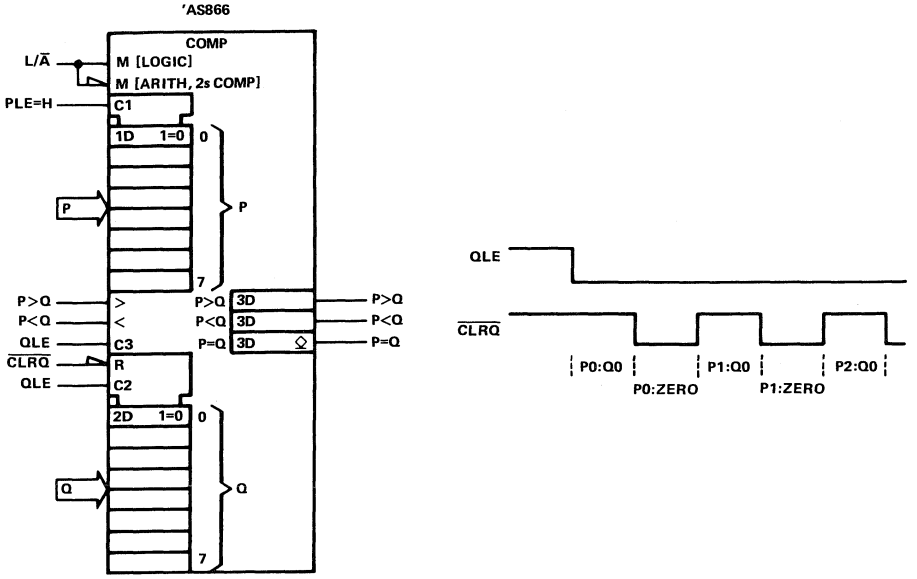
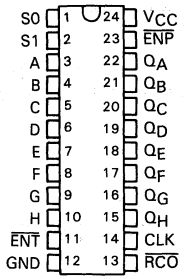


FIGURE 1–MAGNITUDE COMPARISONS COMBINED WITH QUICK COMPARISONS TO ZERO (RANGE VERIFICATIONS)

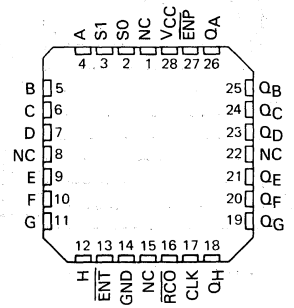
D2661, DECEMBER 1982—REVISED DECEMBER 1983

- Included among the Package Options are Compact 24-Pin, 300-Mil-Wide Dips and Small Outline (SO) and 28-Pin Ceramic Chip Carriers
- Fully Programmable with Synchronous Counting and Loading
- 'AS867 Has Asynchronous Clear, 'AS869 Has Synchronous Clear
- Fully Independent Clock circuit Simplifies Use
- Ripple Carry Output for n-Bit Cascading
- Improved Performance Compared to Schottky TTL:
  - Typical Power Reduced by 38%
  - Maximum Count Frequency is 25% Higher
- Dependable Texas Instruments Quality and Reliability

SN54AS867, SN54AS869 . . . JT PACKAGE
SN74AS867, SN74AS869 . . . NT PACKAGE
SN74AS867, SN74AS869 . . . DW PACKAGE
(TOP VIEW)



SN54AS867, SN54AS869 . . . FH OR FK PACKAGE
SN74AS867, SN74AS869 . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the eight flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset to either level. The load mode circuitry allows parallel loading of the cascaded counters. As loading is synchronous, selecting the load mode disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

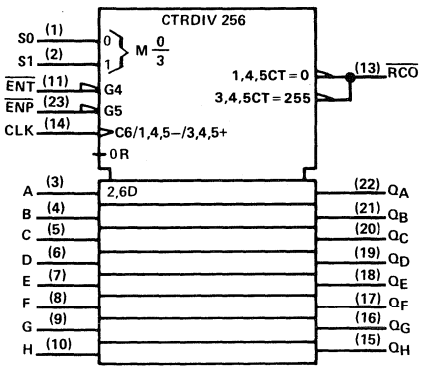
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ($\overline{ENP}$ and $\overline{ENT}$) must be low to count. The direction of the count is determined by the levels of the select inputs (see Function Table). Input $\overline{ENT}$ is fed forward to enable the carry output. The ripple carry output thus enabled will produce a low-level pulse while the count is zero (all outputs low) counting down or 255 counting up (all outputs high). This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the enable $\overline{ENP}$ and $\overline{ENT}$ inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

These counters feature a fully independent clock circuit. With the exception of thee asynchronous clear on the 'AS867, changes at control inputs (S0, S1) that will modify the operating mode have no effect on the Q outputs until clocking occurs. Anytime the $\overline{ENP}$ and/or $\overline{ENT}$ is taken high, $\overline{RCO}$ will either go or remain high. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

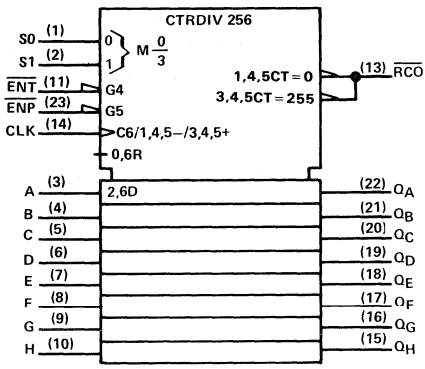
The SN54AS867 and SN54AS869 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS867 and SN74AS869 are characterized for operation from 0°C to 70°C.

logic symbols

'AS867



'AS869



Pin numbers shown are for JT and NT packages.

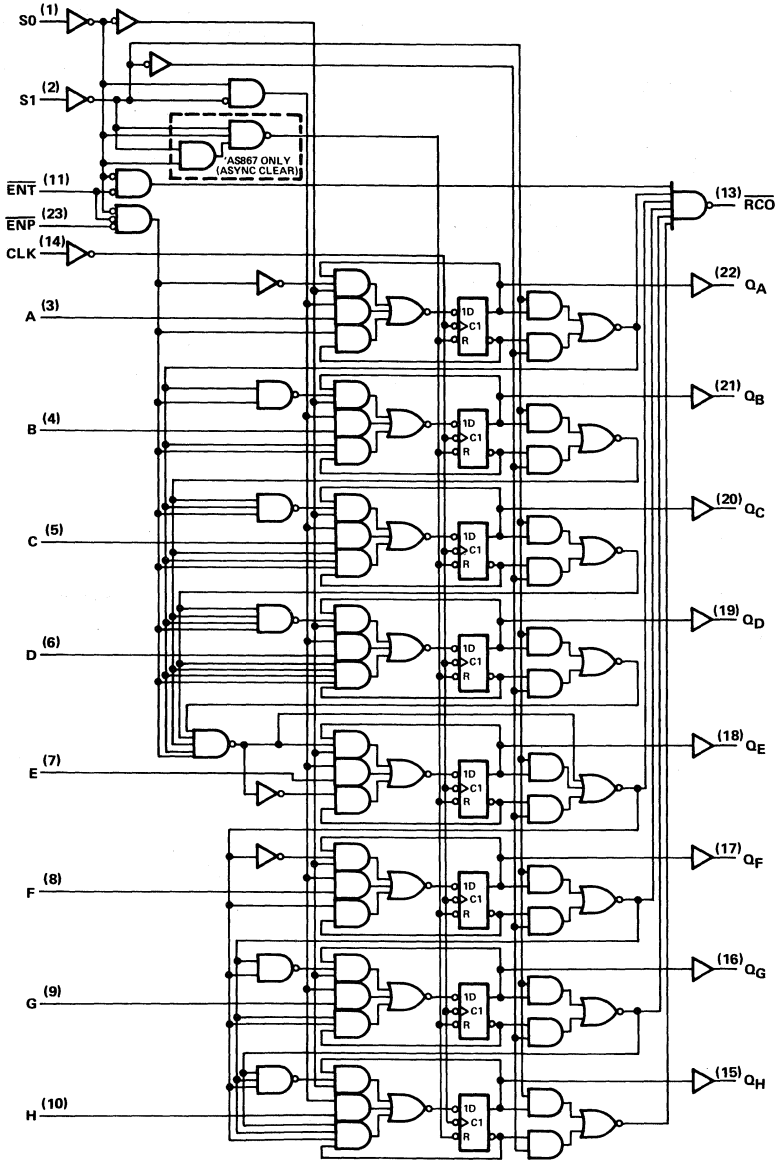
FUNCTION TABLE

S1	S0	FUNCTION
L	L	Clear
L	H	Count down
H	L	Load
H	H	Count up

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature: SN54AS867, SN54AS869 . . . . . −55°C to 125°C
SN74AS867, SN74AS869 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

logic diagram (positive logic)



recommended operating conditions

			SN54AS867			SN74AS867			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0		40	0		50	MHz
$t_{w(clock)}$	Duration		12.5			10			ns
$t_{w(clear)}$	Duration of clear pulse (S0 and S1 low)		12.5			10			ns
t_{su}	Setup time†	Data inputs A-H	5			4			ns
		Enable P ($\overline{ENP}$) or Enable T ($\overline{ENT}$)	9			8			ns
		S0 or S1 (load)	11			10			ns
		S0 or S1 (clear)	11			10			ns
		S0 or S1 (count down)	42			40			ns
		S0 or S1 (count up)	42			40			ns
t_h	Hold time at any input with respect to clock↑		0			0			ns
t_{skew}	Skew time between S0 and S1 (maximum to avoid inadvertent clear)		8			7			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

†This setup time is required to ensure stable data.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS867			SN74AS867			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = 18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.34	0.5		0.34	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	$\overline{ENT}$	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	Other inputs					20			20	
I_{IL}	$\overline{ENT}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−4			−4	mA
	Other inputs					−2			−2	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			134	195		134	195	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

recommended operating conditions

			SN54AS869			SN74AS869			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0		40	0		45	MHz
$t_{w(clock)}$	Duration		12.5			11			ns
t_{su}	Setup time†	Data inputs A-H	6			5			ns
		Enable P ($\overline{ENP}$) or Enable T ($\overline{ENT}$)	10			9			ns
		S0 or S1 (load)	13			11			ns
		S0 or S1 (clear)	13			11			ns
		S0 or S1 (count down)	52			50			ns
		S0 or S1 (count up)	52			50			ns
t_h	Hold time at any input with respect to clock†		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

†This setup time is required to ensure stable data.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS869			SN74AS869			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = 18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.34	0.5		0.34	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	$\overline{ENT}$	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	Other inputs					20			20	
I_{IL}	$\overline{ENT}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−4			−4	mA
	Other inputs					−2			−2	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			125	180		125	180	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS867 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS867		SN74AS867		
			MIN	MAX	MIN	MAX	
f_{max}			40		50		MHz
t_{PLH}	CLK	$\overline{RCO}$	5	31	5	22	ns
t_{PHL}			6	19	6	16	
t_{PLH}	CLK	Any Q	3	12	3	11	ns
t_{PHL}			4	16	4	15	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	3	19	3	10	ns
t_{PHL}			5	21	5	17	
t_{PLH}	$\overline{ENP}$	$\overline{RCO}$	5	14	5	14	ns
t_{PHL}			5	21	5	17	
t_{PHL}	Clear (S0, S1 low)	Any Q	7	23	7	21	ns

'AS869 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS869		SN74AS869		
			MIN	MAX	MIN	MAX	
f_{max}			40		45		MHz
t_{PLH}	CLK	$\overline{RCO}$	6	35	6	35	ns
t_{PHL}			6	20	6	18	
t_{PLH}	CLK	Any Q	3	12	3	11	ns
t_{PHL}			4	16	4	15	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	3	25	3	15	ns
t_{PHL}			6	21	6	17	
t_{PLH}	$\overline{ENP}$	$\overline{RCO}$	5	27	5	19	ns
t_{PHL}			6	21	6	18	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D2661, DECEMBER 1982—REVISED DECEMBER 1983

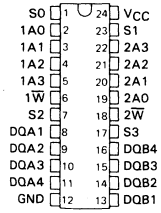
- 'AS870 in Compact 24-Pin, 300-mil DIP and Small Outline (SO) and Plastic and Ceramic 28-Pin Chip Carriers
- 'AS871 in 28-Pin 600-mil DIP and Both Plastic and Ceramic Chip Carriers
- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Typical Access Time Is 11 ns
- Each Register File Has Individual Write Enable Controls and Address Lines
- Designed Specifically for Multibus Architecture and Overlapping File Operations
- Prioritized B Input Port Prevents Write Conflicts During Dual Input Mode
- Dependable Texas Instruments Quality and Reliability

description

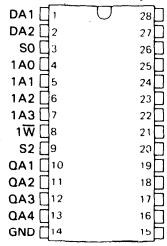
These devices feature two 16-word by 4-bit register files. Each register file has individual write-enable controls and address lines. The 'AS870 has two 4-bit data I/O ports (DQA1-DQA4 and DQB1-DQB4). The 'AS871 has one 4-bit data I/O port (DQB1-DQB4) with the other data port having individual data inputs (DA1-DA4) and data outputs (QA1-QA4). The data I/O ports can output to Bus A and Bus B, receive input from Bus A and Bus B, receive input from Bus A and output to Bus B, or output to Bus A and receive input from Bus B. To prevent writing conflicts in the dual-input mode, the B input port takes priority. Two select lines, S0 and S1, control which port has access to which register. S2 determines whether the A ports are in the input or the output modes and S3 does likewise for the B ports. The address lines (1A0-1A3 or 2A0-2A3) are decoded by an internal 1-of-16 decoder to select which register word is to be accessed. All outputs are 3-state buffer-type outputs designed specifically to drive bus lines directly.

The SN54AS870 and SN54AS871 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS870 and SN74AS871 are characterized for operation from 0°C to 70°C.

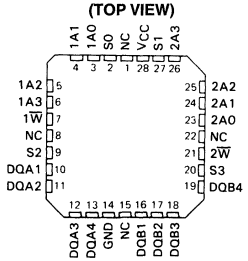
SN54AS870 . . . JT PACKAGE
SN74AS870 . . . NT PACKAGE
SN74AS870 . . . DW PACKAGE
(TOP VIEW)



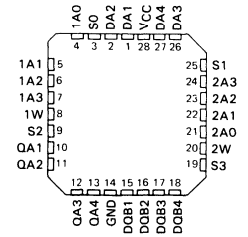
SN54AS871 . . . JD PACKAGE
SN74AS871 . . . N PACKAGE
(TOP VIEW)



SN54AS870 . . . FH OR FK PACKAGE
SN74AS870 . . . FN PACKAGE
(TOP VIEW)



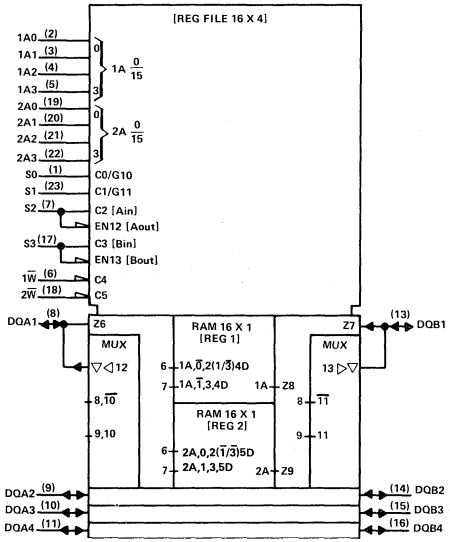
SN54AS871 . . . FH OR FK PACKAGE
SN74AS871 . . . FN PACKAGE
(TOP VIEW)



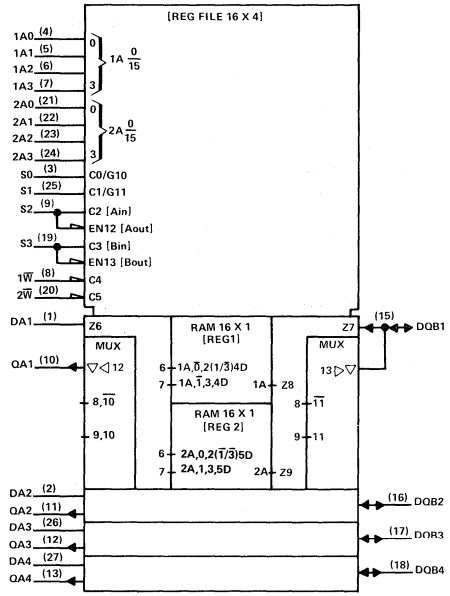
NC — No internal connection

logic symbols

'AS870



'AS871



Pin numbers shown are for JD, JT, N, and NT packages.

FUNCTION TABLE

FILE SELECT			INPUT/OUTPUT		
S0	S1	FILE SEL	S2	S3	I/O SEL
L	L	1R TO A, 1R TO B	L	L	A OUT, B OUT
H	L	2R TO A, 1R TO B			
L	H	1R TO A, 2R TO B			
H	H	2R TO A, 2R TO B			
L	L	A TO 1R, 1R TO B	H	L	A IN, B OUT
H	L	A TO 2R, 1R TO B			
L	H	A TO 1R, 2R TO B			
H	H	A TO 2R, 2R TO B			
L	L	1R TO A, B TO 1R	L	H	A OUT, B IN
H	L	2R TO A, B TO 1R			
L	H	1R TO A, B TO 2R			
H	H	2R TO A, B TO 2R			
L	L	B TO 1R	H	H	A IN, B IN
H	L	A TO 2R, B TO 1R			
L	H	A TO 1R, B TO 2R			
H	H	B TO 2R			

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS870, SN54AS871 . . . . . −55 °C to 125 °C
SN74AS870, SN74AS871 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54AS870 SN54AS871			SN74AS870 SN74AS871			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				32			48	mA
t_w	Duration of write pulse		12			12			ns
t_{su}	Setup times	Address before write↓	5			5			ns
		Data before write↑	15			15			
		Select before write↓	12			12			
t_h	Hold times	Address after write↑	0			0			ns
		Data after write↑	0			0			
		Select after write↑	12			12			
T_A	Operating free-air temperature		−55		125	0		70	°C

'AS870 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS870			SN74AS870			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	DQA and DQB ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.2			0.2	
I_{IH}	W1 and W2	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	Other control inputs					40			40	
	DQA and DQB ports‡					50			50	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−2			−2	mA
	DQA and DQB ports‡					−2			−2	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			120	190		120	190	mA

'AS871 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS871			SN74AS871			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}	QA outputs	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	QA outputs	V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I	Control and DA inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	DQB ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.2			0.2	
I_{IH}	W1, W2 and DA inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	Other control inputs					40			40	
	DQB ports‡					50			50	
I_{IL}	Control and DA inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−2			−2	mA
	DQB ports‡					−2			−2	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			120	190		120	190	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the output currents I_{IOZ} and I_{OZL}, respectively.
§The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

'AS870 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS870		SN74AS870		
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Any A	Any DQ	5	20	5	15	ns
$t_{a(S)}$	S0	Any DQA	3	15	3	13	ns
	S1	Any DQB	3	15	3	13	
t_{dis}	S2	Any DQA	3	12	3	11	ns
	S3	Any DQB	3	12	3	11	
t_{en}	S2	Any DQA	3	15	3	12	ns
	S3	Any DQB	3	15	3	12	
t_{pd}	$\overline{W}$	Any DQ	5	23	5	19	ns
	DQA	DQB	5	25	5	22	
	DQB	DQA	5	25	5	22	

'AS871 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS871		SN74AS871		
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Any A	Any QA or DQB	5	20	5	16	ns
$t_{a(S)}$	S0	Any QA	3	15	3	13	ns
	S1	Any DQB	3	15	3	13	
t_{dis}	S2	Any QA	3	12	3	11	ns
	S3	Any DQB	3	12	3	11	
t_{en}	S2	Any QA	3	15	3	12	ns
	S3	Any DQB	3	15	3	12	
t_{pd}	$\overline{W}$	Any QA or DQB	5	23	5	19	ns
	DA	DQB	5	26	5	23	
	DQB	QA	5	26	5	23	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D2661, APRIL 1982—REVISED SEPTEMBER 1984

- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **'ALS880 and 'AS880 Are Alternative Versions with Inverting Outputs**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These dual 4-bit registers feature three-state outputs designed specifically for bus driving. This makes these devices particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

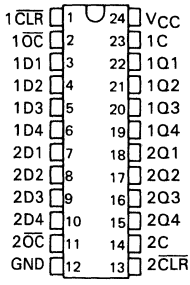
The dual 4-bit latches are transparent D-type. While the latch enable input (1C or 2C) is high, the Q outputs will follow the data (D) inputs in true form, according to the function table. When the latch enable input is taken low, the outputs will be latched. When $\overline{CLR}$ goes low, the Q outputs go low independently of enable C. The outputs are in a high-impedance state when $\overline{OC}$ (output control) is at a high logic level.

The SN54ALS873A and SN54AS873 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS873A and SN74AS873 are characterized for operation from 0°C to 70°C.

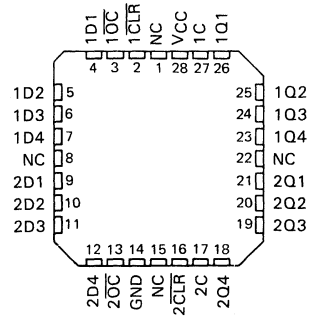
FUNCTION TABLE (EACH LATCH)

INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	ENABLE C	D	Q
L	L	X	X	L
L	H	H	H	H
L	H	H	L	L
L	H	L	X	Q_0
H	X	X	X	Z

SN54ALS873A, SN54AS873 . . . JT PACKAGE
SN74ALS873A, SN74AS873 . . . NT PACKAGE
SN74ALS873A, SN74AS873 . . . DW PACKAGE
(TOP VIEW)

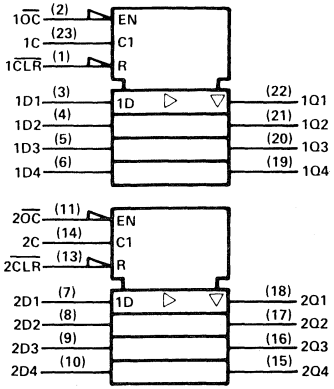


SN54ALS873A, SN54AS873 . . . FH OR FK PACKAGE
SN74ALS873A, SN74AS873 . . . FN PACKAGE
(TOP VIEW)

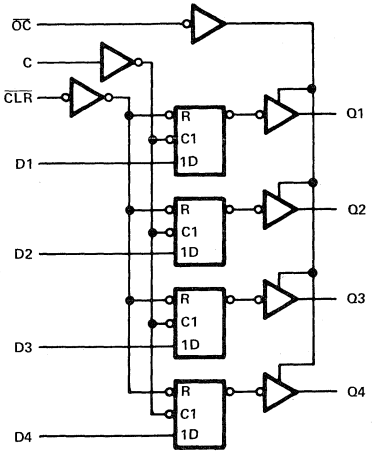


NC—No internal connection

logic symbol



functional block diagram (each quad latch, positive logic)



Pin numbers shown are for JT and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS873A, SN54AS873 . . . . . −55°C to 125°C
SN74ALS873A, SN74AS873 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS873A			SN74ALS873A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
t_w	Pulse duration	$\overline{CLR}$ low	15			15			ns
		Enable C high	10			10			
t_{su}	Setup time, data before enable C↓		10			10			ns
t_h	Hold time, data after enable C↓		7			7			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS873A			SN74ALS873A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		11	21		11	21	mA
		Outputs low		16	29		16	29	
		Outputs disabled		20	31		20	31	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

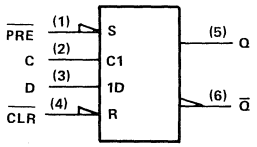
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54/74ALS873A			SN54ALS873A		SN74ALS873A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q		8	10	2	15	2	14	ns
t_{PHL}				9	12	2	15	2	14	
t_{PLH}	C	Q		13	17	8	22	8	21	ns
t_{PHL}				13	17	8	22	8	21	
t_{PHL}	$\overline{CLR}$	Q		13	18	6	23	6	20	ns
t_{PZH}	$\overline{OC}$	Q		10	13	4	21	4	18	ns
t_{PZL}				12	16	4	21	4	18	
t_{PHZ}	$\overline{OC}$	Q		5.5	7	2	12	2	10	ns
t_{PLZ}				6	8	2	15	2	12	

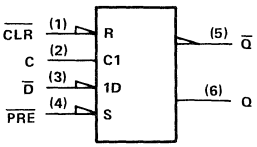
NOTE 1: For load circuit and voltage waveforms, see page 1-12

D latch signal conventions

It is TI practice to name the outputs and other inputs of a D-type latch and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active low.

In some applications it may be advantageous to redesignate the data input $\overline{D}$. In that case all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.





Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (⊳) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 ($\overline{Q}$) is still in phase with the data input $\overline{D}$, but now both are considered active-low.

recommended operating conditions

			SN54AS873			SN74AS873			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				32			48	mA
t_w	Pulse duration	$\overline{CLR}$ low	4.5			3.5			ns
		Enable C high	5.5			4.5			
t_{su}	Setup time, data before enable C↓		2			2			ns
t_h	Hold time, data after enable C↓		3			3			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS873			SN74AS873			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		68	110		68	110	mA
		Outputs low		67	109		67	109	
		Outputs disabled		80	129		80	129	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS873		SN74AS873		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	3	9	3	6	ns
t_{PHL}			3	7	3	6	
t_{PLH}	C	Q	6	14	6	11.5	ns
t_{PHL}			4	9	4	7.5	
t_{PHL}	$\overline{CLR}$	Q	3	8.5	3	7.5	ns
t_{PZH}	$\overline{OC}$	Q	2	8	2	6.5	ns
t_{PZL}			4	11	4	9.5	
t_{PHZ}	$\overline{OC}$	Q	2	8	2	6.5	ns
t_{PLZ}			2	8.5	2	7.5	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS

D2661, APRIL 1982—REVISED SEPTEMBER 1984

- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **Choice of True or Inverting Logic**

  'ALS874A, 'AS874 True Outputs
  'ALS876, 'AS876 Inverting Outputs
- **Asynchronous Clear**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

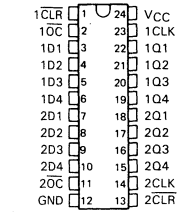
description

These dual four-bit registers feature three-state outputs designed specifically for bus driving. This makes these devices paricularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

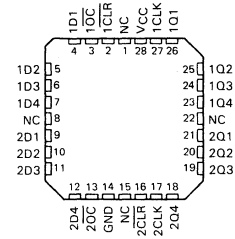
The edge-triggered flip-flops enter data on the low-to-high transition of the clock. The 'ALS874A and 'AS874 have CLR inputs and noninverting Q outputs; the 'ALS876 and 'AS876 have PRE inputs and inverting Q outputs. In each case, taking this input low causes the four Q or Q outputs to go low independently of the clock.

The SN54ALS874A, SN54AS874, SN54ALS876 and SN54AS876 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS874A, SN74AS874, SN74ALS876, and SN74AS876 are characterized for operation from 0°C to 70°C.

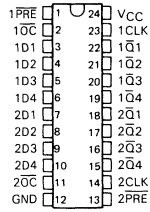
SN54ALS874A, SN54AS874 . . . JT PACKAGE
SN74ALS874A, SN74AS874 . . . NT PACKAGE
SN74ALS874A, SN74AS874 . . . DW PACKAGE
(TOP VIEW)



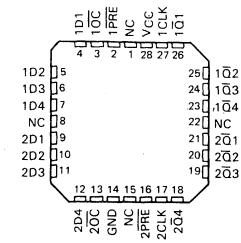
SN54ALS874A, SN54AS874 . . . FH OR FK PACKAGE
SN74ALS874A, SN74AS874 . . . FN PACKAGE
(TOP VIEW)



SN54ALS876, SN54AS876 . . . JT PACKAGE
SN74ALS876, SN74AS876 . . . NT PACKAGE
SN74ALS876, SN74AS876 . . . DW PACKAGE
(TOP VIEW)



SN54ALS876, SN54AS876 . . . FH OR FK PACKAGE
SN74ALS876, SN74AS876 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

FUNCTION TABLES

'ALS874A, 'AS874 (EACH FLIP-FLOP)

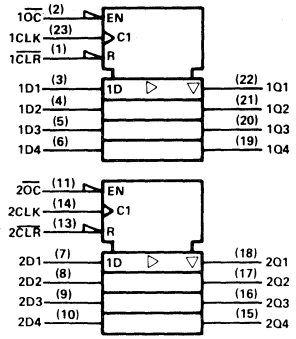
INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	CLK	D	Q
L	L	X	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	Q_0
H	X	X	X	Z

'ALS876, 'AS876 (EACH FLIP-FLOP)

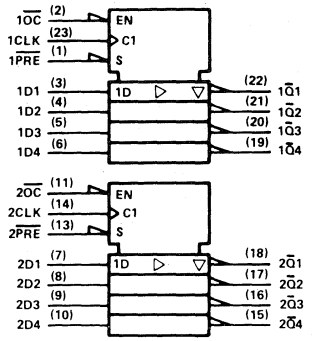
INPUTS				OUTPUT
OC	$\overline{PRE}$	CLK	D	$\overline{Q}$
L	L	X	X	L
L	H	↑	H	L
L	H	↑	L	H
L	H	L	X	$\overline{Q}_0$
H	X	X	X	Z

logic symbols

'ALS874A, 'AS874

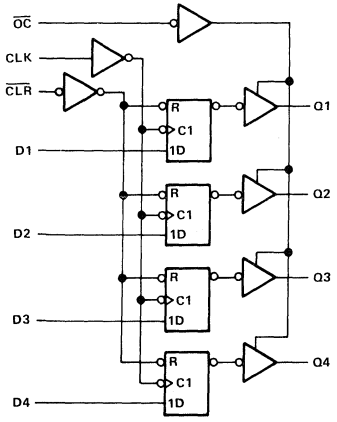


'ALS876, 'AS876

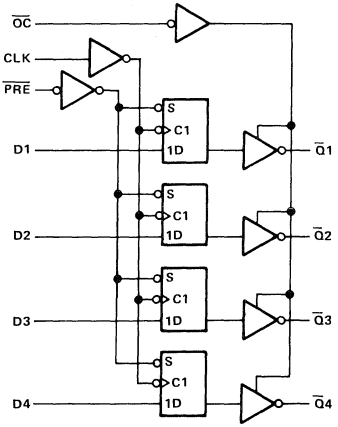


logic diagrams (positive logic)

'ALS874A, 'AS874 (EACH QUAD FLIP-FLOP)



'ALS876, 'AS876 (EACH QUAD FLIP-FLOP)



Pin numbers shown are for JT and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS874A, SN54ALS876 . . . . . −55°C to 125°C
SN74ALS874A, SN74ALS876 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS874A SN54ALS876			SN74ALS874A SN74ALS876			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency		0		25	0		30	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	10			10			ns
		CLK high	20			16.5			
		CLK low	20			16.5			
t_{su}	Setup time before CLK↑	Data	15			15			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	10			10			
t_h	Hold time, data after CLK↑		4			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS874A SN54ALS876			SN74ALS874A SN74ALS876			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	$V_{CC}-2$			$V_{CC}-2$			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS874A	V_{CC} = 5.5 V	Output high		14	21		14	21	mA
			Outputs low		19	30		19	30	
			Outputs disabled		20	32		20	32	
	'ALS876		Outputs high		14	21		14	21	
			Outputs low		18	29		18	29	
			Outputs disabled		20	31		20	31	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS874A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54/74ALS874A			SN54ALS874A		SN74ALS874A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			40	50		25		30		MHz
t_{PLH}	CLK	Any Q		8	10	4	15	4	14	ns
t_{PHL}				8	13	4	15	4	14	
t_{PHL}	$\overline{CLR}$	Any Q		11	14	5	20	5	17	ns
t_{PZH}	$\overline{OC}$	Any Q		9	12	4	21	4	18	ns
t_{PZL}				11	15	4	21	4	18	
t_{PHZ}	$\overline{OC}$	Any Q		6	8	2	12	2	10	ns
t_{PLZ}				5.7	7	3	15	3	12	

'ALS876 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS876		SN74ALS876		
			MIN	MAX	MIN	MAX	
f_{max}			25		30		MHz
t_{PLH}	CLK	Any $\overline{Q}$	4	15	4	14	ns
t_{PHL}			4	15	4	14	
t_{PHL}	$\overline{PRE}$	Any $\overline{Q}$	6	22	6	19	ns
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$	4	21	4	18	ns
t_{PZL}			4	21	4	18	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$	2	10	2	8	ns
t_{PLZ}			3	15	3	13	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS874, SN54AS876 . . . . . −55°C to 125°C
SN74AS874, SN74AS876 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS874 SN54AS876			SN74AS874 SN74AS876			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				32			48	mA
f_{clock}	Clock frequency		0		100	0		125	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	3			2			ns
		CLK high	4			3			
		CLK low	5			4			
t_{su}	Setup time before CLK↑	Data	2.5			2			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	5			4			
t_h	Hold time, data after CLK↑		1			1			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS874 SN54AS876			SN74AS874 SN74AS876			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.4				V
		V_{CC} = 4.5 V	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			10	μA
I_{IL}	D	V_{CC} = 5.5 V,	V_I = 0.4 V			−3			−2	mA
	All other					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS874	V_{CC} = 5.5 V	Output high		82	133		82	133	mA
			Outputs low		92	149		92	149	
			Outputs disabled		100	160		100	160	
	'AS876		Outputs high		88	142		88	142	
			Outputs low		94	150		94	150	
			Outputs disabled		100	160		100	160	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS874 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS874		SN74AS874		
			MIN	MAX	MIN	MAX	
f_{max}			100		125		MHz
t_{PLH}	CLK	Any Q	3	11.5	3	8.5	ns
t_{PHL}			4	12.5	4	10.5	
t_{PHL}	$\overline{CLR}$	Any Q	4	11	4	9.5	ns
t_{PZH}	$\overline{OC}$	Any Q	2	8	2	7	ns
t_{PZL}			3	11.5	3	10.5	
t_{PHZ}	$\overline{OC}$	Any Q	2	7	2	6	ns
t_{PLZ}			2	8.5	2	7.5	

'AS876 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS876		SN74AS876		
			MIN	MAX	MIN	MAX	
f_{max}			100		125		MHz
t_{PLH}	CLK	Any $\overline{Q}$	3	11.5	3	8.5	ns
t_{PHL}			4	12.5	4	10.5	
t_{PHL}	$\overline{PRE}$	Any $\overline{Q}$	4	11	4	9.5	ns
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$	2	8	2	7	ns
t_{PZL}			3	11.5	3	10.5	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$	2	7	2	6	ns
t_{PLZ}			2	7	2	6	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **Choice of True or Inverting Logic**

  'ALS874, 'AS874 — True Outputs
  'ALS876, 'AS876 — Inverting Outputs

- **Asynchronous Clear**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

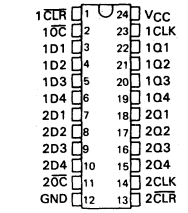
description

These dual four-bit registers feature three-state outputs designed specifically for bus driving. This makes these devices particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

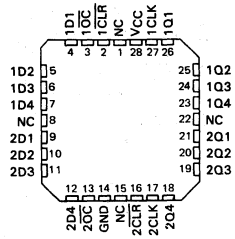
The edge-triggered flip-flops enter data on the low-to-high transition of the clock. The 'ALS874 and 'AS874 have $\overline{CLR}$ inputs and noninverting Q outputs; the 'ALS876 and 'AS876 have $\overline{PRE}$ inputs and inverting $\overline{Q}$ outputs. In each case, taking this input low causes the four Q or $\overline{Q}$ outputs to go low independently of the clock.

The SN54ALS874, SN54AS874, SN54ALS876 and SN54AS876 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS874, SN74AS874, SN74ALS876, and SN74AS876 are characterized for operation from 0°C to 70°C.

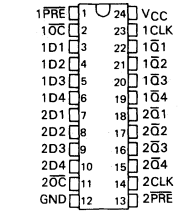
SN54ALS874, SN54AS874 . . . JT PACKAGE
SN74ALS874, SN74AS874 . . . NT PACKAGE
SN74ALS874, SN74AS874 . . . DW PACKAGE
(TOP VIEW)



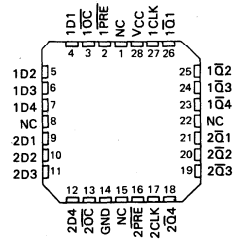
SN54ALS874, SN54AS874 . . . FH OR FK PACKAGE
SN74ALS874, SN74AS874 . . . FN PACKAGE
(TOP VIEW)



SN54ALS876, SN54AS876 . . . JT PACKAGE
SN74ALS876, SN74AS876 . . . NT PACKAGE
SN74ALS876, SN74AS876 . . . DW PACKAGE
(TOP VIEW)



SN54ALS876, SN54AS876 . . . FH OR FK PACKAGE
SN74ALS876, SN74AS876 . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

FUNCTION TABLES

'ALS874, 'AS874 (EACH FLIP-FLOP)

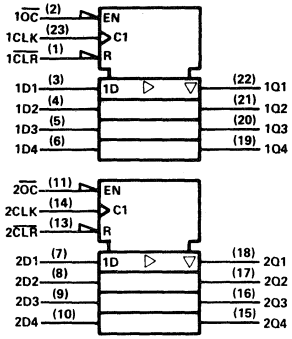
INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	CLK	D	Q
L	L	X	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	Q_0
H	X	X	X	Z

'ALS876, 'AS876 (EACH FLIP-FLOP)

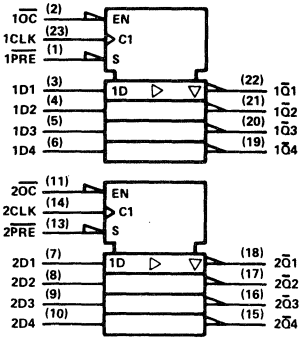
INPUTS				OUTPUT
$\overline{OC}$	$\overline{PRE}$	CLK	D	$\overline{Q}$
L	L	X	X	L
L	H	↑	H	L
L	H	↑	L	H
L	H	L	X	$\overline{Q}_0$
H	X	X	X	Z

logic symbols

'ALS874, 'AS874

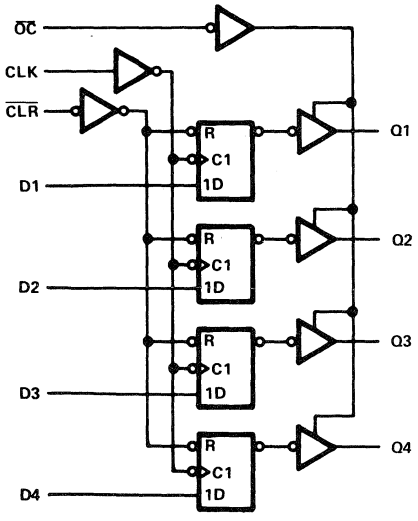


'ALS876, 'AS876

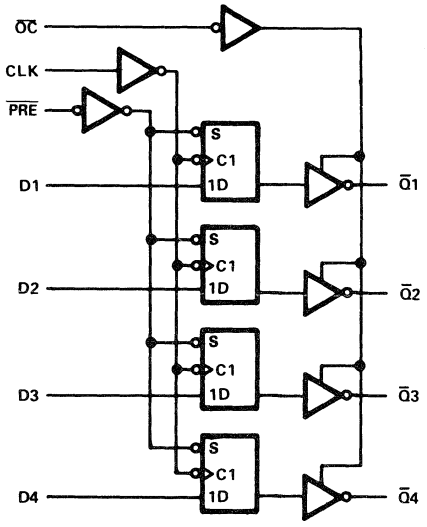


logic diagrams (positive logic)

'ALS874, 'AS874 (EACH QUAD FLIP-FLOP)



'ALS876, 'AS876 (EACH QUAD FLIP-FLOP)



Pin numbers shown are for JT and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS874, SN54ALS876 . . . . . −55°C to 125°C
SN74ALS874, SN74ALS876 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS874 SN54ALS876			SN74ALS874 SN74ALS876			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency		0		25	0		30	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	10			10			ns
		CLK high	20			16.5			
		CLK low	20			16.5			
t_{su}	Setup time before CLK↑	Data	15			15			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	10			10			
t_h	Hold time, data after CLK↑		4			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS874 SN54ALS876			SN74ALS874 SN74ALS876			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		14	21		14	21	mA
		Outputs low		18	29		18	29	
		Outputs disabled		20	31		20	31	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS874 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS874		SN74ALS874		
			MIN	MAX	MIN	MAX	
f_{max}			25		30		MHz
t_{PLH}	CLK	Any Q	4	15	4	14	ns
t_{PHL}			4	15	4	14	
t_{PHL}	$\overline{CLR}$	Any Q	6	22	6	19	ns
t_{PZH}	$\overline{OC}$	Any Q	4	21	4	18	ns
t_{PZL}			4	21	4	18	
t_{PHZ}	$\overline{OC}$	Any Q	2	10	2	8	ns
t_{PLZ}			3	15	3	13	

'ALS876 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS876		SN74ALS876		
			MIN	MAX	MIN	MAX	
f_{max}			25		30		MHz
t_{PLH}	CLK	Any $\overline{Q}$	4	15	4	14	ns
t_{PHL}			4	15	4	14	
t_{PHL}	$\overline{PRE}$	Any $\overline{Q}$	6	22	6	19	ns
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$	4	21	4	18	ns
t_{PZL}			4	21	4	18	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$	2	10	2	8	ns
t_{PLZ}			3	15	3	13	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS874, SN54AS876 . . . . . −55°C to 125°C
SN74AS874, SN74AS876 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS874 SN54AS876			SN74AS874 SN74AS876			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				32			48	mA
f_{clock}	Clock frequency		0		100	0		125	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	3			2			ns
		CLK high	4			3			
		CLK low	5			4			
t_{su}	Setup time before CLK↑	Data	2.5			2			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	5			4			
t_h	Hold time, data after CLK↑		1			1			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS874 SN54AS876			SN74AS874 SN74AS876			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	D	V_{CC} = 5.5 V,	V_I = 0.4 V			−3			−2	mA
	All other					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS874	V_{CC} = 5.5 V	Outputs high		82	133		82	133	mA
			Outputs low		92	149		92	149	
			Outputs disabled		100	160		100	160	
	'AS876		Outputs high		88	142		88	142	
			Outputs low		94	150		94	150	
			Outputs disabled		100	160		100	160	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS874 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS874		SN74AS874		
			MIN	MAX	MIN	MAX	
f_{max}			100		125		MHz
t_{PLH}	CLK	Any Q	3	11.5	3	8.5	ns
t_{PHL}			4	12.5	4	10.5	
t_{PHL}	$\overline{CLR}$	Any Q	4	11	4	9.5	ns
t_{PZH}	$\overline{OC}$	Any Q	2	8	2	7	ns
t_{PZL}			3	11.5	3	10.5	
t_{PHZ}	$\overline{OC}$	Any Q	2	7	2	6	ns
t_{PLZ}			2	8.5	2	7.5	

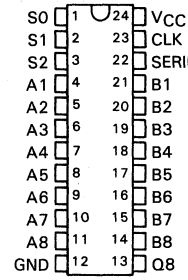
'AS876 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS876		SN74AS876		
			MIN	MAX	MIN	MAX	
f_{max}			100		125		MHz
t_{PLH}	CLK	Any $\overline{Q}$	3	11.5	3	8.5	ns
t_{PHL}			4	12.5	4	10.5	
t_{PHL}	$\overline{PRE}$	Any $\overline{Q}$	4	11	4	9.5	ns
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$	2	8	2	7	ns
t_{PZL}			3	11.5	3	10.5	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$	2	7	2	6	ns
t_{PLZ}			2	7	2	6	

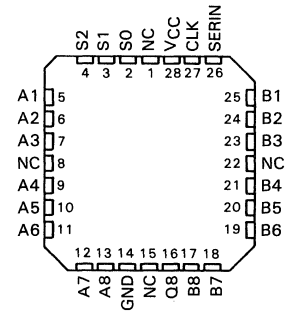
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- Included among the Package Options Are Compact, 24-Pin, 300-mil-Wide Dips and Small Outline (SO) and 28-Pin Plastic and Ceramic Chip Carriers
- Buffered 3-State Outputs Drive Bus Lines Directly
- Cascadable to n-Bits
- Eight Selectable Transceiver/Port Functions:
  - A to B or B to A
  - Register to A or Register to B
  - Shifted to A or Shifted to B
  - Off-Line Shifts (A and B Ports in High-Impedance State)
  - Register Clear
- Particularly Suitable for Use in Signature-Analysis Circuitry
- Serial Register Provides:
  - Parallel Storage of Either A or B Input Data
  - Serial Transmission of Data from Either A or B Port
- Dependable Texas Instruments Quality and Reliability

SN54AS877 . . . JT PACKAGE
SN74AS877 . . . NT PACKAGE
SN74AS877 . . . DW PACKAGE
(TOP VIEW)



SN54AS877 . . . FH OR FK PACKAGE
SN74AS877 . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

The 'AS877 features two 8-bit I/O ports (A1-A8 and B1-B8), an 8-bit parallel-load, serial-in, parallel-out shift register, and control logic. With these features, this device is capable of performing eight selectable transceiver or port functions, depending on the state of the three select lines S0, S1, and S2. These functions include: transferring data from port A to port B or vice versa (i.e., the transceiver function), transferring data from the register to either port, serial shifting data to either port, performing off-line shifts (with A and B ports in high-impedance state), and clearing the register. Synchronous parallel loading of the internal register can be accomplished from either port on the positive transition of the clock while serially shifting data in via the SERIN input. The 'AS877 is ideally suited for applications needing signature-analysis circuitry to enhance system verification and/or fault analysis. All serial data is shifted right. All outputs are buffer-type outputs designed specifically to drive bus lines directly and all are 3-state except for Q8, which is a totem-pole output.

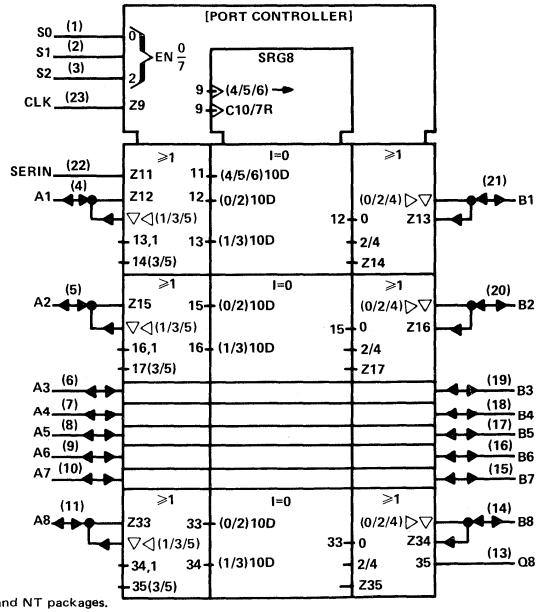
The SN54AS877 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS877 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

MODE S2 S1 S0	CLOCK	SERIN	A1 Q1 B1	A2 Q2 B2	A3 Q3 B3	A4 Q4 B4	A5 Q5 B5	A6 Q6 B6	A7 Q7 B7	A8 Q8 B8	PORT FUNCTION
L L L	H or L	X	Z Q_n A1	Z Q_n A2	Z Q_n A2	Z Q_n A4	Z Q_n A5	Z Q_n A6	Z Q_n A7	Z Q_n A8	A TO B
L L L	↑	X	Z A1 A1	Z A2 A2	Z A3 A3	Z A4 A4	Z A5 A5	Z A6 A6	Z A7 A7	Z A8 A8	
L L H	H or L	X	B1 Q_n Z	B2 Q_n Z	B3 Q_n Z	B4 Q_n Z	B5 Q_n Z	B6 Q_n Z	B7 Q_n Z	B8 Q_n Z	B TO A
L L H	↑	X	B1 B1 Z	B2 B2 Z	B3 B3 Z	B4 B4 Z	B5 B5 Z	B6 B6 Z	B7 B7 Z	B8 B8 Z	
L H L	H or L	X	X Q_n Q1	X Q_n Q2	X Q_n Q3	X Q_n Q4	X Q_n Q5	X Q_n Q6	X Q_n Q7	X Q_n Q8	Q_N TO B_N
L H L	↑	X	Z A1 A1	Z A2 A2	Z A3 A3	Z A4 A4	Z A5 A5	Z A6 A6	Z A7 A7	Z A8 A8	
L H H	H or L	X	Q1 Q_n X	Q2 Q_n X	Q3 Q_n X	Q4 Q_n X	Q5 Q_n X	Q6 Q_n X	Q7 Q_n X	Q8 Q_n X	Q_N TO A_N
L H H	↑	X	B1 B1 Z	B2 B2 Z	B3 B3 Z	B4 B4 Z	B5 B5 Z	B6 B6 Z	B7 B7 Z	B8 B8 Z	
H L L	H or L	X	Z Q_n Q1	Z Q_n Q2	Z Q_n Q3	Z Q_n Q4	Z Q_n Q5	Z Q_n Q6	Z Q_n Q7	Z Q_n Q8	SHIFT
H L L	↑	H	Z H H	Z Q1 Q1	Z Q2 Q2	Z Q3 Q3	Z Q4 Q4	Z Q5 Q5	Z Q6 Q6	Z Q7 Q7	TO
H L L	↑	L	Z L L	Z Q1 Q1	Z Q2 Q2	Z Q3 Q3	Z Q4 Q4	Z Q5 Q5	Z Q6 Q6	Z Q7 Q7	B
H L H	H or L	X	Q1 Q_n Z	Q2 Q_n Z	Q3 Q_n Z	Q4 Q_n Z	Q5 Q_n Z	Q6 Q_n Z	Q7 Q_n Z	Q8 Q_n Z	SHIFT
H L H	↑	H	H H Z	Q1 Q1 Z	Q2 Q2 Z	Q3 Q3 Z	Q4 Q4 Z	Q5 Q5 Z	Q6 Q6 Z	Q7 Q7 Z	TO
H L H	↑	L	L L Z	Q1 Q1 Z	Q2 Q2 Z	Q3 Q3 Z	Q4 Q4 Z	Q5 Q5 Z	Q6 Q6 Z	Q7 Q7 Z	A
H H L	H or L	X	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	
H H L	↑	H	Z H Z	Z Q1 Z	Z Q2 Z	Z Q3 Z	Z Q4 Z	Z Q5 Z	Z Q6 Z	Z Q7 Z	SHIFT
H H L	↑	L	Z L Z	Z Q1 Z	Z Q2 Z	Z Q3 Z	Z Q4 Z	Z Q5 Z	Z Q6 Z	Z Q7 Z	
H H H	H or L	X	Z Q_n Z	Z Qn Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	CLEAR
H H H	↑	X	Z L Z	Z L Z	Z L Z	Z L Z	Z L Z	Z L Z	Z L Z	Z L Z	

n = level of Q_n(n = 1, 2 . . . 8) established on most recent ↑ transition of CLK. Q1 thru Q8 are the shift register outputs; only Q8 is available externally. The double inversions that take place as data travels from port to port are ignored in this table.

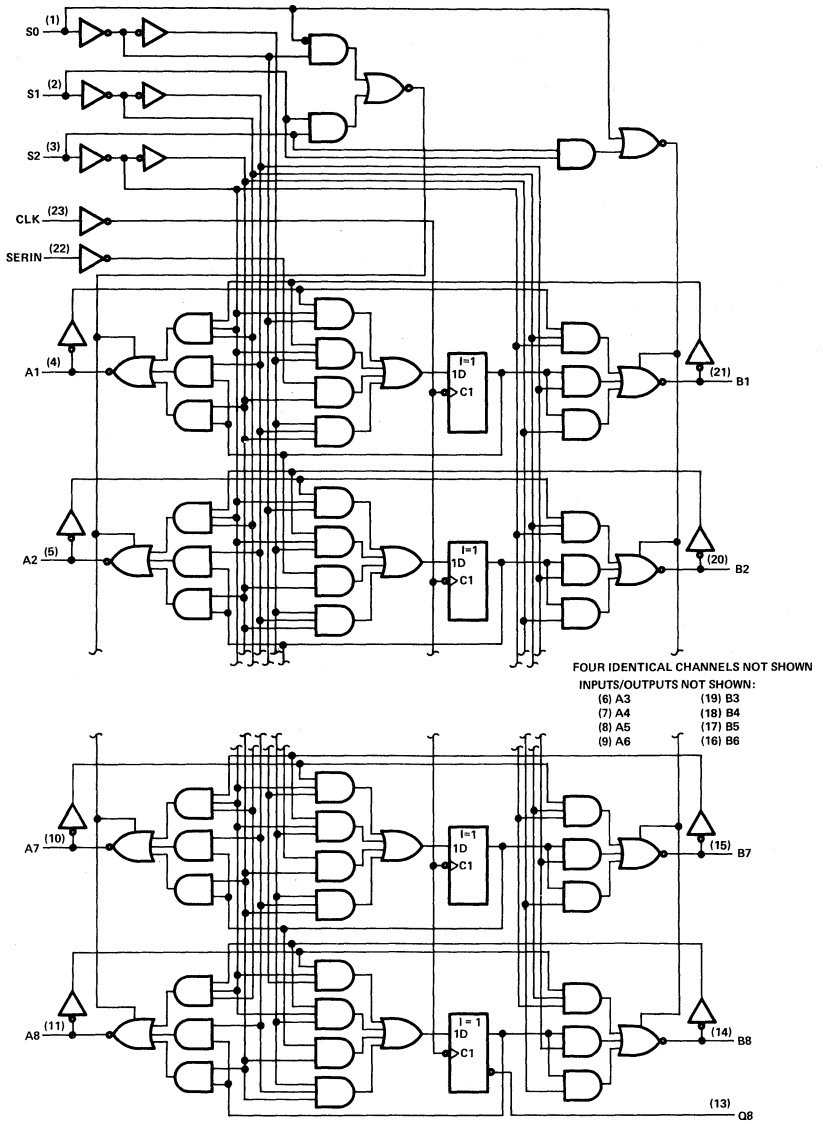
logic symbol



Pin numbers shown are for JT and NT packages.

2

logic diagram (positive logic)



absolute maximum ratings over free-air temperature range

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS877 . . . . . −55°C to 125°C
SN74AS877 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS877			SN74AS877			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	A1-A8, B1-B8			−12			−15	mA
		Q8			−2			−2	
I_{OL}	Low-level output current	A1-A8, B1-B8			32			48	mA
		Q8			20			20	
f_{clock}	Clock frequency		0		45	0		50	MHz
t_w	Duration of clock pulse		11			10			ns
t_{su}	Setup time before CLK↑	A1-A8, B1-B8 SERIN	5.5			5.5			ns
		S0, S1, S2	5.5			5.5			
t_h	Hold time, data after CLK↑	A1-A8, B1-B8 SERIN	0			0			ns
		S0, S1, S2	0			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

Additional information on these products can be obtained from the factory as it becomes available.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS877			SN74AS877			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	A1-A8	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2	3.2					V
	B1-B8	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2	3.3		
	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			
V_{OL}	All outputs except Q8	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
	Q8	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	
I_I	S0, S1, S2	V_{CC} = 5.5 V,	V_I = 7 V			0.3			0.3	mA
	CLK and SERIN					0.1			0.1	
	A1-A8, B1-B8	V_{CC} = 5.5 V,	V_I = 5.5 V			0.2			0.2	
I_{IH}	S0, S1, S2	V_{CC} = 5.5 V,	V_I = 2.7 V			60			60	µA
	CLK and SERIN					20			20	
	A1-A8, B1-B8‡					70			70	
I_{IL}	S0, S1, S2	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	CLK and SERIN					−0.5			−0.5	
	A1-A8, B1-B8‡					−0.75			−0.75	
I_O§	Except Q8	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
	Q8			−20		−112	−20		−112	
I_{CC}		V_{CC} = 5.5 V			136	220		136	220	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the output currents I_{OZH} and I_{OZL}, respectively.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

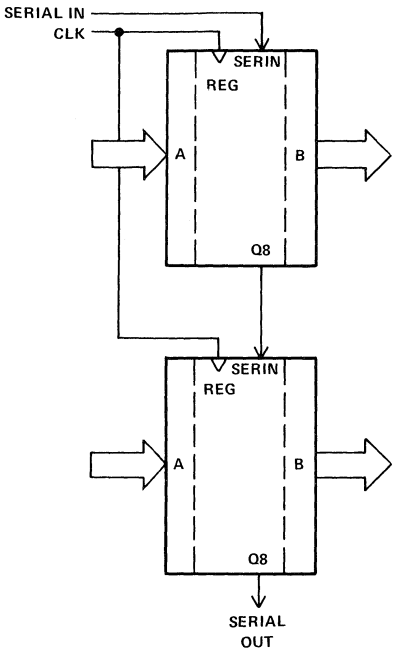
switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS877		SN74AS877		
			MIN	MAX	MIN	MAX	
f_{max}			45		50		MHz
t_{PLH}	Any A port	Any B port	2	8.5	2	7	ns
t_{PHL}			3	10.5	3	9	
t_{PLH}	Any B port	Any A port	2	9	2	7.5	ns
t_{PHL}			3	10.5	3	9	
t_{PLH}	S0, S1, S2	Any A or B port	3	11.5	3	10	ns
t_{PHL}			2	9.5	2	8	
t_{PLH}	CLK	Any A or B port	2	11	2	9	ns
t_{PHL}			3	13	3	11.5	
t_{PLH}	CLK	Q8	2	10.5	2	8	ns
t_{PHL}			3	10	3	8.5	
t_{PHZ}	S0, S1, S2	Any A or B port	2	7.5	2	6.5	ns
t_{PLZ}			3	13	3	10.5	
t_{PZH}			2	9	2	7	ns
t_{PZL}			3	11.5	3	9.5	

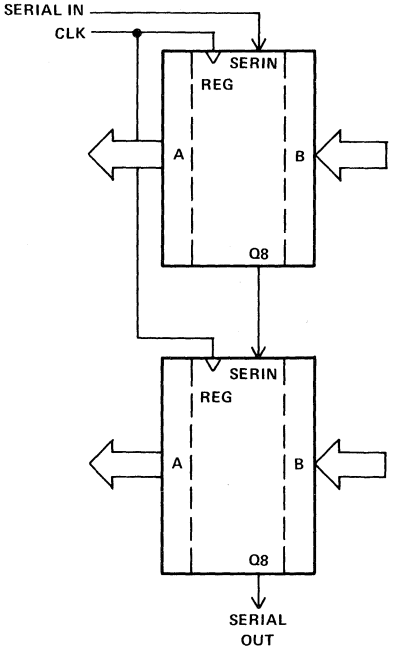
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TYPICAL APPLICATION DATA

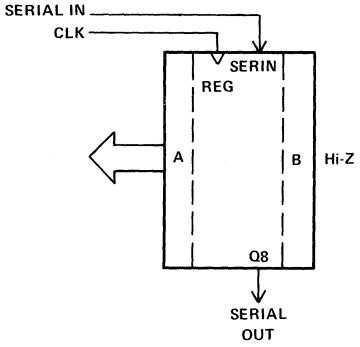
BUS A TO BUS B OR
SERIAL TRANSMISSION



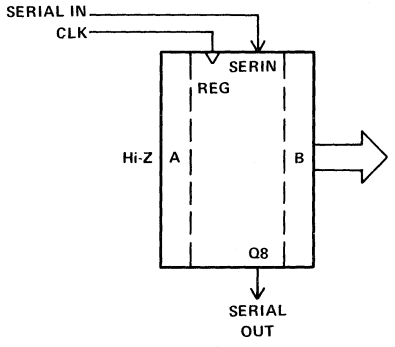
BUS B TO BUS A OR
SERIAL TRANSMISSION



SERIAL IN TO A PORT

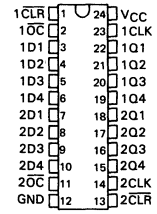


SERIAL IN TO B PORT

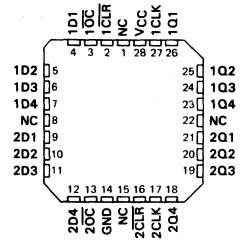


- **3-State Bus-Driving Outputs**
- **Full Parallel-Access for Loading**
- **Buffered Control Inputs**
- **Choice of True or Inverting Logic**
  - **'ALS878, 'AS878 True Outputs**
  - **'ALS879, 'AS879 Inverting Outputs**
- **Synchronous Clear**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

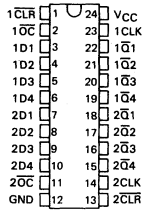
SN54ALS878, SN54AS878 . . . JT PACKAGE
SN74ALS878, SN74AS878 . . . NT PACKAGE
SN74ALS878, SN74AS878 . . . DW PACKAGE
(TOP VIEW)



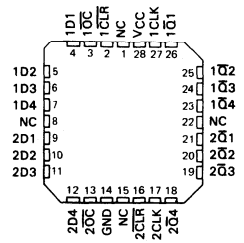
SN54ALS878, SN54AS878 . . . FH OR FK PACKAGE
SN74ALS878, SN74AS878 . . . FN PACKAGE
(TOP VIEW)



SN54ALS879, SN54AS879 . . . JT PACKAGE
SN74ALS879, SN74AS879 . . . NT PACKAGE
SN74ALS879, SN74AS879 . . . DW PACKAGE
(TOP VIEW)



SN54ALS879, SN54AS879 . . . FH OR FK PACKAGE
SN74ALS879, SN74AS879 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

These dual 4-bit registers feature three-state outputs designed specifically for bus driving. This makes these devices particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The dual 4-bit edge-triggered flip-flops enter data on the low-to-high transition of the clock (1CLK and 2CLK). All types have individual synchronous clear inputs and output control pins for each group of 4-bit registers.

The SN54ALS878, SN54ALS879, SN54AS878, and SN54AS879 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS878, SN74ALS879, SN74AS878, and SN74AS879 are characterized for operation from 0°C to 70°C.

FUNCTION TABLES

'ALS878, 'AS878
(EACH FLIP-FLOP)

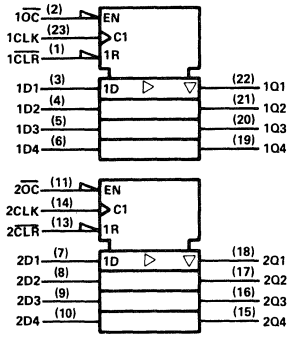
INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	CLK	D	Q
L	L	↑	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	Q_0
H	X	X	X	Z

'ALS879, 'AS879
(EACH FLIP-FLOP)

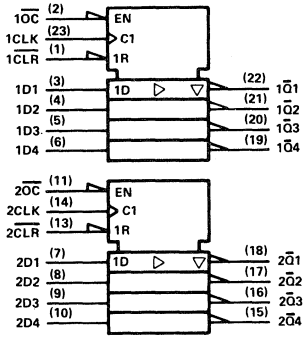
INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	CLK	D	$\overline{Q}$
L	L	↑	X	H
L	H	↑	H	L
L	H	↑	L	H
L	H	L	X	Q_0
H	X	X	X	Z

logic symbols

'ALS878, 'AS878

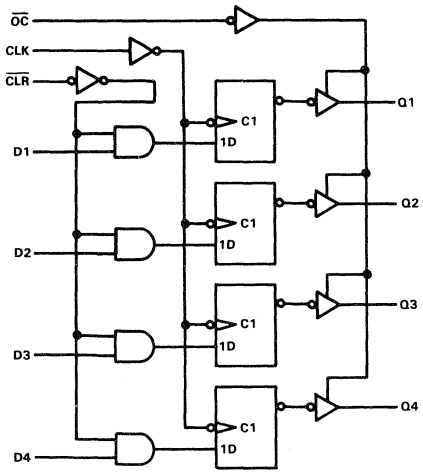


'ALS879, 'AS879

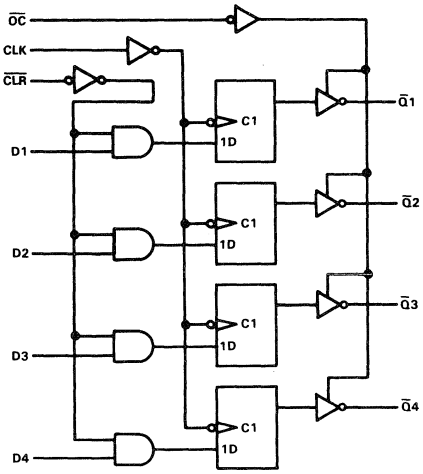


logic diagrams (positive logic)

'ALS878, 'AS878 (EACH QUAD FLIP-FLOP)



'ALS879, 'AS879 (EACH QUAD FLIP-FLOP)



Pin numbers shown are for JT and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS878, SN54ALS879 . . . . . −55°C to 125°C
SN74ALS878, SN74ALS879 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS878 SN54ALS879			SN74ALS878 SN74ALS879			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency	'ALS878	0		25	0		30	MHz
		'ALS879	0		20	0		25	
t_w	Pulse duration	'ALS878 CLK high or low	20			16.5			ns
		'ALS879 CLK high or low	25			20			
t_{su}	Setup time before CLK↑	Data	15			15			ns
		$\overline{CLR}$	20			20			
t_h	Hold time after CLK↑	Data	4			4			ns
		$\overline{CLR}$	0			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS878 SN54ALS879			SN74ALS878 SN74ALS879			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		14	21		14	21	mA
		Outputs low		18	29		18	29	
		Outputs disabled		20	31		20	31	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

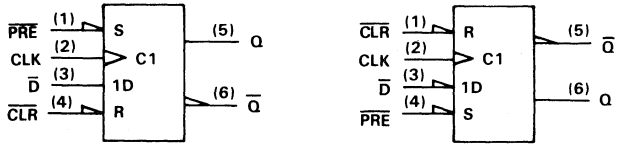
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS878 SN54ALS879		SN74ALS878 SN74ALS879		
			MIN	MAX	MIN	MAX	
f_{max}	'ALS878		25		30		MHz
	'ALS879		20		25		
t_{PLH}	CLK	Q ('ALS878) or $\overline{Q}$ ('ALS879)	4	15	4	14	ns
t_{PHL}			4	17	4	16	
t_{PZH}	$\overline{OC}$	Q ('ALS878) or $\overline{Q}$ ('ALS879)	4	22	4	20	ns
t_{PZL}			4	22	4	20	
t_{PHZ}	$\overline{OC}$	Q ('ALS878) or $\overline{Q}$ ('ALS879)	2	12	2	10	ns
t_{PLZ}			3	16	3	13	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D flip-flop signal conventions

It is TI practice to name the outputs and other inputs of a D-type flip-flop and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active low.

In some applications it may be advantageous to redesignate the data input $\overline{D}$. In that case all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.



Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (▷) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 ($\overline{Q}$) is still in phase with the data input $\overline{D}$, but now both are considered active-low.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS878, SN54AS879 . . . . . −55 °C to 125 °C
SN74AS878, SN74AS879 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54AS878 SN54AS879			SN74AS878 SN74AS879			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				32			48	mA
f_{clock}	Clock frequency		0		100	0		125	MHz
t_w	Pulse duration	CLK low	3			2			ns
		CLK high	5			4			
t_{su}	Setup time before CLK↑	Data	3			2			ns
		$\overline{CLR}$	6.5			5.5			
t_h	Hold time after CLK↑	Data	3			2			ns
		$\overline{CLR}$	0			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS878 SN54AS879			SN74AS878 SN74AS879			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.29	0.5				V
		V_{CC} = 4.5 V	I_{OL} = 48 mA					0.33	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	D	V_{CC} = 5.5 V,	V_I = 0.4 V			−3			−2	mA
	All other					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS878	V_{CC} = 5.5 V, See Note 1	Outputs high		82	132		82	132	mA
			Outputs low		96	155		96	155	
			Outputs disabled		100	160		100	160	
	'AS879		Outputs high		88	142		88	142	
			Outputs low		94	150		94	150	
			Outputs disabled		100	160		100	160	

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with CLR and all D inputs grounded, and CLK and OC at 4.5 V.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS878 SN54AS879		SN74AS878 SN74AS879		
			MIN	MAX	MIN	MAX	
f_{max}			100		125		MHz
t_{PLH}	CLK	Q ('AS878) or $\overline{Q}$ ('AS879)	3	11.5	3	8.5	ns
t_{PHL}			4	12.5	4	10.5	
t_{PZH}	$\overline{OC}$	Q ('AS878) or $\overline{Q}$ ('AS879)	2	8	2	7	ns
t_{PZL}			3	11.5	3	10.5	
t_{PHZ}	$\overline{OC}$	Q ('AS878) or $\overline{Q}$ ('AS879)	2	7	2	6	ns
t_{PLZ}			2	7	2	6	

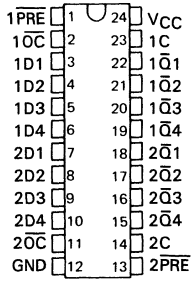
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TYPES SN54ALS880, SN54AS880, SN74ALS880, SN74AS880
DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

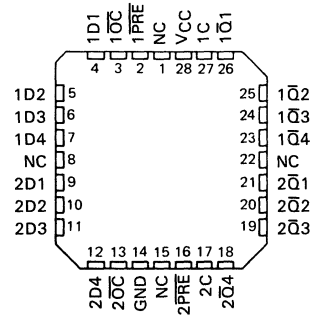
D2661, DECEMBER 1982—REVISED DECEMBER 1983

- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **'ALS873 Is Alternative Version with Noninverting Outputs**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS880, SN54AS880 . . . JT PACKAGE
SN74ALS880, SN74AS880 . . . NT PACKAGE
SN74ALS880, SN74AS880 . . . DW PACKAGE
(TOP VIEW)



SN54ALS880, SN54AS880 . . . FH OR FK PACKAGE
SN74ALS880, SN74AS880 . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

These dual 4-bit registers feature three-state outputs designed specifically for bus driving. This makes these devices particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

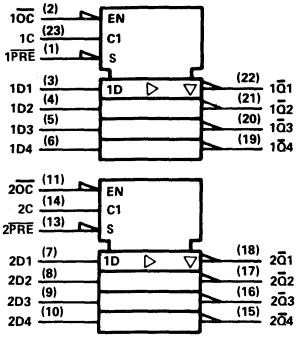
The dual 4-bit latches are transparent D-type. While the latch enable input (1C or 2C) is high, the $\overline{Q}$ outputs will follow the data (D) inputs in inverted form, according to the function table. When the latch enable input is taken low, the outputs will be latched. When $\overline{PRE}$ goes low, the $\overline{Q}$ outputs go low independently of the clock. The outputs are in a high-impedance state when $\overline{OC}$ (output control) is at a high logic level.

The SN54ALS880 and SN54AS880 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS880 and SN74AS880 are characterized for operation from 0 °C to 70 °C.

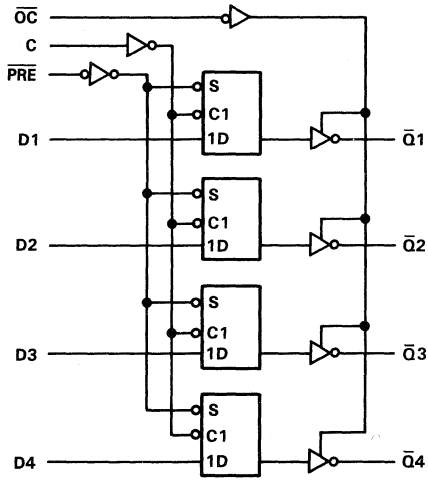
FUNCTION TABLES (EACH LATCH)

INPUTS				OUTPUT
$\overline{OC}$	$\overline{PRE}$	ENABLE C	D	$\overline{Q}$
L	L	X	X	L
L	H	H	H	L
L	H	H	L	H
L	H	L	X	$\overline{Q}_0$
H	X	X	X	Z

logic symbol



logic diagram (each quad latch, positive logic)



Pin numbers shown are for JT and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS880, SN54AS880 . . . . . −55 °C to 125 °C
SN74ALS880, SN74AS880 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54ALS880			SN74ALS880			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
t_w	Pulse duration	$\overline{PRE}$ low	15			15			ns
		Enable C high	15			15			
t_{su}	Setup time, data before enable C↓		10			10			ns
t_h	Hold time, data after enable C↓		10			10			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS880			SN74ALS880			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		14	21		14	21	mA
		Outputs low		19	29		19	29	
		Outputs disabled		20	31		20	31	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

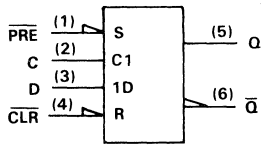
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS880		SN74ALS880		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$	3	23	3	20	ns
t_{PHL}			3	15	3	14	
t_{PLH}	C	$\overline{Q}$	8	31	8	24	ns
t_{PHL}			8	22	8	21	
t_{PHL}	$\overline{PRE}$	$\overline{Q}$	6	24	6	21	ns
t_{PZH}	$\overline{OC}$	$\overline{Q}$	4	21	5	18	ns
t_{PZL}			4	21	5	18	
t_{PHZ}	$\overline{OC}$	$\overline{Q}$	2	10	2	8	ns
t_{PLZ}			3	15	3	13	

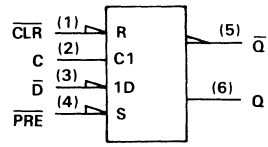
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D latch signal conventions

It is TI practice to name the outputs and other inputs of a D-type latch and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active low.

In some applications it may be advantageous to redesignate the data input $\overline{D}$. In that case all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.





Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (▷) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 ($\overline{Q}$) is still in phase with the data input $\overline{D}$, but now both are considered active-low.

recommended operating conditions

			SN54AS880			SN74AS880			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				32			48	mA
t_w	Pulse duration	$\overline{PRE}$ low	4.5			3.5			ns
		Enable C high	3.5			2.5			
t_{su}	Setup time, data before enable C↓		2			2			ns
t_h	Hold time, data after enable C↓		1			1			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS880			SN74AS880			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.30	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		73	118		73	118	mA
		Outputs low		76	122		76	122	
		Outputs disabled		86	137		86	137	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

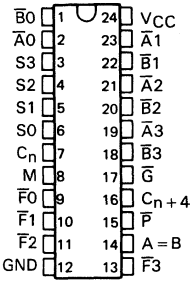
'ALS465 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS880		SN74AS880		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$	4	11	4	9.5	ns
t_{PHL}			4	9	4	8.5	
t_{PLH}	C	$\overline{Q}$	6	14	6	11.5	ns
t_{PHL}			4	10	4	8	
t_{PHL}	$\overline{PRE}$	$\overline{Q}$	4	11.5	4	10	ns
t_{PZH}	$\overline{OC}$	$\overline{Q}$	2	8	2	7.5	ns
t_{PZL}			4	11	4	10	
t_{PHZ}	$\overline{OC}$	$\overline{Q}$	2	8	2	6.5	ns
t_{PLZ}			2	9	2	8	

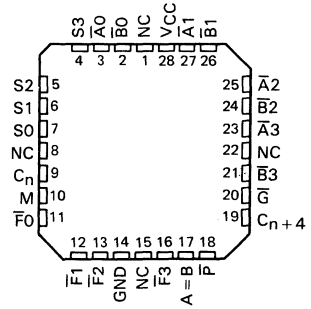
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- The 'AS881A is Offered in 300-mil DIPS and is Available in Small Outline (SO) and Plastic and Ceramic Chip Carriers
- Full Look-Ahead for High-Speed Operations on Long Words
- Arithmetic Operating Modes:
  - Addition
  - Subtraction
  - Shift Operand A One Position
  - Magnitude Comparison
  - Plus Twelve Other Arithmetic Operations
- Logic Function Modes
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
  - 'AS881A Provides Status Register Checks
  - Plus Ten Other Logic Operations
- Dependable Texas Instruments Quality and Reliability

SN54AS181A . . . J OR JT PACKAGE
SN54AS881A . . . JT PACKAGE
SN74AS181A . . . N OR NT OR DW PACKAGE
SN74AS881A . . . NT OR DW PACKAGE
(TOP VIEW)

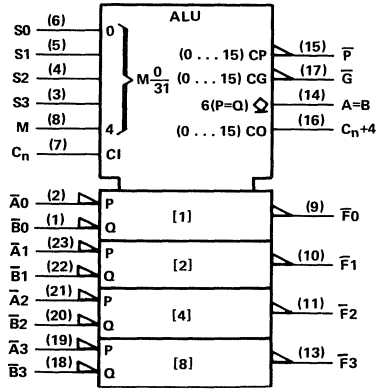


SN54AS181A, SN54AS881A . . . FH OR FK PACKAGE
SN74AS181A, SN74AS881A . . . FN PACKAGE
'AS181A, 'AS881A
(TOP VIEW)



NC—No internal connection

logic symbol

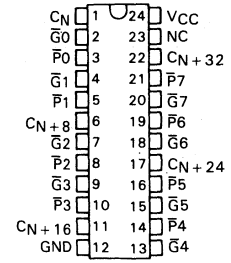


Pin numbers shown are J, JT, N and NT packages.

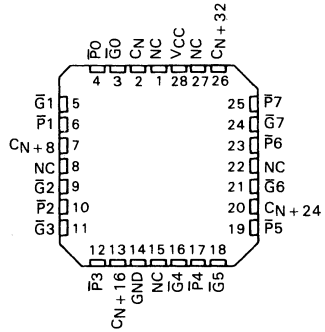
For complete information on the SN54AS881A and the SN74AS881A, see page 2-175.

- **Directly Compatible with the New 'AS181A and 'AS881A ALU's**
- **Included among the Package Options Are Compact, 24-Pin, 300-mil-Wide DIPs and Small Outline (SO) and 28-Pin Plastic and Ceramic Chip Carriers**
- **Capable of Anticipating the Carry Across a Group of Eight 4-Bit Binary Adders**
- **Cascadable to Perform Look-Ahead Across n-Bit Adders**
- **Typical Carry Time, C_n to Any C_{n+i}, Is Less Than 6 ns (C_L = 15 pF)**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS882 . . . JT PACKAGE
SN74AS882 . . . NT PACKAGE
SN74AS882 . . . DW PACKAGE
(TOP VIEW)



SN54AS882 . . . FH OR FK PACKAGE
SN74AS882 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'AS882 is a high-speed look-ahead carry generator capable of anticipating the carry across a group of eight 4-bit adders permitting the designer to implement look-ahead for a 32-bit ALU with a single package or, by cascading 'AS882's, full look-ahead is possible across n-bit adders.

The SN54AS882 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS882 is characterized for operation from 0°C to 70°C.

'AS882 LOGIC EQUATIONS

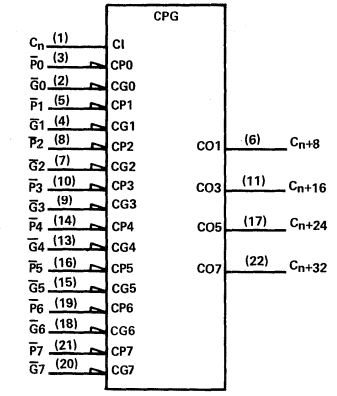
$$C_{n+8} = G1 + P1G0 + P1P0C_n$$

$$C_{n+16} = G3 + P3G2 + P3P2G1 + P3P2P1G0 + P3P2P1P0C_n$$

$$C_{n+24} = G5 + P5G4 + P5P4G3 + P5P4P3G2 + P5P4P3P2G1 + P5P4P3P2P1G0 + P5P4P3P2P1P0C_n$$

$$C_{n+32} = G7 + P7G6 + P7P6G5 + P7P6P5G4 + P7P6P5P4G3 + P7P6P5P4P3G2 + P7P6P5P4P3P2G1 + P7P6P5P4P3P2P1G0 + P7P6P5P4P3P2P1P0C_n$$

logic symbol



Pin numbers shown are for JT and NT packages.

ADVANCE INFORMATION

This document contains information on a new product. Specifications are subject to change without notice.

FUNCTION TABLE
FOR C_{n+32} OUTPUT

INPUTS																OUTPUT
$\overline{G}7$	$\overline{G}6$	$\overline{G}5$	$\overline{G}4$	$\overline{G}3$	$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}7$	$\overline{P}6$	$\overline{P}5$	$\overline{P}4$	$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	C_n	C_{n+32}
L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	L	L	X	X	X	X	X	X	X	H
X	X	X	L	X	X	X	X	L	L	L	X	X	X	X	X	X	H
X	X	X	X	L	X	X	X	L	L	L	L	X	X	X	X	X	H
X	X	X	X	X	L	X	X	L	L	L	L	L	X	X	X	X	H
X	X	X	X	X	X	L	X	L	L	L	L	L	L	X	X	X	H
X	X	X	X	X	X	X	L	L	L	L	L	L	L	L	X	X	H
X	X	X	X	X	X	X	X	L	L	L	L	L	L	L	L	H	H
All other combinations																	L

FUNCTION TABLE
FOR C_{n+24} OUTPUT

INPUTS													OUTPUT
$\overline{G}5$	$\overline{G}4$	$\overline{G}3$	$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}5$	$\overline{P}4$	$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	C_n	C_{n+24}
L	X	X	X	X	X	X	X	X	X	X	X	X	H
X	L	X	X	X	X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	L	L	X	X	X	X	X	H
X	X	X	L	X	X	L	L	L	X	X	X	X	H
X	X	X	X	L	X	L	L	L	L	X	X	X	H
X	X	X	X	X	L	L	L	L	L	L	X	X	H
X	X	X	X	X	X	L	L	L	L	L	L	H	H
All other combinations													L

FUNCTION TABLE
FOR C_{n+16} OUTPUT

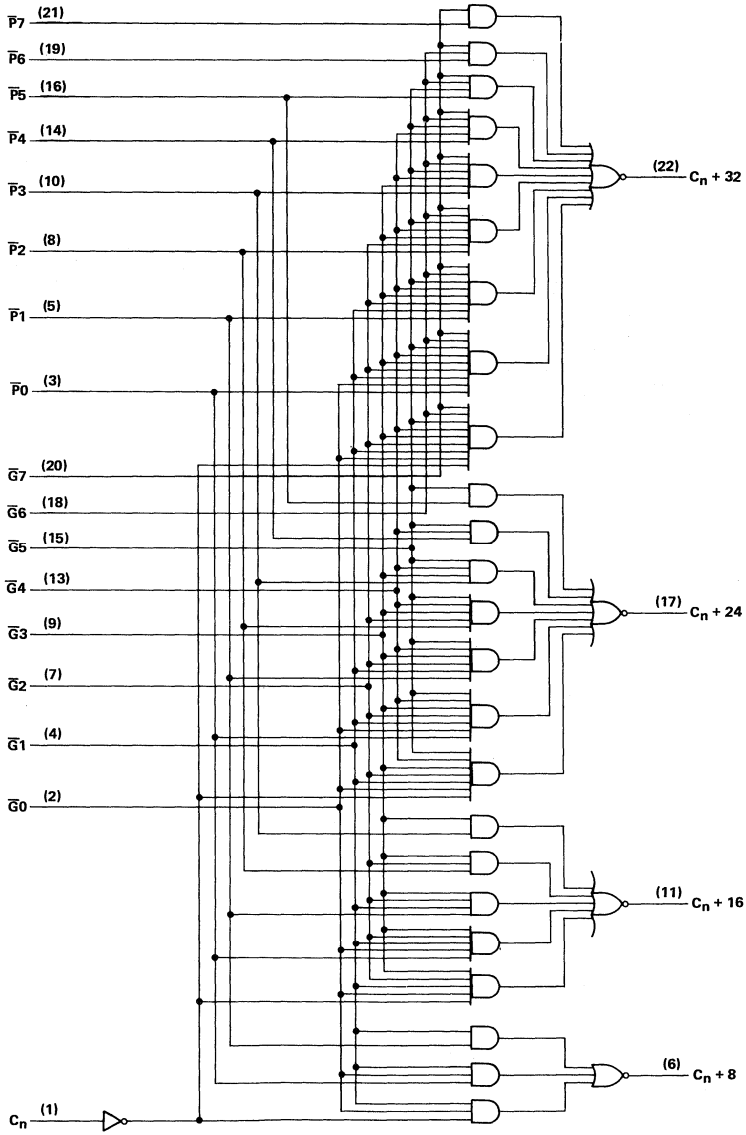
INPUTS									OUTPUT
$\overline{G}3$	$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	C_n	C_{n+16}
L	X	X	X	X	X	X	X	X	H
X	L	X	X	L	X	X	X	X	H
X	X	L	X	L	L	X	X	X	H
X	X	X	L	L	L	L	X	X	H
X	X	X	X	L	L	L	L	H	H
All other combinations									L

FUNCTION TABLE
FOR C_{n+8} OUTPUT

INPUTS					OUTPUT
$\overline{G}1$	$\overline{G}0$	$\overline{P}1$	$\overline{P}0$	C_n	C_{n+8}
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

Any inputs not shown in a given table are irrelevant with respect to that output.

logic diagram (positive logic)



Pin numbers shown are for JT and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS882 . . . . . −55 °C to 125 °C
SN74AS882 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS882			SN74AS882			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS882			SN74AS882			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V, to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I	C_n	V_{CC} = 5.5 V,	V_I = 7 V			0.5			0.5	mA
	$\overline{G}0$, $\overline{G}6$					4			4	
	$\overline{G}1$, $\overline{G}2$, $\overline{G}4$					6			6	
	$\overline{G}3$					7.5			7.5	
	$\overline{G}5$					7			7	
	$\overline{G}7$					4.5			4.5	
	$\overline{P}0$, $\overline{P}1$					2			2	
	$\overline{P}2$, $\overline{P}3$					1.5			1.5	
	$\overline{P}4$, $\overline{P}5$					1			1	
	$\overline{P}6$, $\overline{P}7$					0.5			0.5	
I_{IH}	C_n	V_{CC} = 5.5 V,	V_I = 2.7 V			0.2			0.2	mA
	$\overline{G}0$, $\overline{G}6$					1.6			1.6	
	$\overline{G}1$, $\overline{G}2$, $\overline{G}4$					2.4			2.4	
	$\overline{G}3$					3			3	
	$\overline{G}5$					2.8			2.8	
	$\overline{G}7$					1.8			1.8	
	$\overline{P}0$, $\overline{P}1$					0.8			0.8	
	$\overline{P}2$, $\overline{P}3$					0.6			0.6	
	$\overline{P}4$, $\overline{P}5$					0.4			0.4	
	$\overline{P}6$, $\overline{P}7$					0.2			0.2	
I_{IL}	C_n	V_{CC} = 5.5 V,	V_I = 0.4 V			−3			−3	mA
	$\overline{G}0$					−26			−26	
	$\overline{G}1$					−37			−37	
	$\overline{G}2$					−40			−40	
	$\overline{G}3$					−47			−47	
	$\overline{G}4$					−41			−41	
	$\overline{G}5$					−44			−44	
	$\overline{G}6$, $\overline{G}7$					−28			−28	
	$\overline{P}0$					−13			−13	
	$\overline{P}1$					−11			−11	
	$\overline{P}2$					−9			−9	
	$\overline{P}3$					−8			−8	
	$\overline{P}4$					−5			−5	
	$\overline{P}5$					−4			−4	
	$\overline{P}6$, $\overline{P}7$					−2			−2	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−150			−150			mA
I_{CC}		V_{CC} = 5.5 V			72	105		72	105	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit, I_{OS}.

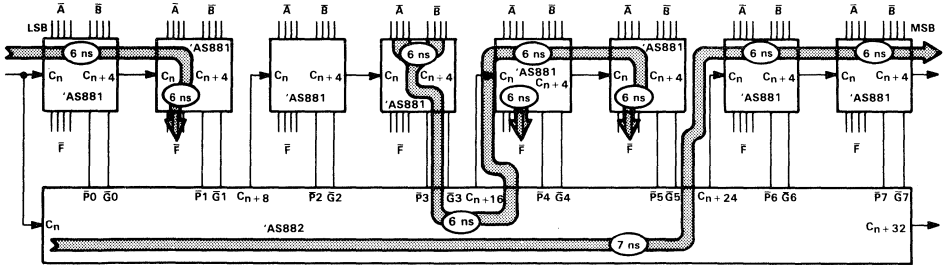
switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS822		SN74AS882		
			MIN	MAX	MIN	MAX	
t_{pd}	C_n	Any output	4	15	4	14	ns
t_{pd}	$\overline{P}$ or $\overline{G}$	C_n + 8	2	9	2	8	
t_{pd}	$\overline{P}$ or $\overline{G}$	C_n + 16	2	9	2	8	
t_{pd}	$\overline{P}$ or $\overline{G}$	C_n + 24	2	11	2	10	
t_{pd}	$\overline{P}$ or $\overline{G}$	C_n + 32	2	13	2	12	

t_{pd} = t_{PHL} or t_{PLH}.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

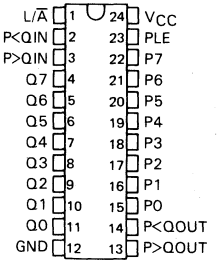
TYPICAL APPLICATION DATA

The application given in figure 1 illustrates how the 'AS882 can implement look-ahead carry for a 32-bit ALU (in this case, the popular 'AS881) with a single package. Typical carry times shown are derived using the standard Advanced Schottky load circuit with C_L = 15 pF.

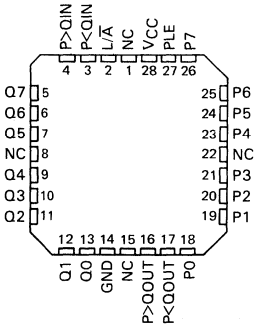


- **Included among the Package Options Are Compact, 24-Pin, 300-mil DIPs and Small Outline (SO) and 28-Pin Ceramic and Plastic Chip Carriers**
- **Latchable P Input Ports with Power-Up Clear**
- **Choice of Logical or Arithmetic (2's Complement) Comparison**
- **Data and PLE Inputs Utilize P-N-P Input Transistors to Reduce DC Loading Effects**
- **Approximately 35% Improvement in AC Performance Over Schottky TTL while Performing More Functions**
- **Cascadable to n-Bits while Maintaining High Performance**
- **10% Less Power than STTL for an 8-Bit Comparison**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS885 . . . JT PACKAGE
SN74AS885 . . . NT PACKAGE
SN74AS885 . . . DW PACKAGE
(TOP VIEW)



SN54AS885 . . . FH OR FK PACKAGE
SN74AS885 . . . FN PACKAGE
(TOP VIEW)



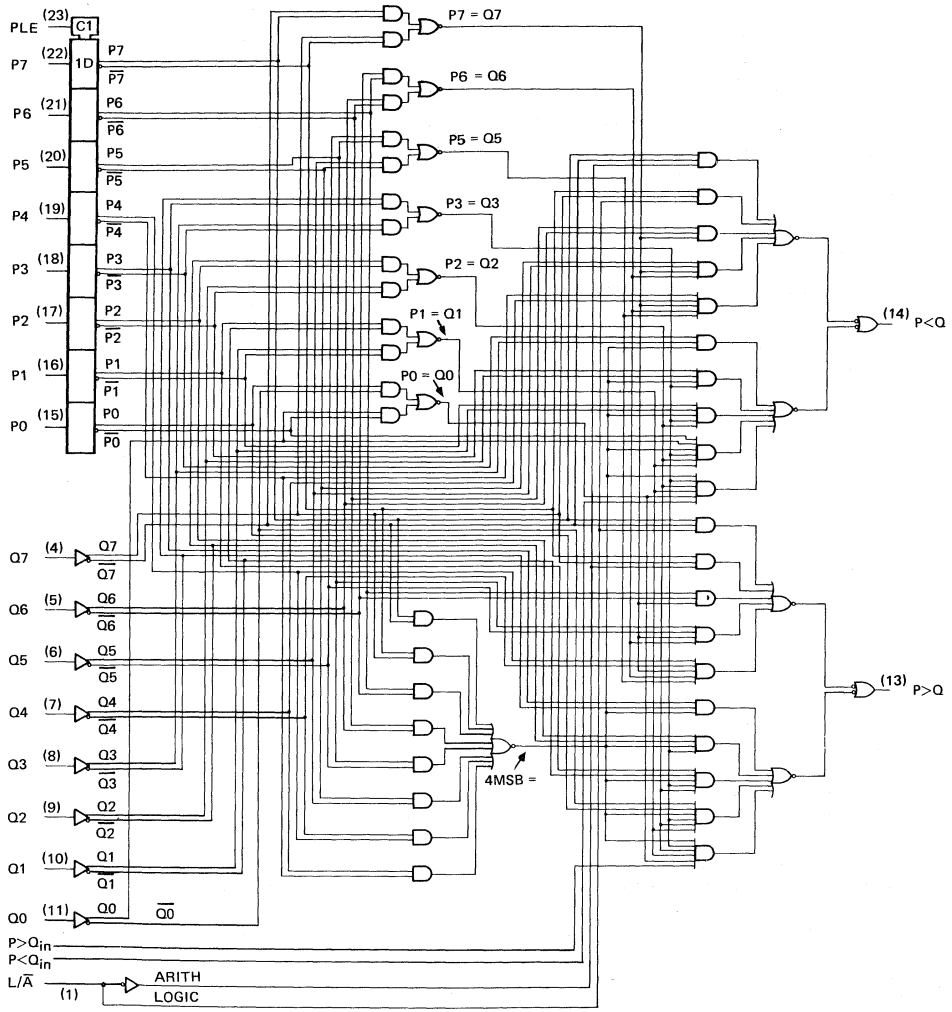
description

These advanced Schottky devices are capable of performing high-speed arithmetic or logic comparisons on two 8-bit binary or two's complement words. Two fully decoded decisions about words P and Q are externally available at two outputs. These devices are fully expandable to any number of bits without external gates. The P > Q and P < Q outputs of a stage handling less-significant bits may be connected to the P > Q and P < Q inputs of the next stage handling more-significant bits to obtain comparisons of words of longer lengths. The cascading paths are implemented with only a two-gate-level delay to reduce overall comparison times for long words. Two alternative methods of cascading are shown in the typical application data.

The latch is transparent when P Latch Enable (PLE) is high; the P input port is latched when PLE is low. This provides the designer with temporary storage for the P data word. The enable circuitry is implemented with minimal delay times to enhance performance when cascaded for longer words. The PLE and P and Q data inputs utilize p-n-p input transistors to reduce the low-level current input requirement to typically −0.25 mA, which minimizes dc loading effects.

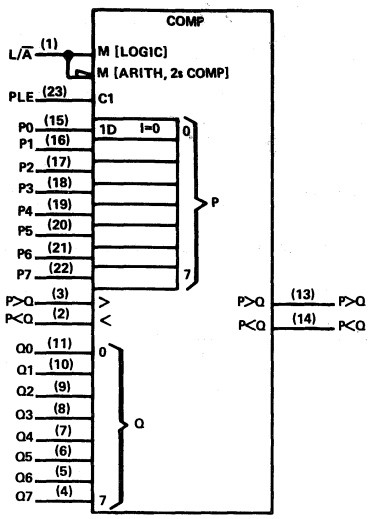
The SN54AS885 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS885 is characterized for operation from 0°C to 70°C.

logic diagram (positive logic)



Pin numbers shown are for JT and NT packages.

logic symbol



Pin numbers shown are for JT and NT packages.

FUNCTION TABLE

COMPARISON	L/$\overline{A}$	DATA INPUTS P0-P7, Q0-Q7	INPUT P>Q	INPUT P<Q	OUTPUTS P>Q	OUTPUTS P<Q
LOGICAL	H	P>Q	X	X	H	L
LOGICAL	H	P<Q	X	X	L	H
LOGICAL*	H	P=Q	H OR L	H OR L	H OR L	H OR L
ARITHMETIC	L	P AG Q	X	X	H	L
ARITHMETIC	L	Q AG P	X	X	L	H
ARITHMETIC*	L	P=Q	H OR L	H OR L	H OR L	H OR L

*In these cases the P>Q output will follow the P>Q input, and the P<Q output will follow the P<Q input.
AG — arithmetically greater than

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS885 . . . . . −55°C to 125°C
SN74AS885 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

PARAMETER		SN54AS885			SN74AS885			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
t_{su}	Setup time to PLE ↓	2			2			ns
t_h	Hold time after PLE ↓	4			4			
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS885			SN74AS885			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	μA
I_{IH}	$L/\overline{A}$	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	Others					20			20	
I_{IL}	$L/\overline{A}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−4			−4	mA
	P > Q_{in} P < Q_{in}					−2			−2	
	P, Q, PLE					−1			−1	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−20		−112	−20		−112	mA
I_{CC}		V_{CC} = 5.5 V	See Note 1		130	210		130	210	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with all inputs high except $L/\overline{A}$, which is low.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS885			SN74AS885			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	L/A	P < Q, P > Q		8.5	14		8.5	13	ns
t_{PHL}				7.5	14		7.5	13	
t_{PLH}	P < Q_{in} P > Q_{in}			5	10		5	8	ns
t_{PHL}				5.5	10		5.5	8	
t_{PLH}	Any P or Q Data Input			13.5	21		13.5	17.5	ns
t_{PHL}				10	17		10	15	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TYPICAL APPLICATION DATA

The 'AS885 can be cascaded to compare words longer than 8-bits. Figure 1 shows the comparison of two 32-bit words; however, the design is expandable to n-bits. Figure 1 shows the optimum cascading arrangement for comparing words of 32 bits or greater. Typical delay times shown are at V_{CC} = 5 V, T_A = 25°C, and use the standard Advanced Schottky load of R_L = 500 Ω, C_L = 50 pF.

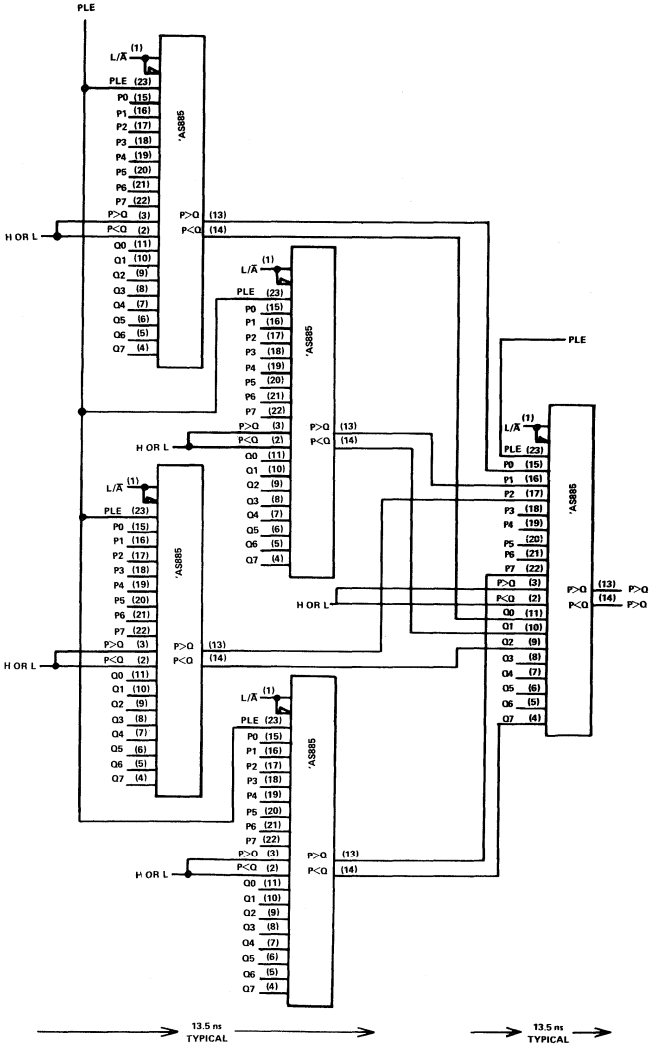


FIGURE 1 – 32-BIT TO 72 (N)-BIT MAGNITUDE COMPARATOR

TYPICAL APPLICATION DATA

The method shown in Figure 2 is the fastest cascading arrangement for comparing 16-bit or 24-bit words. Typical delay times shown are at V_{CC} = 5 V, T_A = 25°C, and use the standard Advanced Schottky load of R_L = 500 Ω, C_L = 50 pF.

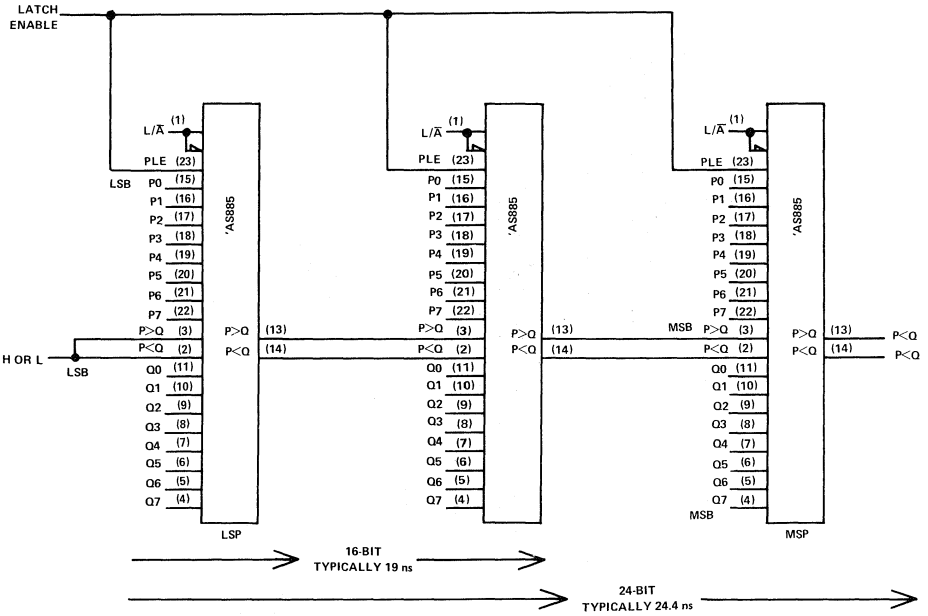


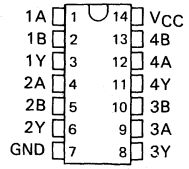
FIGURE 2

TYPES SN54ALS1000A, SN54AS1000, SN74ALS1000A, SN74AS1000
QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS/DRIVERS

D2661, APRIL 1982—REVISED DECEMBER 1983

- **'ALS1000A is a Buffer Version of 'ALS00A**
- **'AS1000 is a Driver Version of 'AS00**
- **'AS1000 Offers High Capacitive Drive Capability**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS1000A, SN54AS1000 . . . J PACKAGE
SN74ALS1000A, SN74AS1000 . . . N PACKAGE
SN74ALS1000A, SN74AS1000 . . . D PACKAGE
(TOP VIEW)



2

description

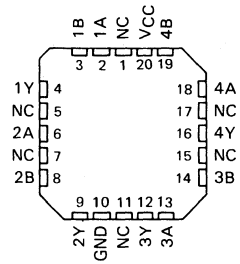
These devices contain four independent 2-input NAND buffers/drivers. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54ALS1000A and SN54AS1000 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1000A and SN74AS1000 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

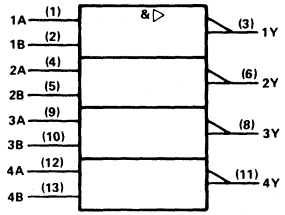
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

SN54ALS1000A, SN54AS1000 . . . FH OR FK PACKAGE
SN74ALS1000A, SN74AS1000 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1000A . . . . . −55 °C to 125 °C
SN74ALS1000A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS1000A			SN74ALS1000A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1000A			SN74ALS1000A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.86	1.6		0.86	1.6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		4.8	7.8		4.8	7.8	mA

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1000A		SN74ALS1000A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2	10	2	8	ns
t_{PHL}			2	10	2	7	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS1000 . . . . . −55 °C to 125 °C
SN74AS1000 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS1000			SN74AS1000			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS1000			SN74AS1000			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V		−135			−135		mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		2.1	3.5		2.1	3.5	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		11.5	19		11.5	19	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS1000		SN74AS1000		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	4.5	1	3.5	ns
t_{PHL}			1	4.5	1	3.5	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D2661, DECEMBER 1983—REVISED DECEMBER 1983

- **Quad Versions of 'ALS805**
- **Buffer Version of 'ALS02**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

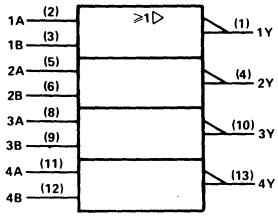
These devices contain four independent 2-input NOR buffers. They perform the Boolean functions $Y = \overline{A+B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The SN54ALS1002A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1002A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

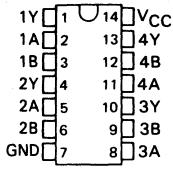
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol

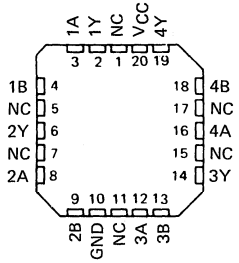


Pin numbers shown are for J and N packages.

SN54ALS1002A . . . J PACKAGE
SN74ALS1002A . . . N PACKAGE
SN74ALS1002A . . . D PACKAGE
(TOP VIEW)



SN54ALS1002A . . . FH OR FK PACKAGE
SN74ALS1002A . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1002A . . . . . −55 °C to 125 °C
SN74ALS1002A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS1002A			SN74ALS1002A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1002A			SN74ALS1002A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		1.7	2.8		1.7	2.8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		5.6	9		5.6	9	mA

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1002A		SN74ALS1002A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2	10	2	8	ns
t_{PHL}			2	10	2	7	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- **Buffer Version of 'ALS03A**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

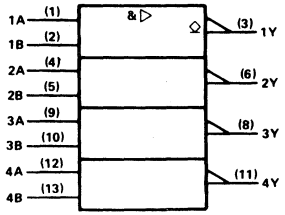
These devices contain four independent 2-input NAND buffers. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS1003A is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS1003A is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (each gate)

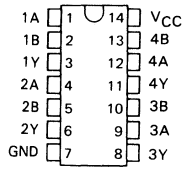
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol

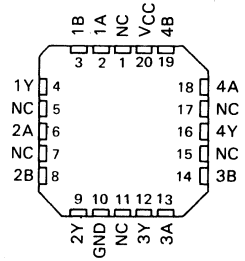


Pin numbers shown are for J and N packages.

SN54ALS1003A . . . J PACKAGE
SN74ALS1003A . . . N PACKAGE
SN74ALS1003A . . . D PACKAGE
(TOP VIEW)



SN54ALS1003A . . . FH OR FK PACKAGE
SN74ALS1003A . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

2

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1003A . . . . . −55 °C to 125 °C
SN74ALS1003A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS1003A			SN74ALS1003A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1003A			SN74ALS1003A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.86	1.6		0.86	1.6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		4.8	7.8		4.8	7.8	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1003A		SN74ALS1003A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	10	40	10	33	ns
t_{PHL}			2	18	2	12	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D2661, APRIL 1982—REVISED DECEMBER 1983

- **'AS1004 Offers High Capacitive-Drive Capability**
- **Driver Version of 'ALS04 and 'AS04**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

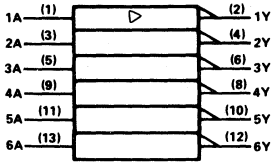
These devices contain six independent inverting drivers. They perform the Boolean function $Y = \overline{A}$.

The SN54ALS1004 and SN54AS1004 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1004 and SN74AS1004 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each inverter)

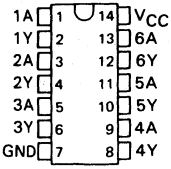
INPUT A	OUTPUT Y
H	L
L	H

logic symbol

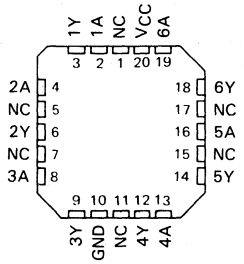


Pin numbers shown are for J and N packages.

SN54ALS1004, SN54AS1004 . . . J PACKAGE
SN74ALS1004, SN74AS1004 . . . N PACKAGE
SN74ALS1004, SN74AS1004 . . . D PACKAGE
(TOP VIEW)



SN54ALS1004, SN54AS1004 . . . FH OR FK PACKAGE
SN74ALS1004, SN74AS1004 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1004 . . . . . −55°C to 125°C
SN74ALS1004 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1004			SN74ALS1004			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1004			SN74ALS1004			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.84	3		0.84	3	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		7	12		7	12	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1004		SN74ALS1004		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	9	1	7	ns
t_{PHL}			1	8	1	6	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS1004 . . . . . −55°C to 125°C
SN74AS1004 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS1004			SN74AS1004			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS1004			SN74AS1004			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V		−135			−135		mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		3.2	5		3.2	5	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		17.2	28		17.2	28	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS1004		SN74AS1004		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	4.5	1	3.5	ns
t_{PHL}			1	4.5	1	3.5	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D2661, APRIL 1982—REVISED DECEMBER 1983

- **Buffer Version of 'ALS05**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

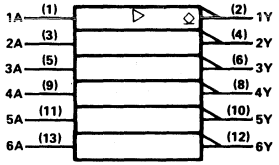
These devices contain six independent inverting buffers. They perform the Boolean function $Y = \overline{A}$. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS1005 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1005 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each inverter)

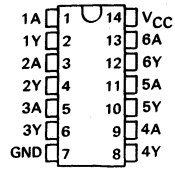
INPUT A	OUTPUT Y
H	L
L	H

logic symbol

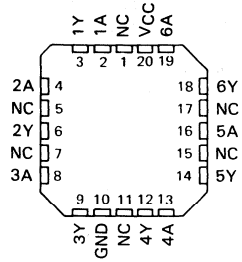


Pin numbers shown are for J and N packages.

SN54ALS1005 . . . J PACKAGE
SN74ALS1005 . . . N PACKAGE
SN74ALS1005 . . . D PACKAGE
(TOP VIEW)



SN54ALS1005 . . . FH OR FK PACKAGE
SN74ALS1005 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1005 . . . . . −55 °C to 125 °C
SN74ALS1005 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS1005			SN74ALS1005			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1005			SN74ALS1005			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.9	3		0.9	3	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		7	12		7	12	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C

switching characteristics (see Note 1)

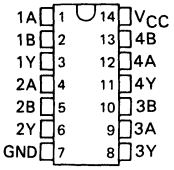
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1005		SN74ALS1005		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	5	35	5	30	ns
t_{PHL}			2	12	2	10	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D2661, DECEMBER 1982—REVISED DECEMBER 1983

- **'ALS1008A is a Buffer Version of 'ALS08**
- **'AS1008 is a Driver Version of 'AS08**
- **'AS1008 Offers High Capacitive Drive Capability**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS1008A, SN54AS1008 . . . J PACKAGE
SN74ALS1008A, SN74AS1008 . . . N PACKAGE
SN74ALS1008A, SN74AS1008 . . . D PACKAGE
(TOP VIEW)



2

description

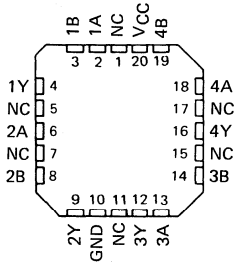
These devices contain four independent 2-input AND buffers/drivers. They perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

The SN54ALS1008A and SN54AS1008 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS1008A and SN74AS1008 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE
(each gate)

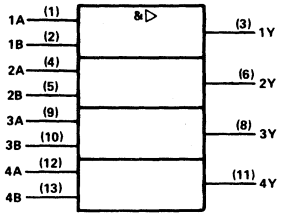
INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

SN54ALS1008A, SN54AS1008 . . . FH OR FK PACKAGE
SN74ALS1008A, SN74AS1008 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1008A . . . . . −55 °C to 125 °C
SN74ALS1008A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS1008A			SN74ALS1008A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1008A			SN74ALS1008A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4				V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.8	3		1.8	3	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		5.7	9.3		5.7	9.3	mA

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1008A		SN74ALS1008A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2	11	2	9	ns
t_{PHL}			3	11	3	9	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS1008 . . . . . −55 °C to 125 °C
SN74AS1008 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS1008			SN74AS1008			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS1008			SN74AS1008			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V		−135			−135		mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		5.6	9.5		5.6	9.5	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		13.5	22		13.5	22	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS1008		SN74AS1008		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	6	1	5	ns
t_{PHL}			1	6	1	5	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D2661, APRIL 1982—REVISED DECEMBER 1983

- **Buffer Version of 'ALS10**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

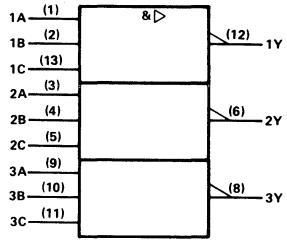
These devices contain three independent 3-input NAND buffers. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

The SN54ALS1010A is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS1010A is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (each gate)

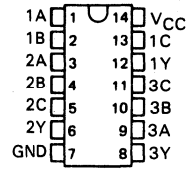
INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

logic symbol

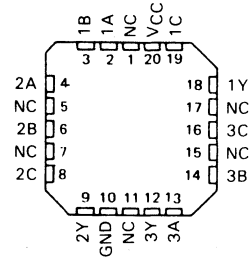


Pin numbers shown are for J and N packages.

SN54ALS1010A . . . J PACKAGE
SN74ALS1010A . . . N PACKAGE
SN74ALS1010A . . . D PACKAGE
(TOP VIEW)



SN54ALS1010A . . . FH OR FK PACKAGE
SN74ALS1010A . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1010A . . . . . −55 °C to 125 °C
SN74ALS1010A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS1010A			SN74ALS1010A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1010A			SN74ALS1010A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.65	1.2		0.65	1.2	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		3.6	5.8		3.6	5.8	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1010A		SN74ALS1010A		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	2	10	2	8	ns
t_{PHL}			2	10	2	7	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D2661, APRIL 1982—REVISED DECEMBER 1983

- **Buffer Version of 'ALS11**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

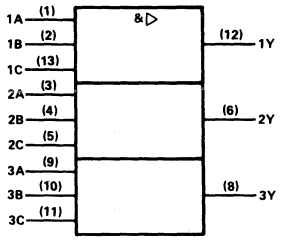
These devices contain three independent 3-input AND buffers. They perform the Boolean functions $Y = A \cdot B \cdot C$ or $Y = \overline{\overline{A}+\overline{B}+\overline{C}}$ in positive logic.

The SN54ALS1011A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1011A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

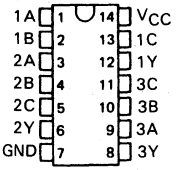
INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

logic symbol

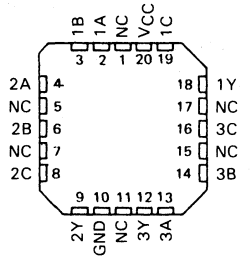


Pin numbers shown are for J and N packages.

SN54ALS1011A . . . J PACKAGE
SN74ALS1011A . . . N PACKAGE
SN74ALS1011A . . . D PACKAGE
(TOP VIEW)



SN54ALS1011A . . . FH OR FK PACKAGE
SN74ALS1011A . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1011A . . . . . −55 °C to 125 °C
SN74ALS1011A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS1011A			SN74ALS1011A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1011A			SN74ALS1011A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.4	2.3		1.4	2.3	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		4.3	7		4.3	7	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

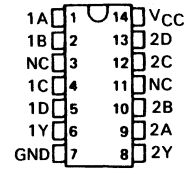
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1011A		SN74ALS1011A		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	2	12	2	10	ns
t_{PHL}			3	11	3	9	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D2661, APRIL 1982—REVISED DECEMBER 1983

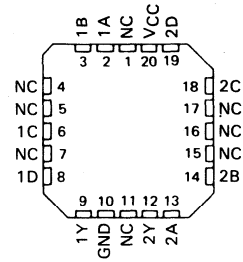
- **Buffer Version of 'ALS20A**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS1020A . . . J PACKAGE
SN74ALS1020A . . . N PACKAGE
SN74ALS1020A . . . D PACKAGE
(TOP VIEW)



2

SN54ALS1020A . . . FH OR FK PACKAGE
SN74ALS1020A . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

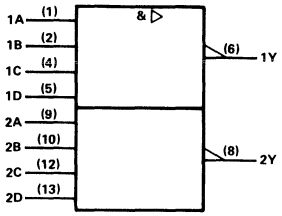
These devices contain two independent 4-input NAND buffers. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

The SN54ALS1020A is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS1020A is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1020A . . . . . −55 °C to 125 °C
SN74ALS1020A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS1020A			SN74ALS1020A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1020A			SN74ALS1020A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.5	0.8		0.5	0.8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		2.4	3.9		2.4	3.9	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

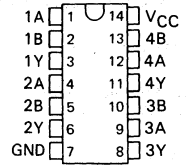
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1020A		SN74ALS1020A		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	2	10	2	8	ns
t_{PHL}			2	10	2	7	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D2661, DECEMBER 1982—REVISED DECEMBER 1983

- **'ALS1032A is a Buffer Version of 'ALS32**
- **'AS1032 is a Driver Version of 'AS32**
- **'AS1032 Offers High Capacitive Drive Capability**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS1032A, SN54AS1032 . . . J PACKAGE
SN74ALS1032A, SN74AS1032 . . . N PACKAGE
SN74ALS1032A, SN74AS1032 . . . D PACKAGE
(TOP VIEW)



2

description

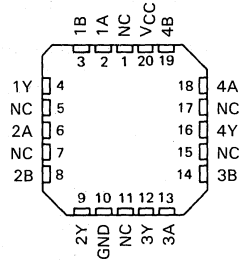
These devices contain four independent 2-input OR buffers/drivers. They perform the Boolean functions $Y = A+B$ or $Y = \overline{A \cdot B}$ in positive logic.

The SN54ALS1032A and SN54AS1032 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1032A and SN74AS1032 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each gate)

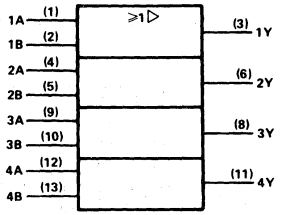
INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

SN54ALS1032A, SN54AS1032 . . . FH OR FK PACKAGE
SN74ALS1032A, SN74AS1032 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1032A . . . . . −55°C to 125°C
SN74ALS1032A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1032A			SN74ALS1032A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1032A			SN74ALS1032A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		2.5	5		2.5	5	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		6.6	10.6		6.6	10.6	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1032A		SN74ALS1032A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2	12	2	9	ns
t_{PHL}			3	15	3	12	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS1032 . . . . . −55 °C to 125 °C
SN74AS1032 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS1032			SN74AS1032			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS1032			SN74AS1032			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.9 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−135			−135			mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		7.7	11.5		7.7	11.5	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		14.7	24		14.7	24	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

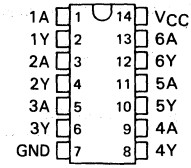
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS1032		SN74AS1032		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	7	1	5.5	ns
t_{PHL}			1	6.5	1	5.5	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

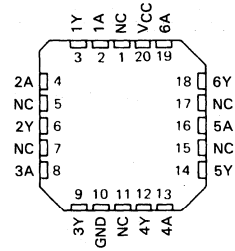
D2661, APRIL 1982—REVISED DECEMBER 1983

- **'AS1034 Offers High Capacitive-Drive Capability**
- **Noninverting Drivers**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS1034, SN54AS1034 . . . J PACKAGE
SN74ALS1034, SN74AS1034 . . . N PACKAGE
SN74ALS1034, SN74AS1034 . . . D PACKAGE
(TOP VIEW)



SN54ALS1034, SN54AS1034 . . . FH OR FK PACKAGE
SN74ALS1034, SN74AS1034 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

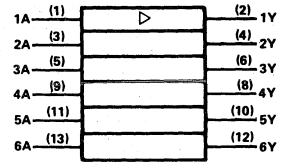
These devices contain six independent noninverting drivers. They perform the Boolean function Y = A.

The SN54ALS1034 and SN54AS1034 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1034 and SN74AS1034 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each buffer)

INPUT A	OUTPUT Y
H	H
L	L

logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1034 . . . . . −55 °C to 125 °C
SN74ALS1034 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS1034			SN74ALS1034			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output curent			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1034			SN74ALS1034			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4				V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		3	6		3	6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		8	14		8	14	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1034		SN74ALS1034		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	10	1	8	ns
t_{PHL}			1	10	1	8	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS1034 . . . . . −55°C to 125°C
SN74AS1034 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS1034			SN74AS1034			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS1034			SN74AS1034			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V		−135			−135		mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		8.5	14		8.5	14	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		20	33		20	33	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

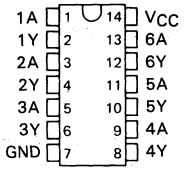
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS1034		SN74AS1034		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	6	1	5	ns
t_{PHL}			1	6	1	5	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D2661, APRIL 1982—REVISED DECEMBER 1983

- **Noninverting Buffers with Open-Collector Outputs**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS1035 . . . J PACKAGE
SN74ALS1035 . . . N PACKAGE
SN74ALS1035 . . . D PACKAGE
(TOP VIEW)



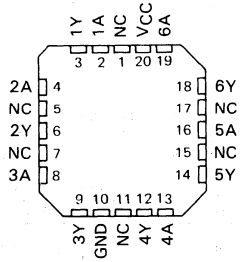
2

description

These devices contain six independent noninverting buffers. They perform the boolean functions Y = A. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS1035 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1035 is characterized for operation from 0°C to 70°C.

SN54ALS1035 . . . FH OR FK PACKAGE
SN74ALS1035 . . . FN PACKAGE
(TOP VIEW)

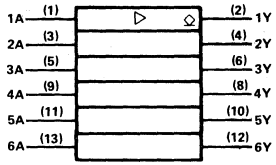


NC—No internal connection

FUNCTION TABLE (each buffer)

INPUT A	OUTPUT Y
H	H
L	L

logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1035 . . . . . −55 °C to 125 °C
SN74ALS1035 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS1035			SN74ALS1035			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1035			SN74ALS1035			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		3	6		3	6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		8	14		8	14	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1035		SN74ALS1035		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	5	35	5	30	ns
t_{PHL}			2	14	2	12	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D2661, DECEMBER 1983

- **Quad Versions of AS805A**
- **Offers High Capacitive-Drive Capability**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

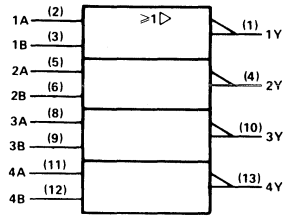
These devices contain four independent 2-input NOR drivers. They perform the Boolean functions $Y = \overline{A+B}$ or $Y = \overline{A \cdot B}$ in positive logic.

The SN54AS1036 is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74AS1036 is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (each gate)

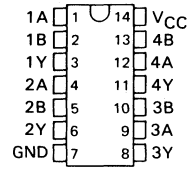
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol

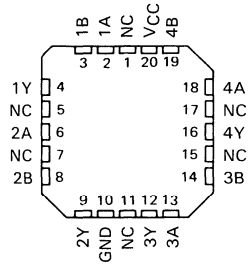


Pin numbers shown are for J and N packages.

SN54AS1036 . . . J PACKAGE
SN74AS1036 . . . N PACKAGE
SN74AS1036 . . . D PACKAGE
(TOP VIEW)



SN54AS1036 . . . FH OR FK PACKAGE
SN74AS1036 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS1036 . . . . . −55 °C to 125 °C
SN74AS1036 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS1036			SN74AS1036			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS1036			SN74AS1036			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.9 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V		−135			−135		mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		4.3	7		4.3	7	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		14	23		14	23	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS1036		SN74AS1036		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	4.5	1	4	ns
t_{PHL}			1	4.5	1	4	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TYPES SN54ALS1240, SN54ALS1241, SN74ALS1240, SN74ALS1241
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982—REVISED DECEMBER 1983

- **Low-Power Version of 'ALS240 and 'ALS241**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **P-N-P Inputs Reduce DC Loading**
- **Dependable Texas Instruments Quality and Reliability**

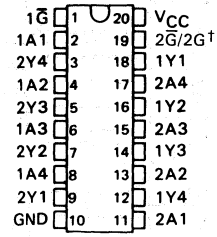
description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out and improved fan-in.

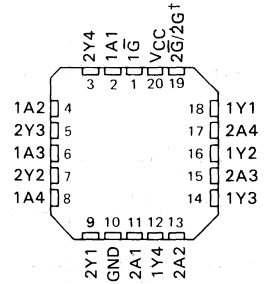
The -1 versions of the SN64ALS' parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 24 milliamperes. There are no -1 versions of the SN54ALS' parts.

The SN54ALS1240 and SN54ALS1241 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1240 and SN74ALS1241 are characterized for operation from 0°C to 70°C.

SN54ALS1240, SN54ALS1241 . . . J PACKAGE
SN74ALS1240, SN74ALS1241 . . . N PACKAGE
SN74ALS1240, SN74ALS1241 . . . DW PACKAGE
(TOP VIEW)



SN54ALS1240, SN54ALS1241 . . . FH OR FK PACKAGE
SN74ALS1240, SN74ALS1241 . . . FN PACKAGE
(TOP VIEW)



†$2\overline{G}$ for 'ALS1240 or 2G for 'ALS1241

2

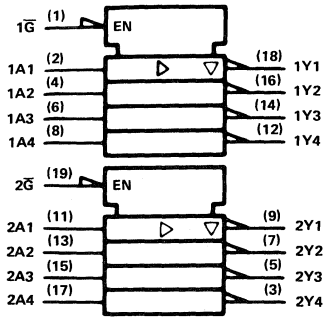
PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

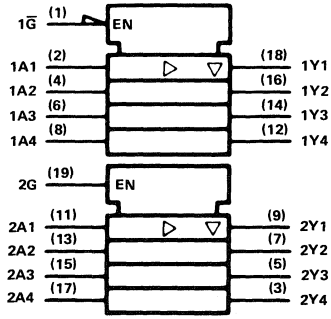
TEXAS INSTRUMENTS

logic symbols

'ALS1240



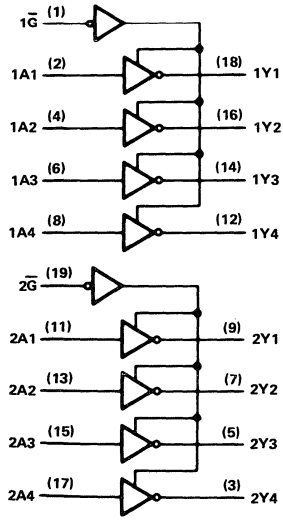
'ALS1241



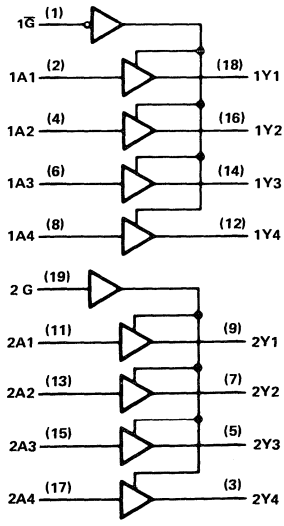
Pin numbers shown are for J and N packages.

functional block diagrams (positive logic)

'ALS1240



'ALS1241



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS1240, SN54ALS1241 . . . . . −55°C to 125°C
SN74ALS1240, SN74ALS1241 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1240 SN54ALS1241			SN74ALS1240 SN74ALS1241			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			8			16	mA
							24†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 24-mA limit applies for the SN74ALS1240-1 and SN74ALS1241-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1240 SN54ALS1241			SN74ALS1240 SN74ALS1241			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V, (I_{OL} = 24 mA for −1 versions)	I_{OL} = 16 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		6.5			6.5		mA
		Outputs low		10			10		
		Outputs disabled		12			12		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS1240 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS1240			SN74ALS1240			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y		9			9		ns
t_{PHL}				9			9		
t_{PZH}	$\overline{G}$	Y		17			17		ns
t_{PZL}				19			19		
t_{PHZ}	$\overline{G}$	Y		7			7		ns
t_{PLZ}				6			6		

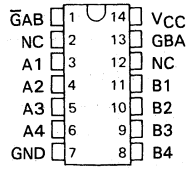
'ALS1241 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS1241			SN74ALS1241			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	Y		9			9		ns
t_{PHL}				9			9		
t_{PZH}	$\overline{G}$ or G	Y		17			17		ns
t_{PZL}				19			19		
t_{PHZ}	$\overline{G}$ or G	Y		7			7		ns
t_{PLZ}				6			6		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

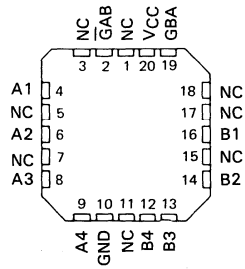
- 2-Way Asynchronous Communication between Data Buses
- P-N-P Inputs Reduce DC Loading
- Low-Power Version of 'ALS242, and 'ALS243
- Three-State Outputs
- Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS1242, SN54ALS1243 . . . J PACKAGE
SN74ALS1242, SN74ALS1243 . . . N PACKAGE
SN74ALS1242, SN74ALS1243 . . . D PACKAGE
(TOP VIEW)



2

SN54ALS1242, SN54ALS1243 . . . FH OR FK PACKAGE
SN74ALS1242, SN74ALS1243 . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

These quadruple bus transceivers are designed for two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs (GBA and $\overline{G}AB$).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 'ALS1242 and 'ALS1243 the capability to store data by simultaneous enabling of $\overline{G}AB$ and GBA. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (8 in all) will remain at their last states. The 4-bit codes appearing on the two sets of buses will be complementary for the 'ALS1242 or identical for the 'ALS1243.

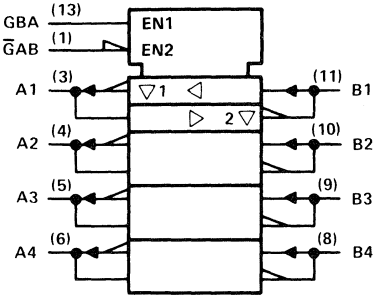
The -1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 24 milliamperes. There are no -1 versions of the SN54ALS' parts.

The SN54ALS1242 and SN54ALS1243 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS1242 and SN74ALS1243 are characterized for operation from 0 °C to 70 °C.

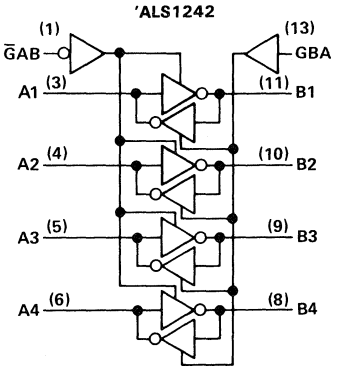
FUNCTION TABLE

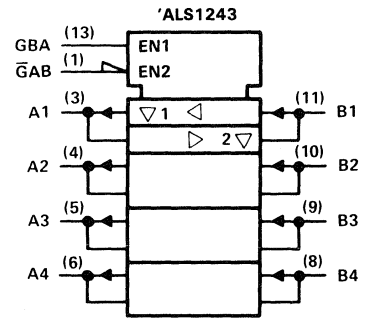
$\overline{G}AB$	GBA	'ALS1242	'ALS1243
L	L	$\overline{A}$ to B	A to B
H	H	$\overline{B}$ to A	B to A
H	L	Isolation	Isolation
L	H	Latch A and B ($A = \overline{B}$)	Latch A and B ($A = B$)

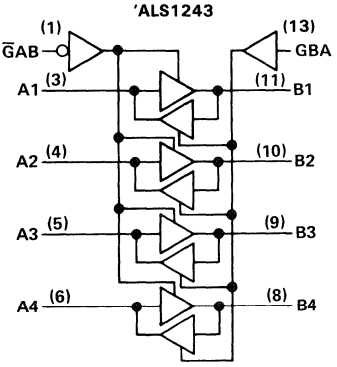
logic symbols



logic diagrams (positive logic)







Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS1242, SN54ALS1243 . . . . . −55°C to 125°C
SN74ALS1242, SN74ALS1243 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1242 SN54ALS1243			SN74ALS1242 SN74ALS1243			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			8			16	mA
							24†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 24-mA limit applies for the SN74ALS1242-1 and SN74ALS1243-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS1242 SN54ALS1243			SN74ALS1242 SN74ALS1243			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 24 mA for −1 versions)	I_{OL} = 16 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports§					−0.1			−0.1	
I_O¶		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS1242	V_{CC} = 5.5 V	Outputs high		6.5			6.5		mA
			Outputs low		10			10		
			Outputs disabled		12			12		
	'ALS1243		Outputs high		8			8		
			Outputs low		12			12		
			Outputs disabled		14			14		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

'ALS1242 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS1242			SN74ALS1242			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	B or A		9			9		ns
t_{PHL}				9			9		
t_{PZH}	$\overline{G}$AB	B		17			17		ns
t_{PZL}				19			19		
t_{PHZ}	$\overline{G}$AB	B		7			7		ns
t_{PLZ}				6			6		
t_{PZH}	GBA	A		17			17		ns
t_{PZL}				19			19		
t_{PHZ}	GBA	A		7			7		ns
t_{PLZ}				6			6		

'ALS1242 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS1243			SN74ALS1243			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	B or A		11			11		ns
t_{PHL}				11			11		
t_{PZH}	$\overline{G}$AB	B		19			19		ns
t_{PZL}				21			21		
t_{PHZ}	$\overline{G}$AB	B		9			9		ns
t_{PLZ}				8			8		
t_{PZH}	GBA	A		19			19		ns
t_{PZL}				21			21		
t_{PHZ}	GBA	A		9			9		ns
t_{PLZ}				8			8		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

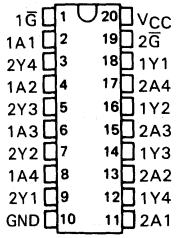
NOTE 2: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

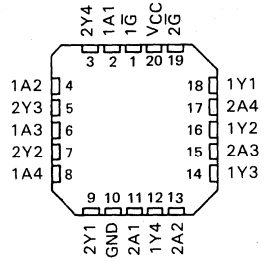
D2661, DECEMBER 1982—REVISED DECEMBER 1983

- **Low-Power Version of 'ALS244A**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **P-N-P Inputs Reduce DC Loading**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS1244A . . . J PACKAGE
SN74ALS1244A . . . N PACKAGE
SN74ALS1244A . . . DW PACKAGE
(TOP VIEW)



SN54ALS1244A . . . FH OR FK PACKAGE
SN74ALS1244A . . . FN PACKAGE
(TOP VIEW)



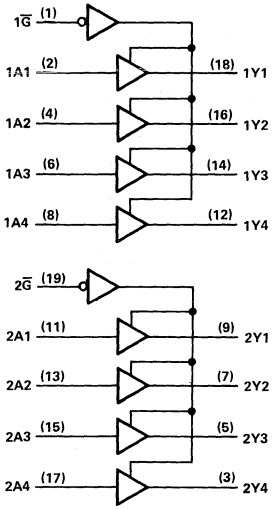
description

This octal buffer and line driver is designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'ALS1240 and 'ALS1241 this device provides the choice of selected combinations of inverting and noninverting outputs symmetrical $\overline{G}$ (active-low input control) inputs, and complementary G and $\overline{G}$ inputs.

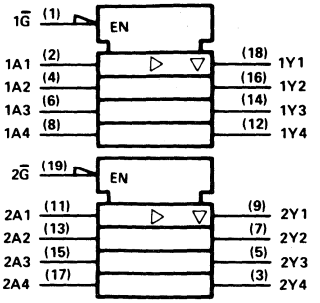
The -1 version of the SN74ALS1244A is identical to the standard version except that the recommended maximum I_{OL} is increased to 24 milliamperes. There is no -1 version of the SN54ALS1244A.

The SN54ALS1244A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1244A is characterized for operation from 0°C to 70°C.

functional block diagram (positive logic)



logic symbol



Pin numbers shown are for J and N packages

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS1244A . . . . . −55°C to 125°C
SN74ALS1244A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1244A			SN74ALS1244A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			8			16	mA
							24†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 24-mA limit applies for the SN74ALS1244A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1244A			SN74ALS1244A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V, (I_{OL} = 24 mA for −1 versions)	I_{OL} = 16 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		6	15		6	11	mA
		Outputs low		10	20		10	17	
		Outputs disabled		11	25		11	20	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1244A		SN74ALS1244A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	16	3	14	ns
t_{PHL}			3	16	3	14	
t_{PZH}	$\overline{G}$	Y	6	26	6	22	ns
t_{PZL}			6	26	6	22	
t_{PHZ}	$\overline{G}$	Y	2	12	2	10	ns
t_{PLZ}			3	16	3	13	

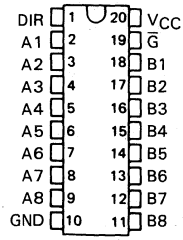
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

2

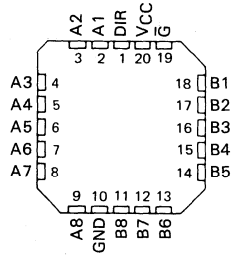
D2661, DECEMBER 1982—REVISED FEBRUARY 1984

- **'Bidirectional Bus Transceivers in High-Density 20-Pin Packages**
- **Lower-Power Version of 'ALS245A**
- **'ALS1245A is Identical to 'ALS1645A**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS1245A . . . J PACKAGE
SN74ALS1245A . . . N PACKAGE
SN74ALS1245A . . . DW PACKAGE
(TOP VIEW)



SN54ALS1245A . . . FH OR FK PACKAGE
SN74ALS1245A . . . FN PACKAGE
(TOP VIEW)



description

This octal bus transceiver is designed for asynchronous two-way communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (G) can be used to disable the device so the buses are effectively isolated.

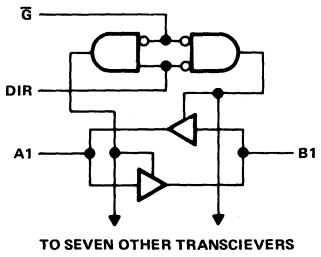
The -1 version of the SN74ALS1245A is identical to the standard versions except that the recommended maximum I_{OL} is increased to 24 milliamperes. There is no -1 version of the SN54ALS1245A.

The SN54ALS1245A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1245A is characterized for operation from 0°C to 70°C.

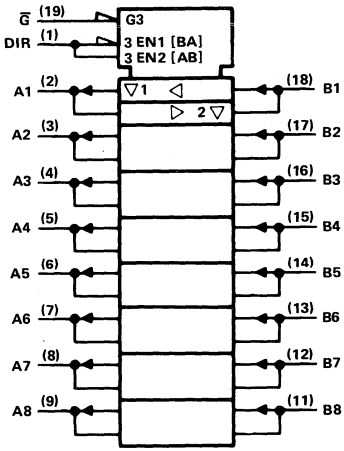
FUNCTION TABLE

CONTROL INPUTS		OPERATION
$\overline{G}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic diagram (positive logic)



logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS1245A . . . . . −55°C to 125°C
SN74ALS1245A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1245A			SN74ALS1245A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			8			16	mA
							24†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limit applies only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 24-mA limit applies for the SN74ALS1245A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS1245A			SN74ALS1245A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 24 mA for −1 version)	I_{OL} = 16 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A, B ports§	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A, B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A, B ports§					−0.1			−0.1	
I_O¶		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Output high		21	33		21	30	mA
			Output low		23	36		23	33	
			Output disabled		25	40		25	36	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1245A		SN74ALS1245A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	15	2	13	ns
t_{PHL}			2	15	2	13	
t_{PZH}	$\overline{G}$	A or B	8	28	8	25	ns
t_{PZL}			8	28	8	25	
t_{PHZ}	$\overline{G}$	A or B	2	14	2	12	ns
t_{PLZ}			3	22	3	18	

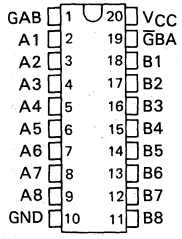
NOTE 1: For load circuit and voltage waveforms, see page 1-12

D2661, DECEMBER 1982—REVISED DECEMBER 1983

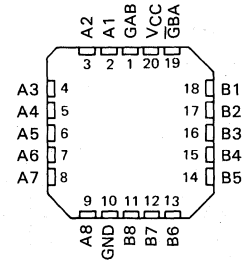
- **Bus Transceivers in High-Density 20-Pin DIPs Small Outline (SO) and the Plastic and Ceramic Chip Carriers Packages**
- **Local Bus Latch Capability**
- **Choice of True or Inverting Logic**
- **Dependable Texas Instruments Quality and Reliability**
- **Choice of 3-State or Open-Collector Outputs**

DEVICE	OUTPUT	LOGIC
'ALS1620	3-State	Inverting
'ALS1621	Open-Collector	True
'ALS1622	Open-Collector	Inverting
'ALS1623	3-State	True

SN54ALS' . . . J PACKAGE
SN74ALS' . . . N PACKAGE
SN74ALS' . . . DW PACKAGE
(TOP VIEW)



SN54ALS' . . . FH OR FK PACKAGE
SN74ALS' . . . FN PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}$BA and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 'ALS1620 thru 'ALS1623 the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the 'ALS1621 and 'ALS1623 or complementary for the 'ALS1620 and 'ALS1622.

The -1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 24 mA. There are no -1 versions of the SN54ALS' parts.

The SN54ALS1620 thru SN54ALS1623 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1620 thru SN74ALS1623 are characterized for operation from 0°C to 70°C.

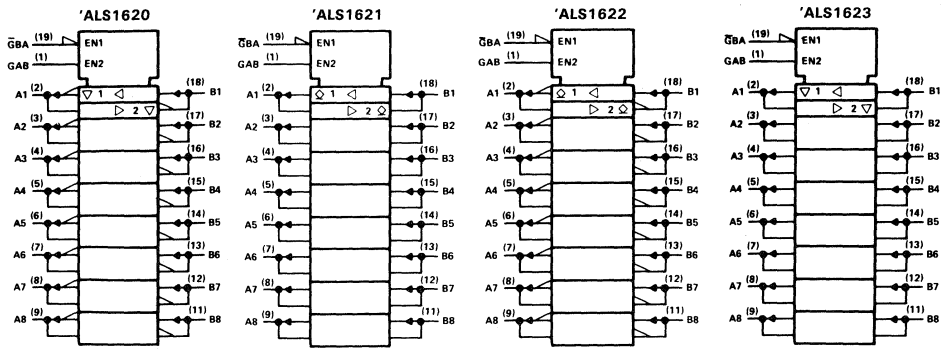
FUNCTION TABLE

ENABLE	INPUTS	OPERATION	
$\overline{G}$BA	GAB	'ALS1620, 'ALS1622	'ALS1621, 'ALS1623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Isolation	Isolation
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus	B data to A bus, A data to B bus

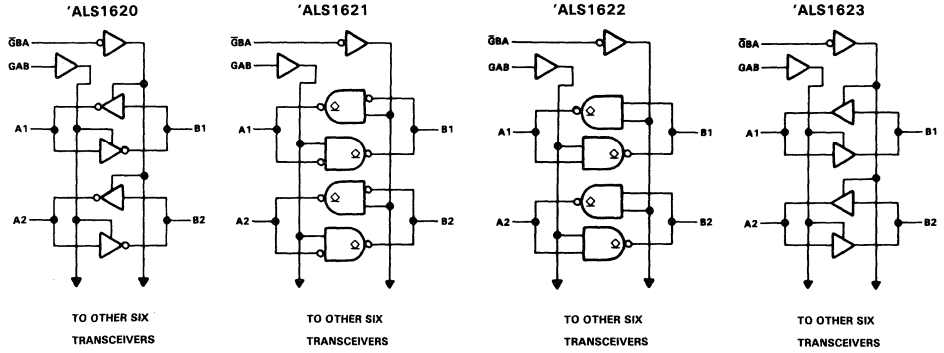
PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

logic symbols



functional block diagrams (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS1620, SN54ALS1623 . . . . . −55°C to 125°C
SN74ALS1620, SN74ALS1623 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1620 SN54ALS1623			SN74ALS1620 SN74ALS1623			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			8			16	mA
							24†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 24-mA limit applies for the SN74ALS1620-1 and SN74ALS1623-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS1620 SN54ALS1623			SN74ALS1620 SN74ALS1623			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 24 mA for −1 versions)	I_{OL} = 16 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports§					−0.1			−0.1	
I_O¶		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS1620	V_{CC} = 5.5 V	Outputs high		14			14		mA
			Outputs low		19			19		
			Outputs disabled		21			21		
	'ALS1623		Outputs high		11			11		
			Outputs low		18			18		
			Outputs disabled		13			13		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

'ALS1620 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS1620			SN74ALS1620			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	B		9			9		ns
t_{PHL}				6			6		
t_{PLH}	B	A		9			9		ns
t_{PHL}				6			6		
t_{PZH}	$\overline{G}$BA	A		14			14		ns
t_{PZL}				17			17		
t_{PHZ}	$\overline{G}$BA	A		7			7		ns
t_{PLZ}				11			11		
t_{PZH}	GAB	B		14			14		ns
t_{PZL}				17			17		
t_{PHZ}	GAB	B		7			7		ns
t_{PLZ}				11			11		

'ALS1623 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS1623			SN74ALS1623			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	B		8			8		ns
t_{PHL}				8			8		
t_{PLH}	B	A		8			8		ns
t_{PHL}				8			8		
t_{PZH}	$\overline{G}$BA	A		18			18		ns
t_{PZL}				21			21		
t_{PHZ}	$\overline{G}$BA	A		12			12		ns
t_{PLZ}				13			13		
t_{PZH}	GAB	B		18			18		ns
t_{PZL}				21			21		
t_{PHZ}	GAB	B		12			12		ns
t_{PLZ}				13			13		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs and I/O ports . . . . . 7 V
Operating free-air temperature range: SN54ALS1621, SN54ALS1622 . . . . . −55°C to 125°C
SN74ALS1621, SN74ALS1622 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1621 SN54ALS1622			SN74ALS1621 SN74ALS1622			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	mV
I_{OL}	Low-level output current			8			16	mA
							24†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 24-mA limit applies for the SN74ALS1621-1 and SN74ALS1622-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS1621 SN54ALS1622			SN74ALS1621 SN74ALS1622			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 24 mA for −1 versions)	I_{OL} = 16 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports§					−0.1			−0.1	
I_{CC}	'ALS1621	V_{CC} = 5.5 V	Outputs high		11			11		mA
			Outputs low		16			16		
	'ALS1622		Outputs high		13			13		
			Outputs low		18			18		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

Additional information on these products can be obtained from the factory as it becomes available.

'ALS1621 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX						UNIT
			SN54ALS1621			SN74ALS1621			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	B		22			22		ns
t_{PHL}				14			14		
t_{PLH}	B	A		22			22		ns
t_{PHL}				14			14		
t_{PLH}	$\overline{G}$BA	A		33			33		ns
t_{PHL}				24			24		
t_{PLH}	GAB	B		33			33		ns
t_{PHL}				24			24		

'ALS1622 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX						UNIT
			SN54ALS1622			SN74ALS1622			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	B		25			25		ns
t_{PHL}				13			13		
t_{PLH}	B	A		25			25		ns
t_{PHL}				13			13		
t_{PLH}	$\overline{G}$BA	A		31			31		ns
t_{PHL}				28			28		
t_{PLH}	GAB	B		31			31		ns
t_{PHL}				28			28		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

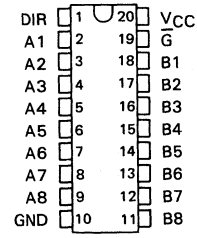
Additional information on these products can be obtained from the factory as it becomes available.

TYPES SN54ALS1638, SN54ALS1639, SN74ALS1638, SN74ALS1639
OCTAL BUS TRANSCEIVERS

D2661, DECEMBER 1982—REVISED DECEMBER 1983

- **Bidirectional Bus Transceivers in High-Density 20-Pin Packages**
- **Low-Power Version of 'ALS638 and 'ALS639**
- **Choice of True or Inverting Logic**
- **A bus Outputs are Open-Collector; B Bus Outputs are 3-State**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS1638, SN54ALS1639 . . . J PACKAGE
SN74ALS1638, SN74ALS1639 . . . N PACKAGE
SN74ALS1638, SN74ALS1639 . . . DW PACKAGE
(TOP VIEW)



2

description

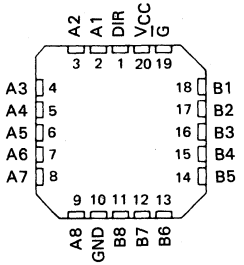
These octal bus transceivers are designed for asynchronous two-way communication between open-collector and 3-State buses. The devices transmit data from the A bus (open-collector) to the B bus (3-state) or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to enable the device so the buses are effectively isolated.

DEVICE	A OUTPUT	B OUTPUT	LOGIC
'ALS1638	Open-Collector	3-State	Inverting
'ALS1639	Open-Collector	3-State	True

The -1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 24 milliamperes. There are no -1 versions of the SN54ALS' parts.

The SN54ALS1638 and SN54ALS1639 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1638 and SN74ALS1639 are characterized for operation from 0°C to 70°C.

SN54ALS1638, SN54ALS1639 . . . FH OR FK PACKAGE
SN74ALS1638, SN74ALS1639 . . . FN PACKAGE
(TOP VIEW)



FUNCTION TABLE

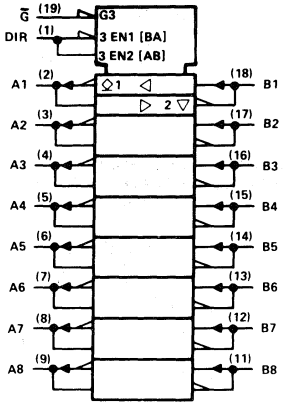
CONTROL INPUTS		OPERATION	
$\overline{G}$	DIR	'ALS1638	'ALS1639
L	L	B data to A bus	B data to A bus
L	H	A data to B bus	A data to B bus
H	X	Isolation	Isolation

ADVANCE INFORMATION

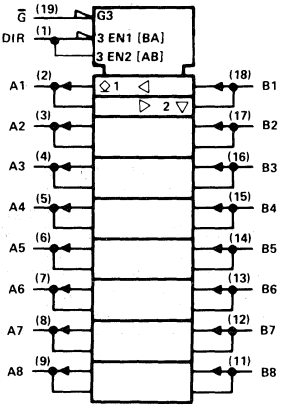
This document contains information on a new product. Specifications are subject to change without notice.

logic symbols

'ALS1638



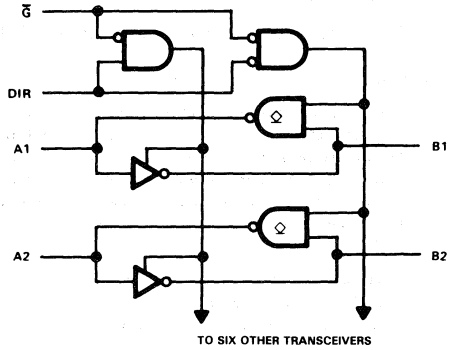
'ALS1639



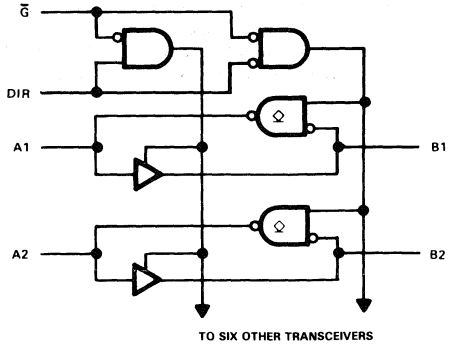
Pin numbers shown are for J and N packages.

functional block diagrams (positive logic)

'ALS1638



'ALS1639



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
A bus I/O ports . . . . . 7 V
B bus I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS1638, SN54ALS1639 . . . . . −55°C to 125°C
SN74ALS1638, SN74ALS1639 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS1638 SN54ALS1639			SN74ALS1638 SN74ALS1639			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{OH}	High-level voltage	A ports			5.5			5.5	V
I_{OH}	High-level output current	B ports			−12			−15	mA
I_{OL}	Low-level output current	A or B ports			8			16	mA
								24†	
T_A	Operating free-air temperature		−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 24-mA limit applies for the SN74ALS1638-1 and SN74ALS1639-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS1638 SN54ALS1639			SN74ALS1638 SN74ALS1639			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	A ports	V_{CC} = 4.5 V,	V_O = 5.5 V			0.1			0.1	mA
V_{OH}	B ports	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	A or B ports	V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 24 mA for −1 versions)	I_{OL} = 16 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports§					−0.1			−0.1	
I_O¶	B ports	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		21			21		mA
			Outputs low		23			23		
			Outputs disabled		25			25		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

'ALS1638 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω (A outputs), R1 = R2 = 500 Ω (B outputs), T_A = MIN to MAX						UNIT
			SN54ALS1638			SN74ALS1638			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	B		6			6		ns
t_{PHL}				21			21		
t_{PLH}	B	A		6			6		ns
t_{PHL}				8			8		
t_{PLH}	$\overline{G}$, DIR	A		23			23		ns
t_{PHL}				17			17		
t_{PZH}	$\overline{G}$	B		12			12		ns
t_{PZL}				15			15		
t_{PHZ}	$\overline{G}$	B		6			6		ns
t_{PLZ}				7			7		

'ALS1639 switching characteistics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω (A outputs), R1 = R2 = 500 Ω (B outputs), T_A = MIN to MAX						UNIT
			SN54ALS1639			SN74ALS1639			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	B		7			7		ns
t_{PHL}				21			21		
t_{PLH}	B	A		7			7		ns
t_{PHL}				9			9		
t_{PLH}	$\overline{G}$, DIR	A		23			23		ns
t_{PHL}				19			19		
t_{PZH}	$\overline{G}$	B		14			14		ns
t_{PZL}				17			17		
t_{PHZ}	$\overline{G}$	B		7			7		ns
t_{PLZ}				9			9		

†All typical values at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

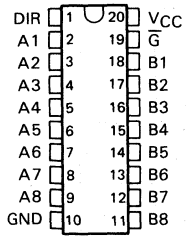
TYPES SN54ALS1640A, SN54ALS1645A, SN54ALS1641 THRU SN54ALS1644
SN74ALS1640A, SN74ALS1645A, SN74ALS1641 THRU SN74ALS1644
OCTAL BUS TRANSCEIVERS

D2661, DECEMBER 1982—REVISED DECEMBER 1983

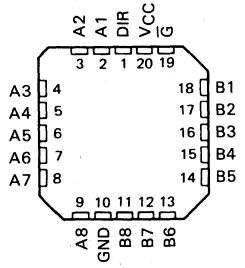
- **Bidirectional Bus Transceivers in High-Density 20-Pin Packages**
- **Lower-Power Versions of 'ALS640 Series**
- **Choice of True or Inverting Logic**
- **Choice of 3-State or Open-Collector Outputs**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	OUTPUT	LOGIC
'ALS1640A	3-State	Inverting
'ALS1641	Open-Collector	True
'ALS1642	Open-Collector	Inverting
'ALS1643	3-State	True and Inverting
'ALS1644	Open-Collector	True and Inverting
'ALS1645A	3-State	True

SN54ALS'... J PACKAGE
SN74ALS'... N PACKAGE
SN74ALS'... DW PACKAGE
(TOP VIEW)



SN54' ... FH OR FK PACKAGE
SN74'... FN PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so the buses are effectively isolated.

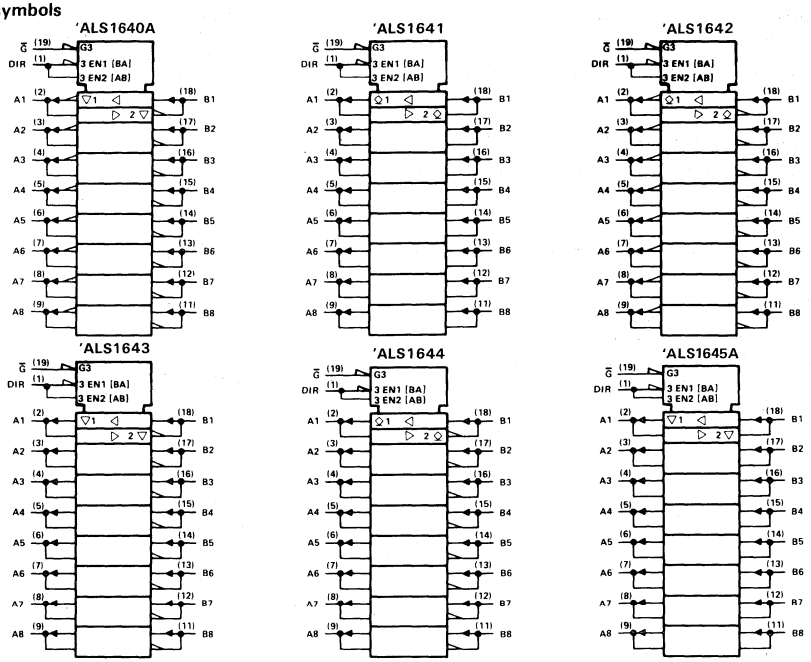
The -1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 24 milliamperes. There are no -1 versions of the SN54ALS' parts.

The SN54ALS' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS' family is characterized for operation from 0°C to 70°C.

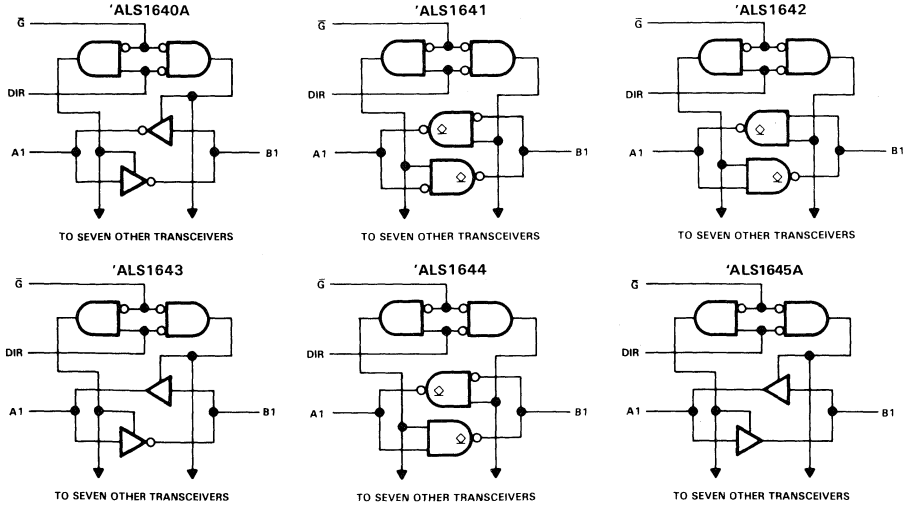
FUNCTION TABLE

CONTROL INPUTS		OPERATION		
$\overline{G}$	DIR	'ALS1640A 'ALS1642	'ALS1641 'ALS1645A	'ALS1643 'ALS1644
L	L	$\overline{B}$ data to A bus	B data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus	$\overline{A}$ data to B bus
H	X	Isolation	Isolation	Isolation

logic symbols



logic diagrams (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS1640A, SN54ALS1643, SN54ALS1645A . . . −55°C to 125°C
SN74ALS1640A, SN74ALS1643, SN74ALS1645A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1640A SN54ALS1643 SN54ALS1645A			SN74ALS1640A SN74ALS1643 SN74ALS1645A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			8			16	mA
							24†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 24-mA limit applies for the SN74ALS1640A-1, SN74ALS1643-1, and SN74ALS1645A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS1640A SN54ALS1643 SN54ALS1645A			SN74ALS1640A SN74ALS1643 SN74ALS1645A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 24 mA for −1 versions)	I_{OL} = 16 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports§					−0.1			−0.1	
I_O¶		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS1640A	V_{CC} = 5.5 V			18	35		18	32	mA
	'ALS1643				22			22		
	'ALS1645A				25	40		25	36	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

'ALS1640A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1640A		SN74ALS1640A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	5	17	5	15	ns
t_{PHL}			2	13	2	10	
t_{PZH}	$\overline{G}$	A or B	5	23	5	20	ns
t_{PZL}			5	25	5	22	
t_{PHZ}	$\overline{G}$	A or B	2	12	2	10	ns
t_{PLZ}			5	16	5	13	

'ALS1643 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS1643			SN74ALS1643			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	B		7			7		ns
t_{PHL}				7			7		
t_{PLH}	B	A		8			8		ns
t_{PHL}				8			8		
t_{PZH}	$\overline{G}$	A		18			18		ns
t_{PZL}				21			21		
t_{PHZ}	$\overline{G}$	A		12			12		ns
t_{PLZ}				13			13		
t_{PZH}	$\overline{G}$	B		18			18		ns
t_{PZL}				21			21		
t_{PHZ}	$\overline{G}$	B		12			12		ns
t_{PLZ}				13			13		

'ALS1645A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1645A		SN74ALS1645A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	15	2	13	ns
t_{PHL}			2	15	2	13	
t_{PZH}	$\overline{G}$	A or B	8	28	8	25	ns
t_{PZL}			8	28	8	25	
t_{PHZ}	$\overline{G}$	A or B	2	14	2	12	ns
t_{PLZ}			3	22	3	18	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs and I/O ports . . . . . 7 V
Operating free-air temperature range: SN54ALS1641, SN54ALS1642, SN54ALS1644 . . . . . −55°C to 125°C
SN74ALS1641, SN74ALS1642, SN74ALS1644 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1641 SN54ALS1642 SN54ALS1644			SN74ALS1641 SN74ALS1642 SN74ALS1644			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			8			16	mA
							24†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 24-mA limit applies for the SN74ALS1641-1, SN74ALS1642-1, and SN74ALS1644-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS1641 SN54ALS1642 SN54ALS1644			SN74ALS1641 SN74ALS1642 SN74ALS1644			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 24 mA for -1 versions)	I_{OL} = 16 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports§					−0.1			−0.1	
I_{CC}	'ALS1641	V_{CC} = 5.5 V			23			23		mA
	'ALS1642				20			20		
	'ALS1644				22			22		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

'ALS1641 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS1641			SN74ALS1641			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A or B	B or A		22			22		ns
t_{PHL}				14			14		
t_{PLH}	$\overline{G}$ or DIR	A or B		26			26		ns
t_{PHL}				26			26		

'ALS1642 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS1642			SN74ALS1642			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A or B	B or A		25			25		ns
t_{PHL}				13			13		
t_{PLH}	$\overline{G}$ or DIR	A or B		29			29		ns
t_{PHL}				29			29		

'ALS1644 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS1644			SN74ALS1644			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A	B		27			27		ns
t_{PHL}				19			19		
t_{PLH}	B	A		24			24		ns
t_{PHL}				17			17		
t_{PLH}	$\overline{G}$ or DIR	A		30			30		ns
t_{PHL}				27			27		
t_{PLH}	$\overline{G}$ or DIR	B		24			24		ns
t_{PHL}				30			30		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

AUGUST 1984

- High Capacitive Drive Capability
- 'ALS1804 Has Typical Delay Time of 4 ns (C_L = 50 pF) and Typical Power Dissipation of 3.4 mW per Gate
- 'AS1804 has Typical Delay Time of 2.6 ns (C_L = 50 pF) and Typical Power Dissipation of Less than 9 mW per gate
- Center V_{CC} and GND Configuration Provides Minimum Lead Inductance in High Current Switching Applications
- Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain six independent 2-input NAND drivers. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

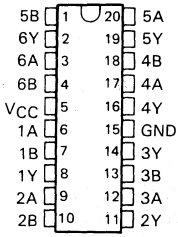
The center pin configuration used in the 'ALS1804 and 'AS1804 provides a reduction of lead inductance when compared to the 'ALS804 and 'AS804. This reduction of lead inductance will minimize noise generated onto either the V_{CC} or GND bus. This reduction is significant in high current switching applications.

The SN54ALS1804 and SN54AS1804 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1804 and SN74AS1804 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each driver)

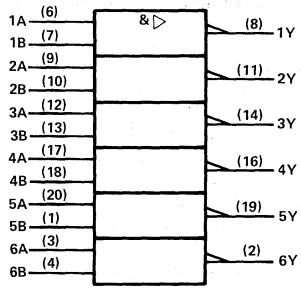
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

SN54ALS1804, SN54AS1804 . . . J PACKAGE
SN74ALS1804, SN74AS1804 . . . N PACKAGE
SN74ALS1804, SN74AS1804 . . . DW PACKAGE
(TOP VIEW)



Use 'ALS804 or 'AS804B for chip carrier option.

logic symbol†



Pin numbers shown are for J and N packages.
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1804 . . . . . −55°C to 125°C
SN74ALS1804 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1804			SN74ALS1804			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1804			SN74ALS1804			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} −12 mA	2						
	V_{CC} = 4.5 V,	I_{OH} −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.9	2.5		0.9	2.5	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		7	12		7	12	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1804		SN74ALS1804		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2	8	2	6	ns
t_{PHL}			2	9	2	7	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS1804 . . . . . −55°C to 125°C
SN74AS1804 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS1804			SN74AS1804			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS1804			SN74AS1804			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V		−135			−135		mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		3.5	5		3.5	5	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		16	27		16	27	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

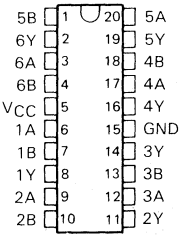
switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS1804		SN74AS1804		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	5	1	4	ns
t_{PHL}			1	5	1	4	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

- High Capacitive Drive Capability
- 'ALS1808 Has Typical Delay Time of 4.8 ns (C_L = 50 pF) and Typical Power Dissipation of 4.5 mW per Gate
- 'AS1808 Has Typical Delay Time of 3.2 ns (C_L = 50 pF) and Typical Power Dissipation of Less than 13 mW per Gate
- Center V_{CC} and GND Configuration Provides Minimum Lead Inductance in High Current Switching Applications
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- Dependable Texas Instruments Quality and Reliability

SN54ALS1808, SN54AS1808 . . . J PACKAGE
SN74ALS1808, SN74AS1808 . . . N PACKAGE
SN74ALS1808, SN74AS1808 . . . DW PACKAGE
(TOP VIEW)



Use 'ALS808 or 'AS808B for chip carrier option.

description

These devices contain six independent 2-input AND drivers. They perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

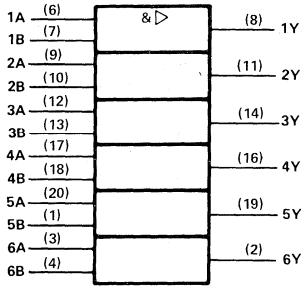
The center pin configuration used in the 'ALS1808 and 'AS1808 provides a reduction of lead inductance when compared to the 'ALS808 and 'AS808. This reduction of lead inductance will minimize noise generated onto either the V_{CC} and GND bus. This reduction is significant in high current switching applications.

The SN54ALS1808 and SN54AS1808 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1808 and SN74AS1808 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each driver)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol†



Pin numbers shown are for J and N packages.
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1808 . . . . . −55°C to 125°C
SN74ALS1808 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1808			SN74ALS1808			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1808			SN74ALS1808			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
	V_{CC} = 4.5 V,	I_{OL} = −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_H	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4 5		3	6		3	6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		8	16		8	16	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS1808			SN74ALS1808			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A or B	Y	2		10	2		8	ns
t_{PHL}			2		10	2		8	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS1808 . . . . . −55°C to 125°C
SN74AS1808 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS1808			SN74AS1808			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS1808			SN74AS1808			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V		−135			−135		mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		8	13		8	13	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		20	33		20	33	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS1808		SN74AS1808		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	6.5	1	6	ns
t_{PHL}			1	6.5	1	6	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

AUGUST 1984

- **High Capacitive Drive Capability**
- **'ALS1832 Has Typical Delay Time of 5 ns (C_L = 50 pF) and Typical Power Dissipation of 5.3 mW per Gate**
- **'AS1832 Has Typical Delay Time of 3.9 ns (C_L = 50 pF) and Typical Power Dissipation of Less than 17 mW per Gate**
- **Center V_{CC} and GND Configuration Provides Minimum Lead Inductance in High Current Switching Applications**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain six independent 2-input OR drivers. They perform the Boolean functions $Y = A+B$ or $Y = \overline{\overline{A} \cdot \overline{B}}$ in positive logic.

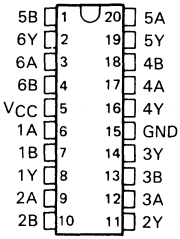
The center pin configuration used in the 'ALS1832 and 'AS1832 provides a reduction of lead inductance when compared to the 'ALS832 and 'AS832. This reduction of lead inductance will minimize noise generated onto either the V_{CC} or GND bus. This reduction is significant in high current switching applications.

The SN54ALS1832 and SN54AS1832 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1832 and SN74AS1832 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each driver)

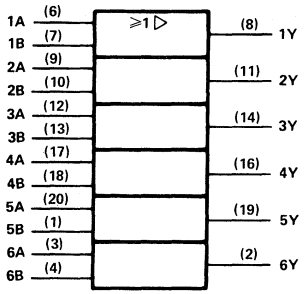
INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

SN54ALS1832, SN54AS1832 . . . J PACKAGE
SN74ALS1832, SN74AS1832 . . . N PACKAGE
SN74ALS1832, SN74AS1832 . . . DW PACKAGE
(TOP VIEW)



Use 'ALS832 or 'AS832B for chip carrier option.

logic symbol†



Pin numbers shown are for J and N packages.

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1832 . . . . . −55°C to 125°C
SN74ALS1832 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1832			SN74ALS1832			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1832			SN74ALS1832			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		4	8		4	8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		9.5	16		9.5	16	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1832		SN74ALS1832		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2	10	2	8	ns
t_{PHL}			2	10	2	8	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS1832 . . . . . −55°C to 125°C
SN74AS1832 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS1832			SN74AS1832			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS1832			SN74AS1832			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V		−135			−135		mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		11	17		11	17	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		22	36		22	36	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS1832		SN74AS1832		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	7	1	6.3	ns
t_{PHL}			1	7	1	6.3	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

SN54ALS2540, SN54ALS2541, SN74ALS2540, SN74ALS2541
OCTAL LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS

JUNE 1984

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **P-N-P Inputs Reduce D-C Loading**
- **Outputs have 25 Ω Series Resistor, No External Resistors are Required**
- **Package Options Include Small Outline (SO) and Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

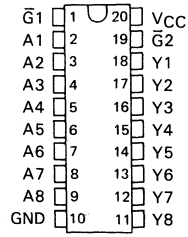
These octal buffers and line drivers are designed to drive capacitive input characteristics of MOS devices and have the performance of the popular SN54ALS240A/SN74ALS240A series. At the same time, they offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout.

The three-state control gate is a 2-input NOR such that if either G1 or G2 is high, all eight outputs are in the high-impedance state.

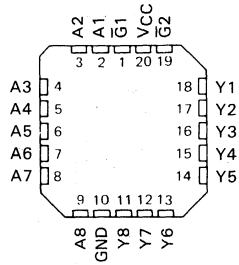
The 'ALS2540 offers inverting data and the 'ALS2541 offers true data at the outputs.

The SN54ALS' is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS' is characterized for operation from 0°C to 70°C.

SN54ALS2540, SN54ALS2541 . . . J PACKAGE
SN74ALS2540, SN74ALS2541 . . . N PACKAGE
SN74ALS2540, SN74ALS2541 . . . DW PACKAGE
(TOP VIEW)

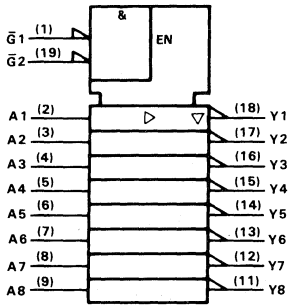


SN54ALS2540, SN54ALS2541 . . . FH OR FK PACKAGE
SN74ALS2540, SN74ALS2541 . . . FN PACKAGE
(TOP VIEW)

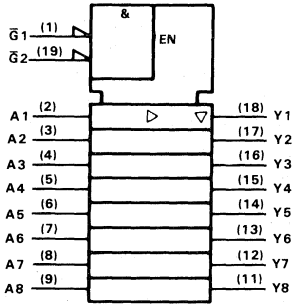


logic symbols

'ALS2540



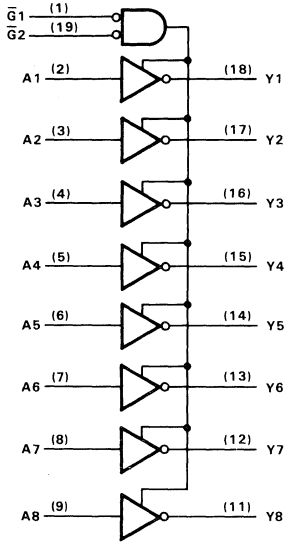
'ALS2541



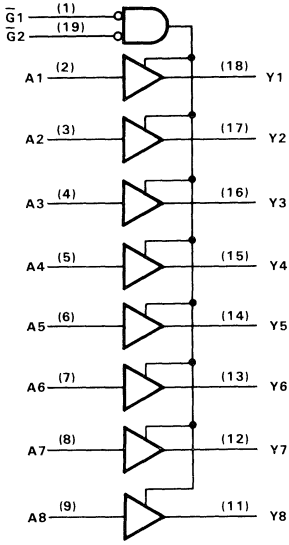
Pin numbers shown are for J and N packages.

logic diagrams (positive logic)

'ALS2540



'ALS2541



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS2540, SN54ALS2541 . . . . . −55°C to 125°C
SN74ALS2540, SN74ALS2541 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS2540 SN54ALS2541			SN74ALS2540 SN74ALS2541			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			12			12	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS2540 SN54ALS2541			SN74ALS2540 SN74ALS2541			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 1 mA		0.15	0.5		0.15	0.5	V
		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.35	0.8		0.35	0.8	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_{OH}		V_{CC} = 4.5 V,	V_O = 2 V	−15			−15			mA
I_{OL}		V_{CC} = 4.5 V,	V_O = 2 V	15			15			mA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}	'ALS2540	V_{CC} = 5.5 V	Outputs high		5	10		5	10	mA
			Outputs low		13	22		13	22	
			Outputs disabled		11	19		11	19	
	'ALS2541	V_{CC} = 5.5 V	Outputs high		6.5	15		6.5	15	mA
			Outputs low		15	25		15	25	
			Outputs disabled		13.5	22		13.5	22	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS2540 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS2540		SN74ALS2540		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	2	14	2	12	ns
t_{PHL}			2	13	2	11	
t_{PZH}	$\overline{G}$	Y	3	17	3	15	ns
t_{PZL}			5	22	5	21	
t_{PHZ}	$\overline{G}$	Y	1	10	1	8	ns
t_{PLZ}			1	10	1	8	

'ALS2541 switching characteristics (see Note 1)

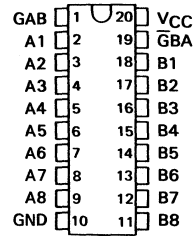
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS2541		SN74ALS2541		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	2	17	2	15	ns
t_{PHL}			2	14	2	12	
t_{PZH}	$\overline{G}$	Y	3	18	3	16	ns
t_{PZL}			5	24	5	20	
t_{PHZ}	$\overline{G}$	Y	1	10	1	8	ns
t_{PLZ}			1	10	1	8	

NOTE 1: For load circuit and voltage waveforms, see page 1-12

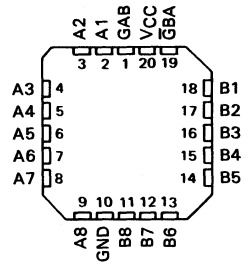
DECEMBER 1983

- **Bidirectional Octal Bus Transceivers For Driving MOS Devices**
- **I/O Ports Have 25 Ohm Series Resistors So No External Resistors Are Required**
- **Local Bus-Latch Capability**
- **Choice of True or Inverting Logic**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS' . . . J PACKAGE
SN74AS' . . . N PACKAGE
SN74AS' . . . DW PACKAGE
(TOP VIEW)



SN54AS' . . . FH OR FK PACKAGE
SN74AS' . . . FN PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed to drive the capacitive input characteristics of MOS devices and allow asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}$BA and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 'AS2620 or 'AS2623 the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the 'AS2623 or complementary for the 'AS2620.

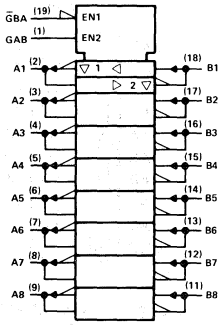
The SN54AS2620 and SN54AS2623 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74AS2620 and SN74AS2623 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE

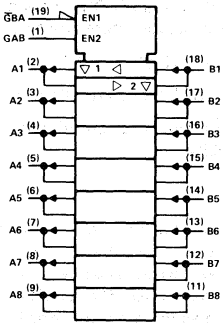
ENABLE INPUTS		OPERATION	
$\overline{G}$BA	GAB	'AS2620	'AS2623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Isolation	Isolation
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus	B data to A bus, A data to B bus

logic symbols

'AS2620



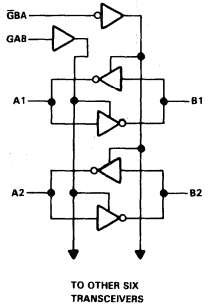
'AS2623



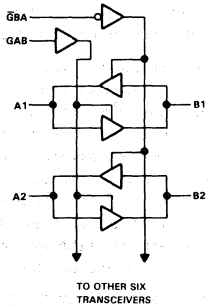
Pin numbers shown are for J and N packages.

logic diagrams (positive logic)

'AS2620



'AS2623



2

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54AS2620, SN54AS2623 . . . . . −55 °C to 125 °C
SN74AS2620, SN74AS2623 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS2620 SN54AS2623			SN74AS2620 SN74AS2623			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS2620 SN54AS2623			SN74AS2620 SN74AS2623			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 1 mA		0.15	0.4		0.15	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.35	0.7		0.35	0.7	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
	A or B ports‡					50			50	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A or B ports‡					−0.5			−0.5	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{OH}		V_{CC} = 4.5 V,	V_O = 2 V	−35			−35			mA
I_{OL}		V_{CC} = 4.5 V,	V_O = 2 V	35			35			mA
I_{CC}	'AS2620	V_{CC} = 5.5 V	Outputs high		62	100		62	100	mA
			Outputs low		74	121		74	121	
			Outputs disabled		48	77		48	77	
	'AS2623	V_{CC} = 5.5 V	Outputs high		57	93		57	93	
			Outputs low		116	189		116	189	
			Outputs disabled		72	116		72	116	

†All typical values are at V_{CC} = 5 V, T_A = 25 °C
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS2620 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS2620		SN74AS2620		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1	9.5	1	8	ns
t_{PHL}			1	7.5	1	6.5	
t_{PLH}	B	A	1	9.5	1	8	ns
t_{PHL}			1	7.5	1	6.5	
t_{PZH}	$\overline{G}$BA	A	1	11	1	10	ns
t_{PZL}			1	12	1	11	
t_{PHZ}	$\overline{G}$BA	A	1	7.5	1	6	ns
t_{PLZ}			1	15	1	12	
t_{PZH}	GAB	B	1	9	1	8	ns
t_{PZL}			1	9	1	8	
t_{PHZ}	GAB	B	1	12	1	11	ns
t_{PLZ}			1	12	1	11	

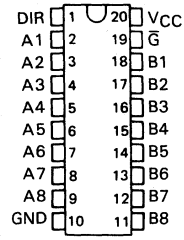
'AS2623 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS2623		SN74AS2623		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1	9.5	1	8.5	ns
t_{PHL}			1	8.5	1	7.5	
t_{PLH}	B	A	1	10	1	9	ns
t_{PHL}			1	9	1	7.5	
t_{PZH}	$\overline{G}$BA	A	1	12.5	1	11	ns
t_{PZL}			1	12	1	11	
t_{PHZ}	$\overline{G}$BA	A	1	8.5	1	7.5	ns
t_{PLZ}			1	13	1	12	
t_{PZH}	GAB	B	1	13	1	12	ns
t_{PZL}			1	13.5	1	12	
t_{PHZ}	GAB	B	1	7.5	1	7	ns
t_{PLZ}			1	14.5	1	12.5	

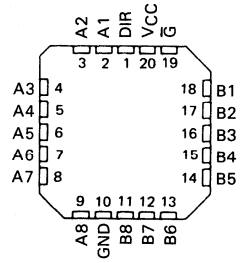
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

- **Bidirectional Octal Bus Transceivers For Driving MOS Devices**
- **I/O Ports Have 25 Ohm Series Resistors So No External Resistors Are Required**
- **Choice of True or Inverting Logic**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS' . . . J PACKAGE
SN74AS' . . . N PACKAGE
SN74AS' . . . DW PACKAGE
(TOP VIEW)



SN54AS' . . . FH OR FK PACKAGE
SN74AS' . . . FN PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed to drive the capacitive input characteristics of MOS devices and allow asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so the buses are effectively isolated.

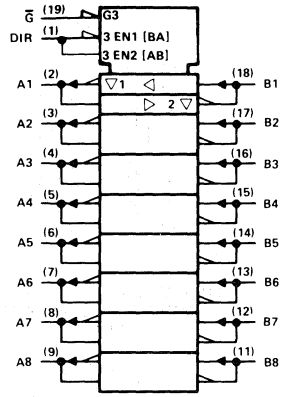
The SN54AS' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS' family is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

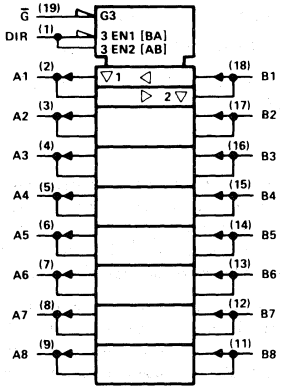
CONTROL INPUTS		OPERATION	
$\overline{G}$	DIR	'AS2640	'AS2645
L	L	$\overline{B}$ data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus
H	X	Isolation	Isolation

logic symbols

'AS2640

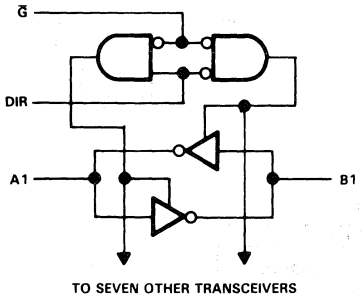


'AS2645

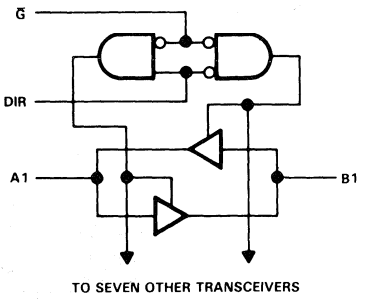


functional block diagrams (positive logic)

'AS2640



'AS2645



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54AS2640, SN54AS2645 . . . . . −55°C to 125°C
SN74AS2640, SN74AS2645 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS2640 SN54AS2645			SN74AS2640 SN74AS2645			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-lvel input voltage			0.8			0.8	V
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS'			SN74AS'			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 1 mA		0.15	0.4		0.15	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.35	0.7		0.35	0.7	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					50			50	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A or B ports‡					−0.5			−0.5	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{OH}		V_{CC} = 4.5 V,	V_O = 2 V	−35			−35			mA
I_{OL}		V_{CC} = 4.5 V,	V_{OL} = 2 V	35			35			mA
I_{CC}	'AS2640	V_{CC} = 5.5 V	Outputs high		37	58		37	58	mA
			Outputs low		78	123		78	123	
			Outputs disabled		51	80		51	80	
	'AS2645		Outputs high		58	95		58	95	
			Outputs low		95	155		95	155	
			Outputs disabled		73	119		73	119	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parametes I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS2640 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS2640		SN74AS2640		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	9.5	1	7.5	ns
t_{PHL}			1	7	1	6.5	
t_{PZH}	$\overline{G}$	A or B	2	11	2	9	ns
t_{PZL}			2	12	2	10	
t_{PHZ}	$\overline{G}$	A or B	1	8	1	7	ns
t_{PLZ}			2	15	2	13	

'AS2645 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS2645		SN74AS2645		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	12	1	10	ns
t_{PHL}			1	11	1	9.5	
t_{PZH}	$\overline{G}$	A or B	1	13	1	11.5	ns
t_{PZL}			1	13	1	10.5	
t_{PHZ}	$\overline{G}$	A or B	1	9	1	8	ns
t_{PLZ}			1	13	1	12	

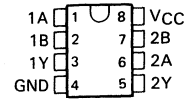
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TYPES SN54ALS8003, SN74ALS8003
DUAL 2-INPUT POSITIVE-NAND GATES

D2746, JULY 1983—REVISED DECEMBER 1983

- **Package Options Include Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability.**

SN54ALS8003 . . . JG PACKAGE
SN74ALS8003 . . . P PACKAGE
(TOP VIEW)



2

description

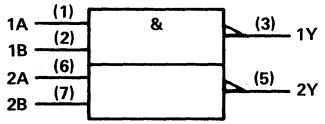
These devices contain two independent 2-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54ALS8003 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS8003 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol



Pin numbers shown are for JG and P packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS8003 . . . . . −55°C to 125°C
SN74ALS8003 . . . . . 0°C to 70°C
Storage temperature . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS8003			SN74ALS8003			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS8003			SN74ALS8003			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.22	0.43		0.22	0.43	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		0.81	1.5		0.81	1.5	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximats one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS8003		SN74ALS8003		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	3	14	3	11	ns
t_{PHL}			2	10	2	8	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

The TTL Data Book
Volume 2

ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.

EXAMPLE: SN 54ALS01 J -00

1. Prefix

MUST CONTAIN TWO TO FOUR LETTERS

SN	Standard Prefix
SNJ	MIL-STD-883 Processed
JANB	MIL-M-38510 Processed

2. Unique Circuit Description

MUST CONTAIN SIX TO TWELVE CHARACTERS

Examples:

54ALS00A
74AS74
74ALS1645A
74ALS1645A-1

3. Package

MUST CONTAIN ONE OR TWO LETTERS

J, JD, JT, JW, N, NT, NW (Dual-in-line packages)†

FH, FK, FE or FN (Chip carriers)

(From pin-connection diagram on individual data sheet)

4. Instructions (Dash No.)

MUST CONTAIN TWO NUMBERS

– 00 No special instructions
– 10 Solder-dipped leads (N and NT packages only)

† These circuits in dual-in-line packages are shipped in one of the carriers shown below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped in the most practical carrier. Please contact your TI sales representative for the method that will best suit your particular needs.

Dual-in-line (J, JD, JT, JW, N, NT, NW)

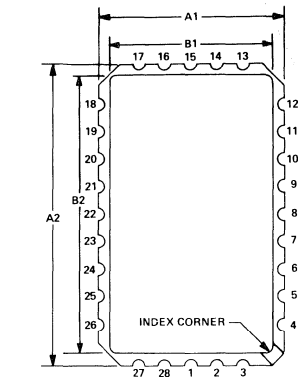
– Slide Magazines
– A-Channel Plastic Tubing
– Barnes Carrier (N only)
– Sectioned Cardboard Box
– Individual Plastic Box

FE ceramic chip carrier packages

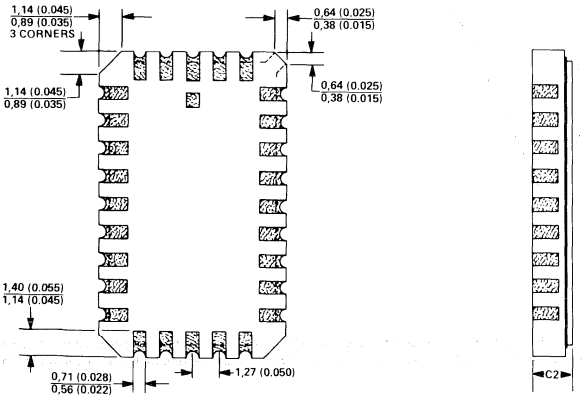
Each of these hermetically sealed leadless chip carrier packages has a metal cap, a 3-layer ceramic base, and a brazed seal. The packages are intended for surface mounting on solder lands on 1,27-mm (0.050-inch) centers. Terminals require no additional cleaning or processing when used in soldered assembly.

RECTANGULAR FE CERAMIC CHIP CARRIER PACKAGE *

(28-terminal package shown)



NUMBER OF TERMINALS	A1		A2		B1		B2		C2	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
28	8,76 (0.345)	9,02 (0.355)	13,84 (0.545)	14,10 (0.555)	7,80 (0.307)	7,95 (0.313)	12,88 (0.507)	13,03 (0.513)	1,65 (0.065)	2,01 (0.079)
32	11,30 (0.445)	11,56 (0.455)	13,84 (0.545)	14,10 (0.555)	10,34 (0.407)	13,03 (0.513)	12,88 (0.507)	13,03 (0.513)	1,65 (0.065)	2,01 (0.079)



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

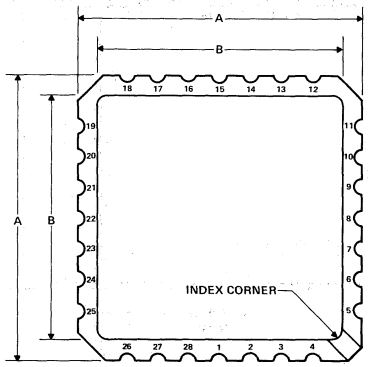
* Memories only!

FH and FK ceramic chip carrier packages

Both versions of these hermetically sealed chip carrier packages have ceramic bases. The FH package has a single-layer base with a ceramic lid and glass seal. The FK package has a three-layer base with a metal lid and braze seal.

The packages are intended for surface mounting on solder lands on 1,27 (0.050-inch) centers. Terminals require no additional cleaning or processing when used in soldered assembly.

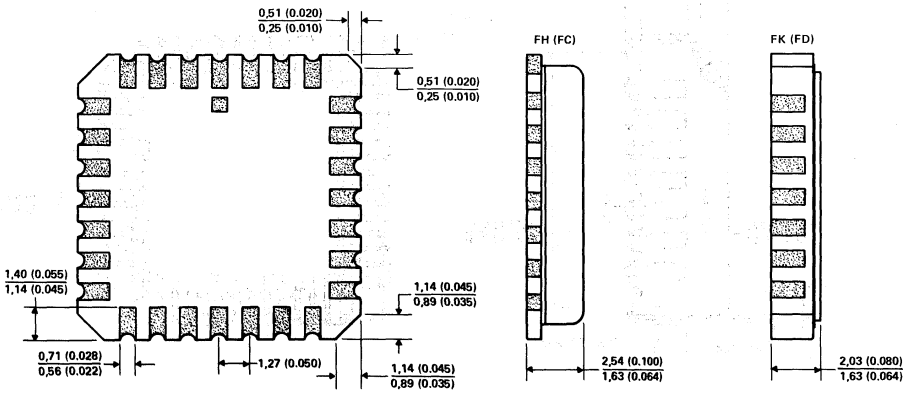
FH AND FK CERAMIC CHIP CARRIER PACKAGES
(28-terminal package shown)



CERAMIC CHIP CARRIERS

JEDEC OUTLINE DESIGNATION*	NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX
MS004CB	20	8,69 (0.342)	9,09 (0.358)	7,80 (0.307)	9,09 (0.358)
MS004CC	28	11,23 (0.422)	11,63 (0.458)	10,31 (0.406)	11,63 (0.458)
MS004CD	44	16,26 (0.640)	16,76 (0.660)	12,58 (0.495)	14,22 (0.560)
MS004CE	52	18,78 (0.739)	19,32 (0.761)	12,58 (0.495)	14,22 (0.560)
MS004CF	68	23,83 (0.938)	24,43 (0.962)	12,6 (0.495)	21,8 (0.862)
MS004CG	84	28,83 (1.135)	29,59 (1.165)	12,6 (0.495)	27,0 (1.065)

*All dimensions and notes for the specified JEDEC outline apply.



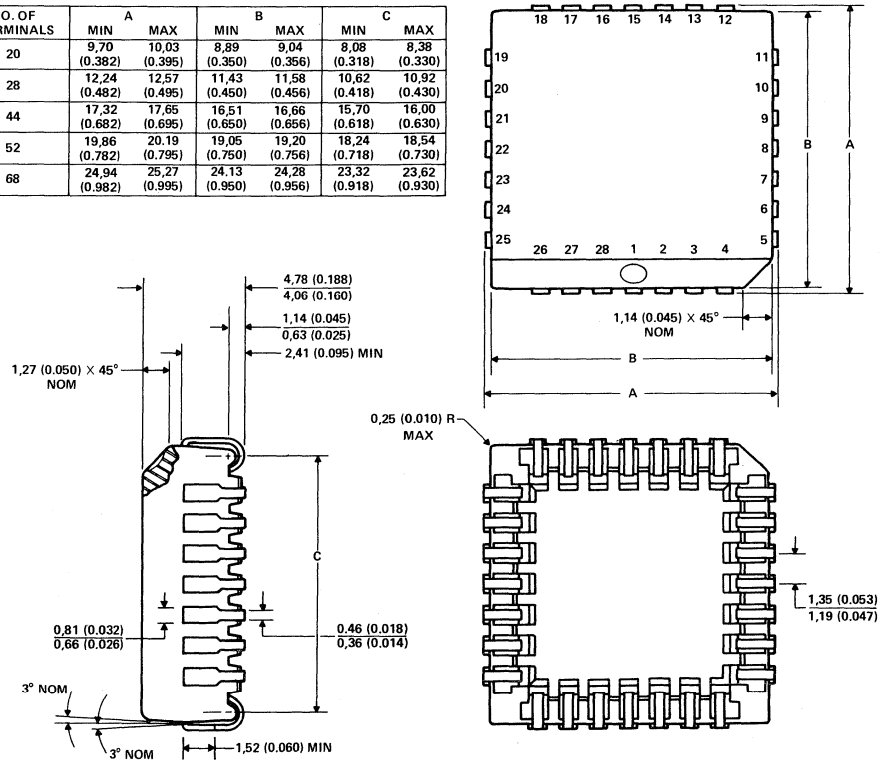
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

FN plastic chip carrier package

Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The packages are intended for surface mounting on solder lands on 1,27-mm (0.050-inch) centers. Leads require no additional cleaning or processing when used in soldered assembly.

FN PLASTIC CHIP CARRIER PACKAGE
(28-terminal package shown)

NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
20	9,70 (0.382)	10,03 (0.395)	8,89 (0.350)	9,04 (0.356)	8,08 (0.318)	8,38 (0.330)
28	12,24 (0.482)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	10,62 (0.418)	10,92 (0.430)
44	17,32 (0.682)	17,65 (0.695)	16,51 (0.650)	16,66 (0.656)	15,70 (0.618)	16,00 (0.630)
52	19,86 (0.782)	20.19 (0.795)	19,05 (0.750)	19,20 (0.756)	18,24 (0.718)	18,54 (0.730)
68	24,94 (0.982)	25,27 (0.995)	24,13 (0.950)	24,28 (0.956)	23,32 (0.918)	23,62 (0.930)

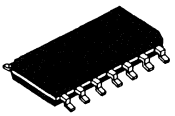


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

D plastic dual-in-line packages (SO package)

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

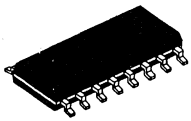
14-PIN
D PACKAGE



NOTES:
1. Body dimensions do not include mold flash.
2. Leads are within 0,25 (0.010) radius of true position at maximum material condition.

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

16-PIN
D PACKAGE



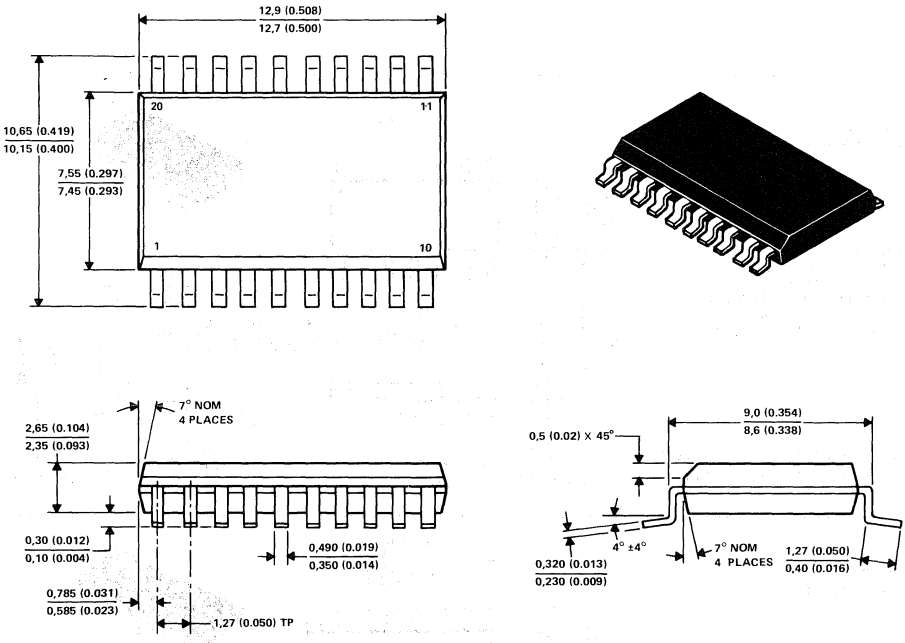
NOTES:
1. Body dimensions do not include mold flash.
2. Leads are within 0,25 (0.010) radius of true position at maximum material condition.

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

DW plastic dual-in-line packages

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

20 PIN PACKAGE
(TENTATIVE SPECIFICATIONS)

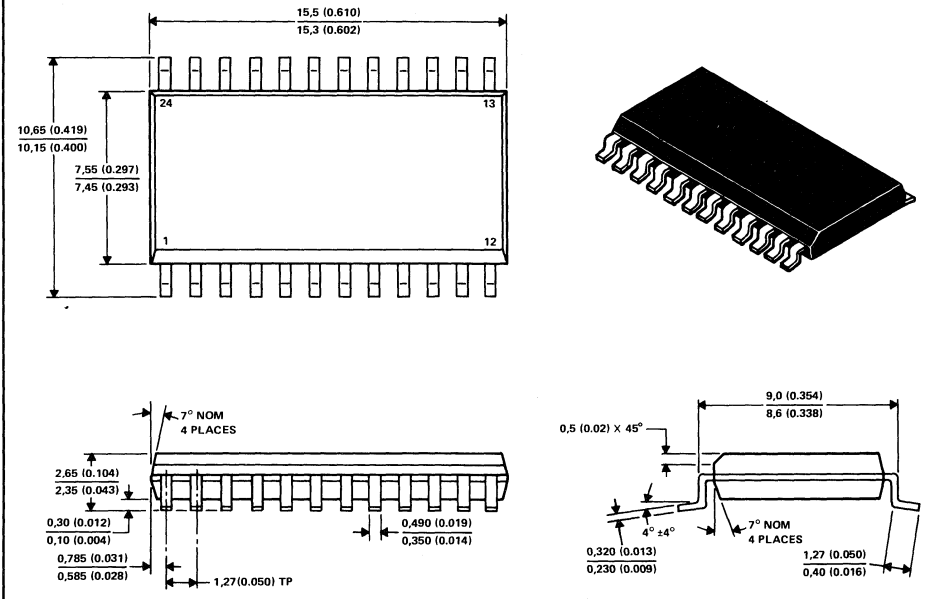


ALL LINEAR DIMENSIONS IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Body dimensions do not include mold flash or protrusion.
B. Mold flash or protrusion shall not exceed 0,15 (0.006).
C. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.

DW plastic dual-in-line packages (continued)

24 PIN PACKAGE
(TENTATIVE SPECIFICATIONS)

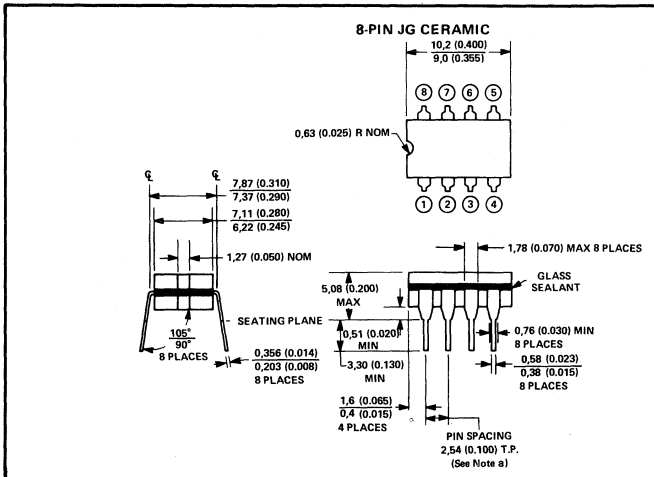


ALL LINEAR DIMENSIONS IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Body dimensions do not include mold flash or protrusion.
B. Mold flash or protrusion shall not exceed 0,15 (0.006).
C. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.

JG ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and 8-lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers (see Note a). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Non-shiny tin-plated leads require no additional cleaning or processing when used in soldered assembly.



NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

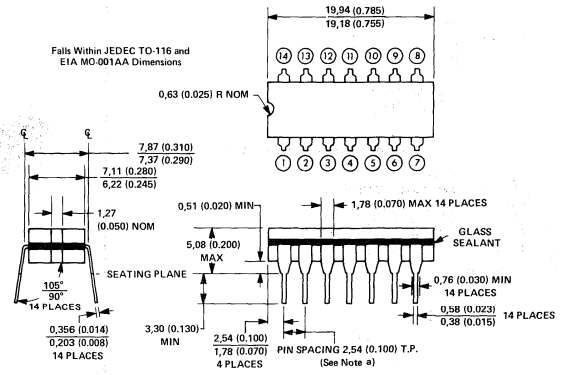
MECHANICAL DATA

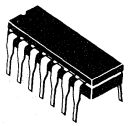
J ceramic packages (including JT and JW dual-in-line and JQ quad-in-line packages)

Each of these hermetically sealed dual-in-line packages consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The JT packages are intended for insertion in mounting-hole rows on 7,62 (0.300) centers, JW packages for mounting-hole rows on 15,24 (0.600) centers, and the JQ quad-in-line package for mounting-hole rows on 15,24 (0.600) and 20,32 (0.800) centers. Once the leads are compressed and inserted sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For the 14-, 16-, and 20-pin packages, the letter J is used by itself since these packages are available only in the 7,62 (0.300) row spacing. For the 24-pin packages, if no second letter or row spacing is specified, the package is assumed to have 15,24 (0.600) row spacing.

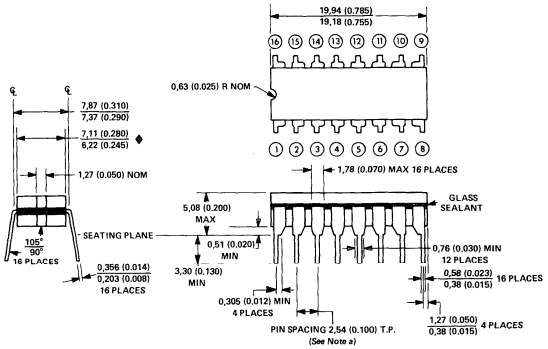
14-PIN J CERAMIC

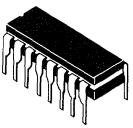




ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

16-PIN J CERAMIC





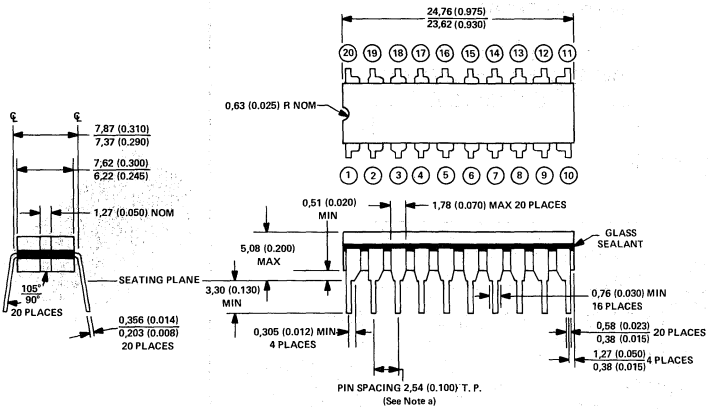
♦ For memories of 64 bits and up and a few MSI/LSI products in Series 54/74 and Series 54S/74S that are derived from memory circuit bars, this maximum is 7,62 (0.300). All other dimensions apply without modification.

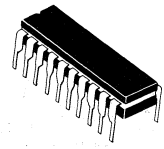
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

J ceramic dual-in-line packages (continued)

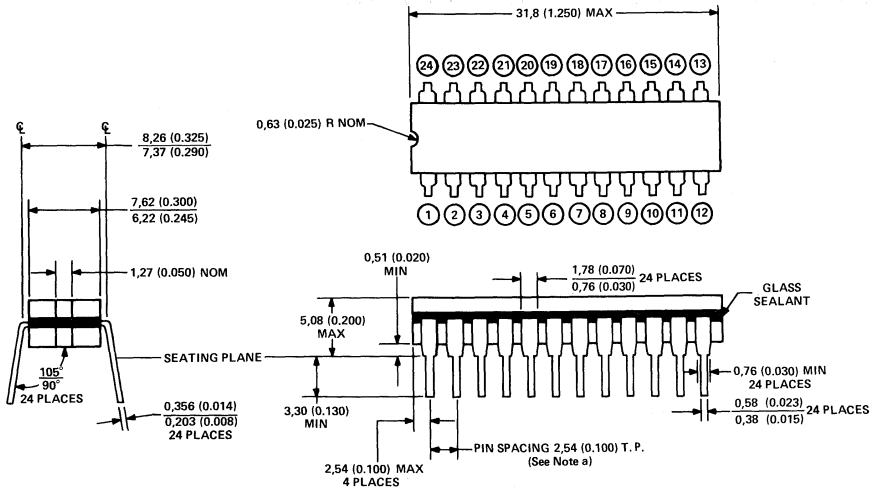
20-PIN J CERAMIC





ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

24-PIN JT CERAMIC, 0.300-INCH ROW SPACING

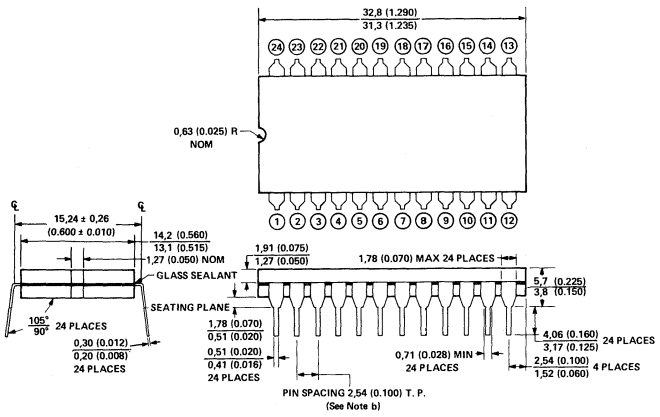


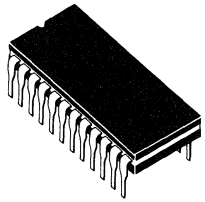
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

J ceramic dual-in-line packages (continued)

24-PIN JW CERAMIC





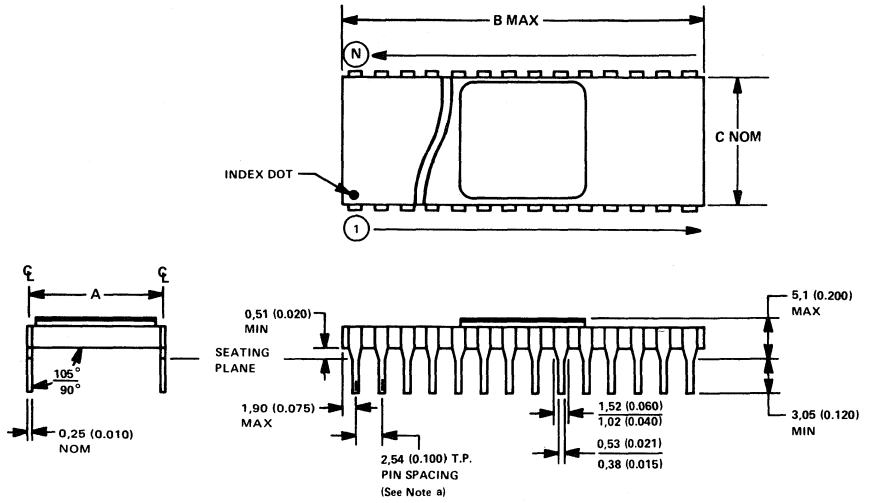
Falls within JEDEC MO-015AA dimensions

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

ceramic packages – side-braze (JD suffix)

This is a hermetically sealed ceramic package with a metal cap and side-brazed tin-plated leads.



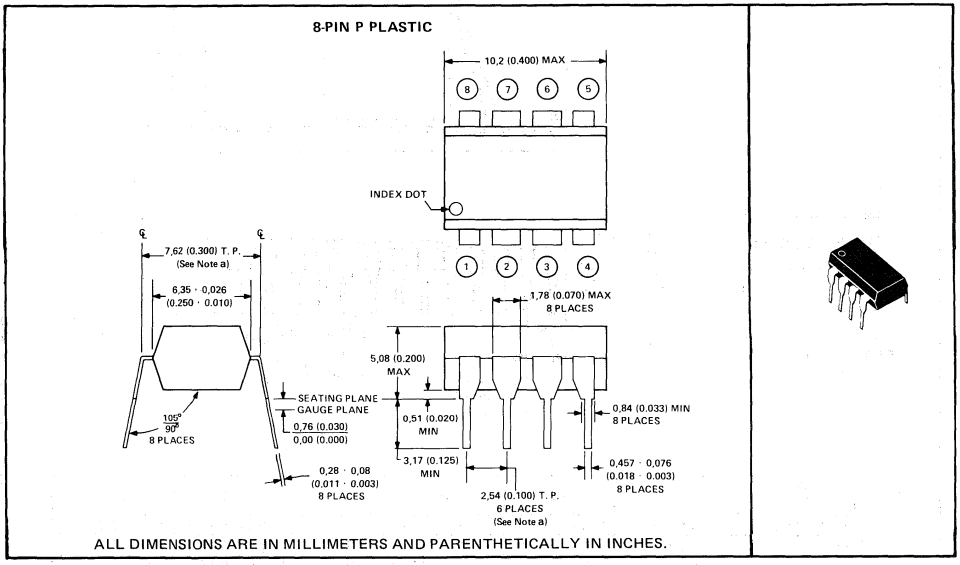
DIM \ PINS	24	28	40	48	52	64
A ± 0,25 (0.010)	15,24 (0.600)	15,24 (0.600)	15,24 (0.600)	15,24 (0.600)	15,24 (0.600)	22,86 (0.900)
B MAX	31,8 (1.25)	36,8 (1.45)	52,1 (2.05)	62,2 (2.45)	67,3 (2.65)	82,6 (3.25)
C NOM	15,0 (0.590)	15,0 (0.590)	15,0 (0.590)	15,0 (0.590)	15,0 (0.590)	22,6 (0.890)

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

P plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on an 8-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62-mm (0.300) centers (see Note a). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Solder-plated leads require no additional cleaning or processing when used in soldered assembly.

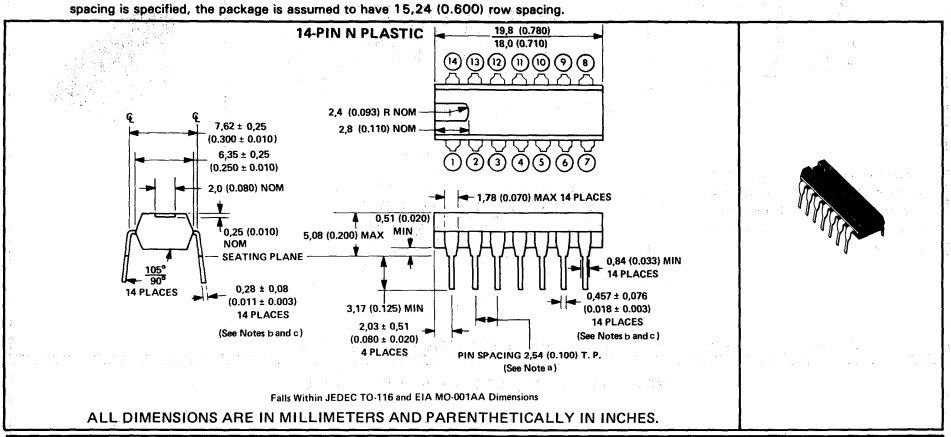


NOTE: a. Each pin is within 0,13 (0.0005) radius of true position (TP) at the gauge plane with maximum material condition and unit installed.

N plastic packages (including NT and NW dual-in-packages)

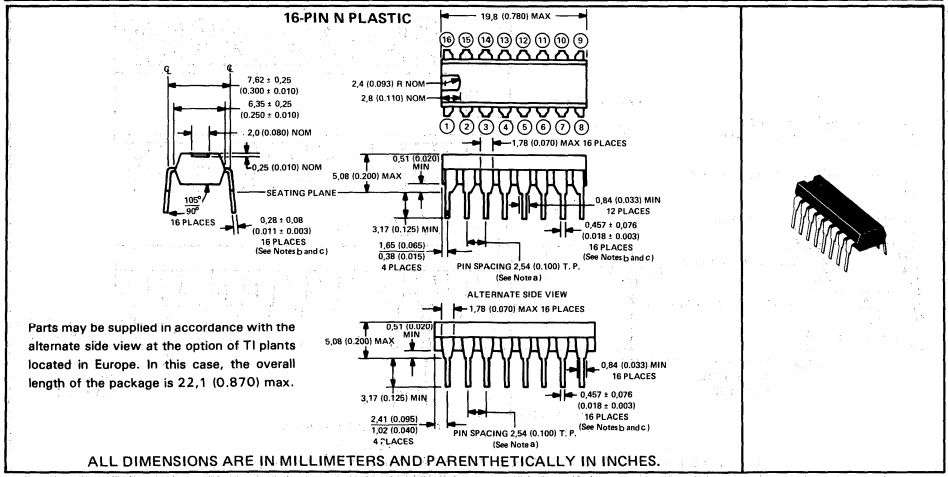
Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300) centers for the NT packages and on 15,24 (0.600) centers for the NW packages. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For the 14-, 16-, 20-, and 28-pin packages, the letter N is used by itself since these packages are available in only one row-spacing width – 7,62 (0.300) for the 14-, 16-, 18-, and 20-pin packages and 15,24 (0.600) for the 28-pin package. For the 24-pin package, if no second letter or row spacing is specified, the package is assumed to have 15,24 (0.600) row spacing.



Falls Within JEDEC TO-116 and EIA MO-001AA Dimensions

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.



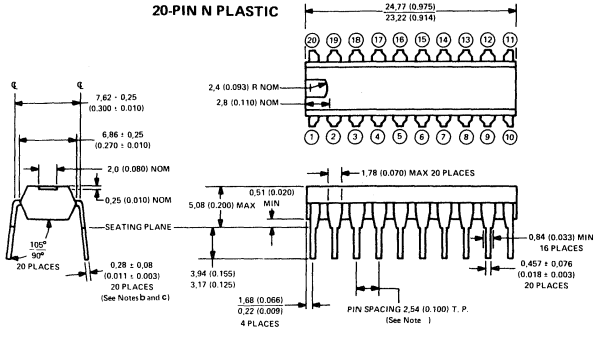
Parts may be supplied in accordance with the alternate side view at the option of TI plants located in Europe. In this case, the overall length of the package is 22,1 (0.870) max.

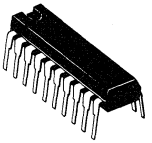
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTES: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
b. This dimension does not apply for solder-dipped leads.
c. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N plastic dual-in-line packages (continued)

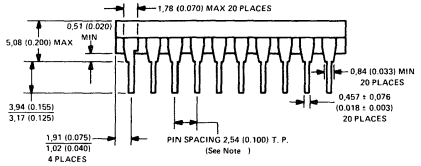
20-PIN N PLASTIC





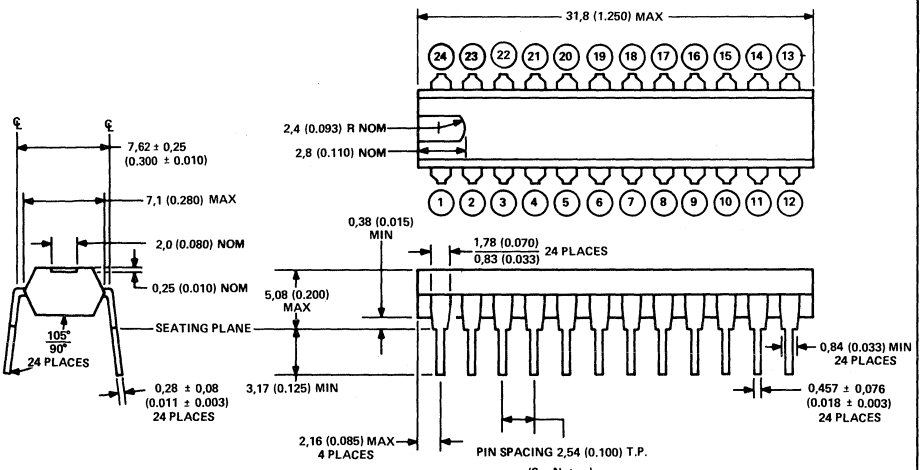
Parts may be supplied in accordance with the alternate side view at the option of TI plants located in Europe. In this case, the overall length of the package is 26,7 (1.050) max.

ALTERNATE SIDE VIEW



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

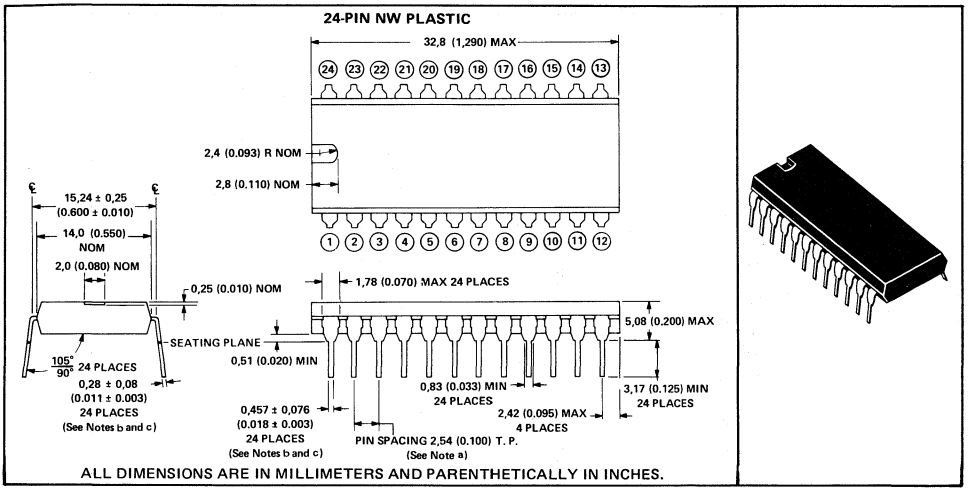
24-PIN NT PLASTIC, 0.300-INCH ROW SPACING



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

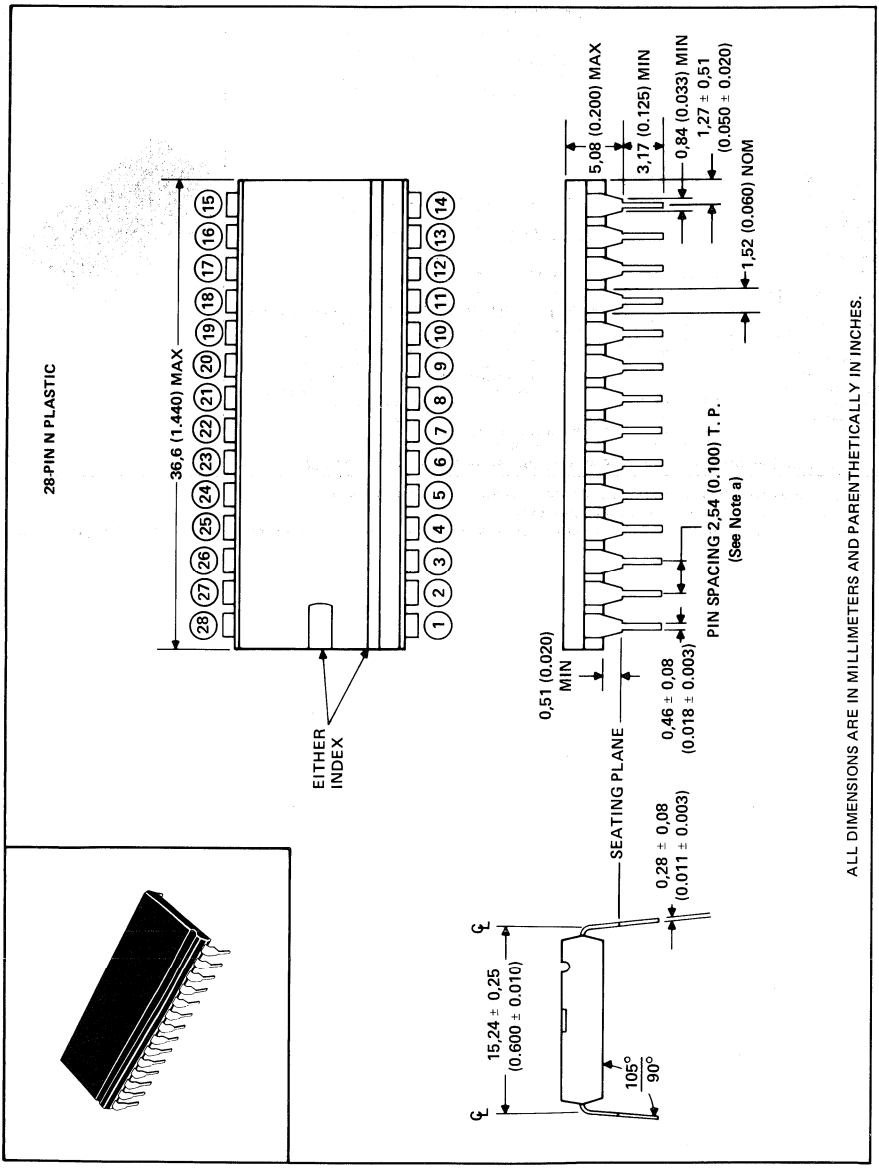
NOTES: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
b. This dimension does not apply for solder-dipped leads.
c. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N plastic dual-in-line packages (continued)



NOTES: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
b. This dimension does not apply for solder-dipped leads.
c. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

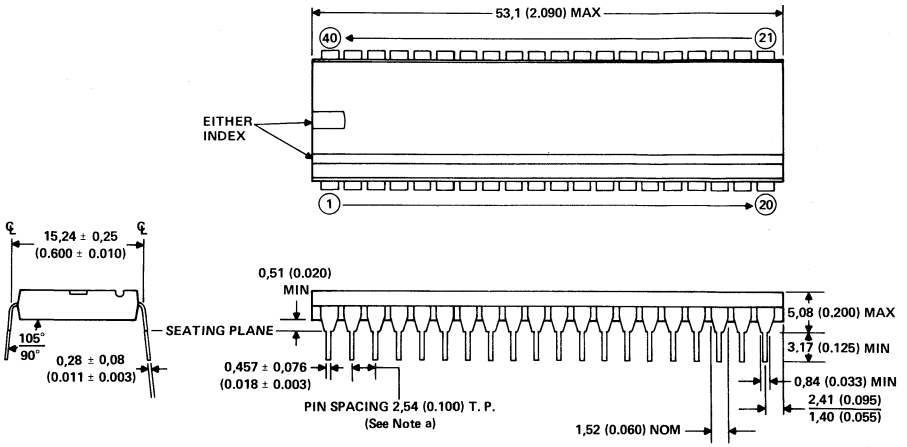
N plastic packages (continued)



NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

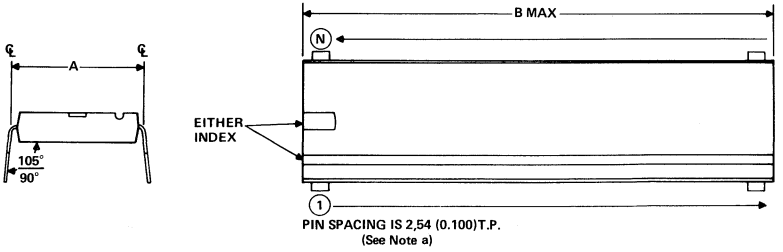
N plastic packages (continued)

40-PIN N PLASTIC



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

48-PIN, 52-PIN, AND 64-PIN N PLASTIC



DIM \ PINS	48	52	64
A ± 0,25 (0.010)	15,24 (0.600)	15,24 (0.600)	22,86 (0.900)
B MAX	62,2 (2.45)	67,3 (2.65)	81,3 (3.20)

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

The TTL Data Book
Volume 2

Overview of IEEE Standard 91-1984

Explanation of Logic Symbols

F.A. Mann
Semiconductor Group

Contents

4

If you have questions on this Explanation of New Logic Symbols, Please contact:

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IEEE Standards may be purchased from:

Institute of Electrical and Electronics Engineers, Inc.
345 East 47th Street
New York, N.Y. 10017

International Electrotechnical Commission (IEC) publications may be purchased from:

American National Standards Institute, Inc.
1430 Broadway
New York, N.Y. 10018

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1.0 INTRODUCTION

The International Electrotechnical Commission (IEC) has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic circuit to each output without showing explicitly the internal logic. At the heart of the system is dependency notation, which will be explained in Section 4.

The system was introduced in the USA in a rudimentary form in IEEE/ANSI Standard Y32.14-1973. Lacking at that time a complete development of dependency notation, it offered little more than a substitution of rectangular shapes for the familiar distinctive shapes for representing the basic functions of AND, OR, negation, etc. This is no longer the case.

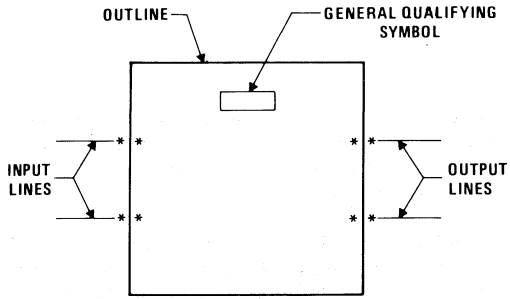
Internationally, Working Group 2 of IEC Technical Committee TC-3 has prepared a new document (Publication 617-12) that consolidates the original work started in the mid 1960's and published in 1972 (Publication 117-15) and the amendments and supplements that have followed. Similarly for the USA, IEEE Committee SCC 11.9 has revised the publication IEEE Std 91/ANSI Y32.14. Now numbered simply IEEE Std 91-1984, the IEEE standard contains all of the IEC work that has been approved, and also a small amount of material still under international consideration. Texas Instruments is participating in the work of both organizations and this document introduces new logic symbols in accordance with the new standards. When changes are made as the standards develop, future editions will take those changes into account.

The following explanation of the new symbolic language is necessarily brief and greatly condensed from what the standards publications will contain. This is not intended to be sufficient for those people who will be developing symbols for new devices. It is primarily intended to make possible the understanding of the symbols used in various data books and the comparison of the symbols with logic diagrams, functional block diagrams, and/or function tables will further help that understanding.

2.0 SYMBOL COMPOSITION

A symbol comprises an outline or a combination of outlines together with one or more qualifying symbols. The shape of the symbols is not significant. As shown in Figure 1, general qualifying symbols are used to tell exactly what logical operation is performed by the elements. Table I shows general qualifying symbols defined in the new standards. Input lines are placed on the left and output lines are placed on the right. When an exception is made to that convention, the direction of signal flow is indicated by an arrow as shown in Figure 11.

All outputs of a single, unsubdivided element always have identical internal logic states determined by the function of the element except when otherwise indicated by an associated qualifying symbol or label inside the element.



*Possible positions for qualifying symbols relating to inputs and outputs

Figure 1. Symbol Composition

The outlines of elements may be abutted or embedded in which case the following conventions apply. There is no logic connection between the elements when the line common to their outlines is in the direction of signal flow. There is at least one logic connection between the elements when the line common to their outlines is perpendicular to the direction of signal flow. The number of logic connections between elements will be clarified by the use of qualifying symbols and this is discussed further under that topic. If no indications are shown on either side of the common line, it is assumed there is only one connection.

When a circuit has one or more inputs that are common to more than one element of the circuit, the common-control block may be used. This is the only distinctively shaped outline used in the IEC system. Figure 2 shows that unless otherwise qualified by dependency notation, an input to the common-control block is an input to each of the elements below the common-control block.

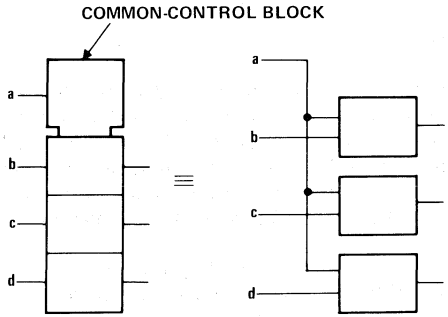


Figure 2. Common-Control Block

A common output depending on all elements of the array can be shown as the output of a common-output element. Its distinctive visual feature is the double line at its top. In addition the common-output element may have other inputs as shown in Figure 3. The function of the common-output element must be shown by use of a general qualifying symbol.

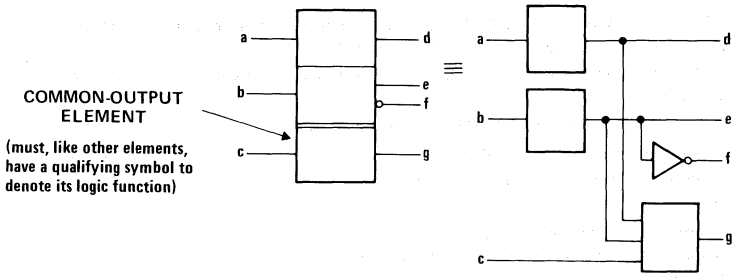


Figure 3. Common-Output Element

3.0 QUALIFYING SYMBOLS

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3.1 General Qualifying Symbols

Table I shows general qualifying symbols defined by IEEE Standard 91. These characters are placed near the top center or the geometric center of a symbol or symbol element to define the basic function of the device represented by the symbol or of the element.

3.2 Qualifying Symbols for Inputs and Outputs

Qualifying symbols for inputs and outputs are shown in Table II and will be familiar to most users with the possible exception of the logic polarity and analog signal indicators. The older logic negation indicator means that the external 0 state produces the internal 1 state. The internal 1 state means the active state. Logic negation may be used in pure logic diagrams; in order to tie the external 1 and 0 logic states to the levels H (high) and L (low), a statement of whether positive logic (1 = H, 0 = L) or negative logic (1 = L, 0 = H) is being used is required or must be assumed. Logic polarity indicators eliminate the need for calling out the logic convention and are used in various data books in the symbology for actual devices. The presence of the triangular polarity indicator indicates that the L logic level will produce the internal 1 state (the active state) or that, in the case of an output, the internal 1 state will produce the external L level. Note how the active direction of transition for a dynamic input is indicated in positive logic, negative logic, and with polarity indication.

The internal connections between logic elements abutted together in a symbol may be indicated by the symbols shown in Table II. Each logic connection may be shown by the presence of qualifying symbols at one or both sides of the common line and if confusion can arise about the numbers of connections, use can be made of one of the internal connection symbols.

EXPLANATION OF NEW LOGIC SYMBOLS

Table I. General Qualifying Symbols

SYMBOL	DESCRIPTION	CMOS EXAMPLE	TTL EXAMPLE
&	AND gate or function.	'HC00	SN7400
≥1	OR gate or function. The symbol was chosen to indicate that at least one active input is needed to activate the output.	'HC02	SN7402
=1	Exclusive OR. One and only one input must be active to activate the output.	'HC86	SN7486
=	Logic identity. All inputs must stand at the same state.	'HC86	SN74180
2k	An even number of inputs must be active.	'HC280	SN74180
2k+1	An odd number of inputs must be active.	'HC86	SN74ALS86
1	The one input must be active.	'HC04	SN7404
▷ or ◁	A buffer or element with more than usual output capability (symbol is oriented in the direction of signal flow).	'HC240	SN74S436
⊓	Schmitt trigger; element with hysteresis.	'HC132	SN74LS18
X/Y	Coder, code converter (DEC/BCD, BIN/OUT, BIN/7-SEG, etc.).	'HC42	SN74LS347
MUX	Multiplexer/data selector.	'HC151	SN74150
DMUX or DX	Demultiplexer.	'HC138	SN74138
Σ	Adder.	'HC283	SN74LS385
P−Q	Subtracter.	*	SN74LS385
CPG	Look-ahead carry generator	'HC182	SN74182
π	Multiplier.	*	SN74LS384
COMP	Magnitude comparator.	'HC85	SN74LS682
ALU	Arithmetic logic unit.	'HC181	SN74LS381
⎍	Retriggerable monostable.	'HC123	SN74LS422
1⎍	Nonretriggerable monostable (one-shot)	'HC221	SN74121
G ⎍	Astable element. Showing waveform is optional.	*	SN74LS320
!G ⎍	Synchronously starting astable.	*	SN74LS624
G! ⎍	Astable element that stops with a completed pulse.	*	*
SRGm	Shift register. m = number of bits.	'HC164	SN74LS595
CTRm	Counter. m = number of bits; cycle length = 2^m.	'HC590	SN54LS590
CTR DIVm	Counter with cycle length = m.	'HC160	SN74LS668
RCTRm	Asynchronous (ripple-carry) counter; cycle length = 2^m.	'HC4020	*
ROM	Read-only memory.	*	SN74187
RAM	Random-access read/write memory.	'HC189	SN74170
FIFO	First-in, first-out memory.	*	SN74LS222
I=0	Element powers up cleared to 0 state.	*	SN74AS877
I=1	Element powers up set to 1 state.	'HC7022	SN74AS877
Φ	Highly complex function; "gray box" symbol with limited detail shown under special rules.	*	SN74LS608

*Not all of the general qualifying symbols have been used in TI's CMOS and TTL data books, but they are included here for the sake of completeness.

Table II. Qualifying Symbols for Inputs and Outputs

Logic negation at input. External 0 produces internal 1.

Logic negation at output. Internal 1 produces external 0.

Active-low input. Equivalent to  in positive logic.

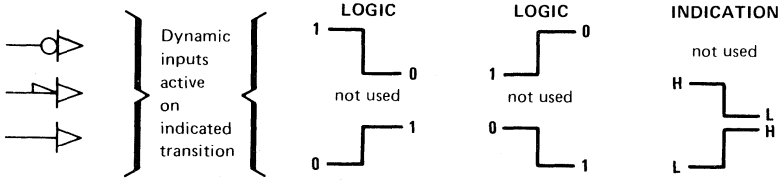
Active-low output. Equivalent to  in positive logic.

Active-low input in the case of right-to-left signal flow.

Active-low output in the case of right-to-left signal flow.

Signal flow from right to left. If not otherwise indicated, signal flow is from left to right.

Bidirectional signal flow.



Nonlogic connection. A label inside the symbol will usually define the nature of this pin.

Input for analog signals (on a digital symbol) (see Figure 14).

Input for digital signals (on an analog symbol) (see Figure 14).

Internal connection. 1 state on left produces 1 state on right.

Negated internal connection. 1 state on left produces 0 state on right.

Dynamic internal connection. Transition from 0 to 1 on left produces transitory 1 state on right.

Internal input (virtual input). It always stands at its internal 1 state unless affected by an overriding dependency relationship.

Internal output (virtual output). Its effect on an internal input to which it is connected is indicated by dependency notation.

The internal (virtual) input is an input originating somewhere else in the circuit and is not connected directly to a terminal. The internal (virtual) output is likewise not connected directly to a terminal. The application of internal inputs and outputs requires an understanding of dependency notation, which is explained in Section 4.

Table III. Symbols Inside the Outline

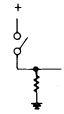
Postponed output (of a pulse-triggered flip-flop). The output changes when input initiating change (e.g., a C input) returns to its initial external state or level. See § 5.

Bi-threshold input (input with hysteresis).

N-P-N open-collector or similar output that can supply a relatively low-impedance L level when not turned off. Requires external pull-up. Capable of positive-logic wired-AND connection.

Passive-pull-up output is similar to N-P-N open-collector output but is supplemented with a built-in passive pull-up.

N-P-N open-emitter or similar output that can supply a relatively low-impedance H level when not turned off. Requires external pull-down. Capable of positive-logic wired-OR connection.



Passive-pull-down output is similar to N-P-N open-emitter output but is supplemented with a built-in passive pull-down.

3-state output.

Output with more than usual output capability (symbol is oriented in the direction of signal flow).

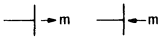
Enable input

When at its internal 1-state, all outputs are enabled.
When at its internal 0-state, open-collector and open-emitter outputs are off, three-state outputs are at normally defined internal logic states and at external high-impedance state, and all other outputs (e.g., totem-poles) are at the internal 0-state.

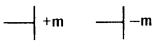
J, K, R, S, T

Usual meanings associated with flip-flops (e.g., R = reset, T = toggle)

Data input to a storage element equivalent to:



Shift right (left) inputs, m = 1, 2, 3, etc. If m = 1, it is usually not shown.



Counting up (down) inputs, m = 1, 2, 3, etc. If m = 1, it is usually not shown.

Binary grouping. m is highest power of 2.

The contents-setting input, when active, causes the content of a register to take on the indicated value.

The content output is active if the content of the register is as indicated.

Input line grouping . . . indicates two or more terminals used to implement a single logic input.

e.g., The paired expander inputs of SN7450.

Fixed-state output always stands at its internal 1 state. For example, see SN74185.

In an array of elements, if the same general qualifying symbol and the same qualifying symbols associated with inputs and outputs would appear inside each of the elements of the array, these qualifying symbols are usually shown only in the first element. This is done to reduce clutter and to save time in recognition. Similarly, large identical elements that are subdivided into smaller elements may each be represented by an unsubdivided outline. The SN54HC242 or SN54LS440 symbol illustrates this principle.

3.3 Symbols Inside the Outline

Table III shows some symbols used inside the outline. Note particularly that open-collector (open-drain), open-emitter (open-source), and three-state outputs have distinctive symbols. Also note that an EN input affects all of the outputs of the circuit and has no effect on inputs. When an enable input affects only certain outputs and/or affects one or more inputs, a form of dependency notation will indicate this (see 4.9). The effects of the EN input on the various types of outputs are shown.

It is particularly important to note that a D input is always the data input of a storage element. At its internal 1 state, the D input sets the storage element to its 1 state, and at its internal 0 state it resets the storage element to its 0 state.

The binary grouping symbol will be explained more fully in Section 8. Binary-weighted inputs are arranged in order and the binary weights of the least-significant and the most-significant lines are indicated by numbers. In this document weights of input and output lines will be represented by powers of two usually only when the binary grouping symbol is used, otherwise decimal numbers will be used. The grouped inputs generate an internal number on which a mathematical function can be performed or that can be an identifying number for dependency notation (Figure 28). A frequent use is in addresses for memories.

Reversed in direction, the binary grouping symbol can be used with outputs. The concept is analogous to that for the inputs and the weighted outputs will indicate the internal number assumed to be developed within the circuit.

Other symbols are used inside the outlines in accordance with the IEC/IEEE standards but are not shown here. Generally these are associated with arithmetic operations and are self-explanatory.

When nonstandardized information is shown inside an outline, it is usually enclosed in square brackets [like these].

4.0 DEPENDENCY NOTATION

4.1 General Explanation

Dependency notation is the powerful tool that sets the IEC symbols apart from previous systems and makes compact, meaningful, symbols possible. It provides the means of denoting the relationship between inputs, outputs, or inputs and outputs without actually showing all the elements and interconnections involved. The information provided by dependency notation supplements that provided by the qualifying symbols for an element's function.

In the convention for the dependency notation, use will be made of the terms "affecting" and "affected." In cases where it is not evident which inputs must be considered as being the affecting or the affected ones (e.g., if they stand in an AND relationship), the choice may be made in any convenient way.

So far, eleven types of dependency have been defined and all of these are used in various TI data books. X dependency is used mainly with CMOS circuits. They are listed below in the order in which they are presented and are summarized in Table IV following 4.12.

Section	Dependency Type or Other Subject
4.2	G, AND
4.3	General Rules for Dependency Notation
4.4	V, OR
4.5	N, Negate (Exclusive-OR)
4.6	Z, Interconnection
4.7	X, Transmission
4.8	C, Control
4.9	S, Set and R, Reset
4.10	EN, Enable
4.11	M, Mode
4.12	A, Address

4.2 G (AND) Dependency

A common relationship between two signals is to have them ANDed together. This has traditionally been shown by explicitly drawing an AND gate with the signals connected to the inputs of the gate. The 1972 IEC publication and the 1973 IEEE/ANSI standard showed several ways to show this AND relationship using dependency notation. While ten other forms of dependency have since been defined, the ways to invoke AND dependency are now reduced to one.

In Figure 4 input **b** is ANDed with input **a** and the complement of **b** is ANDed with **c**. The letter G has been chosen to indicate AND relationships and is placed at input **b**, inside the symbol. A number considered appropriate by the symbol designer (1 has been used here) is placed after the letter G and also at each affected input. Note the bar over the 1 at input **c**.

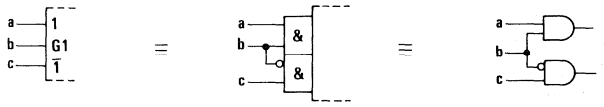


Figure 4. G Dependency Between Inputs

In Figure 5, output **b** affects input **a** with an AND relationship. The lower example shows that it is the internal logic state of **b**, unaffected by the negation sign, that is ANDed. Figure 6 shows input **a** to be ANDed with a dynamic input **b**.

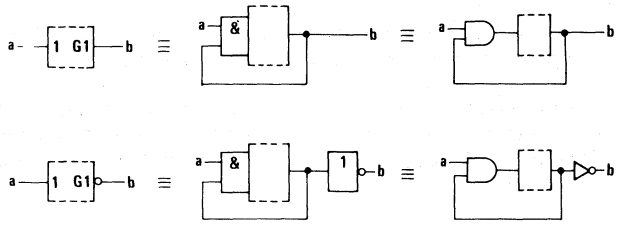


Figure 5. G Dependency Between Outputs and INputs

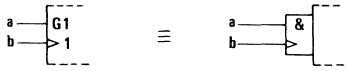


Figure 6. G Dependency with a Dynamic Input

The rules for G dependency can be summarized thus:

When a G*m* input or output (*m* is a number) stands at its internal 1 state, all inputs and outputs affected by G*m* stand at their normally defined internal logic states. When the G*m* input or output stands at its 0 state, all inputs and outputs affected by G*m* stand at their internal 0 states.

4

4.3 Conventions for the Application of Dependency Notation in General

The rules for applying dependency relationships in general follow the same pattern as was illustrated for G dependency.

Application of dependency notation is accomplished by:

1) labeling the input (or output) *affecting* other inputs or outputs with the letter symbol indicating the relationship involved (e.g., G for AND) followed by an identifying number, appropriately chosen, and
2) labeling each input or output *affected* by that affecting input (or output) with that same number.

If it is the complement of the internal logic state of the affecting input or output that does the affecting, then a bar is placed over the identifying numbers at the affected inputs or outputs (Figure 4).

If two affecting inputs or outputs have the same letter and same identifying number, they stand in an OR relationship to each other (Figure 7).

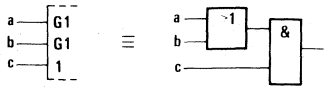


Figure 7. ORed Affecting Inputs

If the affected input or output requires a label to denote its function (e.g., "D"), this label will be *prefixed* by the identifying number of the affecting input (Figure 15).

If an input or output is affected by more than one affecting input, the identifying numbers of each of the affecting inputs will appear in the label of the affected one, separated by commas. The normal reading order of these numbers is the same as the sequence of the affecting relationships (Figure 15).

If the labels denoting the functions of affected inputs or outputs must be numbers (e.g., outputs of a coder), the identifying numbers to be associated with both affecting inputs and affected inputs or outputs will be replaced by another character selected to avoid ambiguity, e.g., Greek letters (Figure 8).

Figure 8. Substitution for Numbers

4.4 V (OR) Dependency

The symbol denoting OR dependency is the letter V (Figure 9).

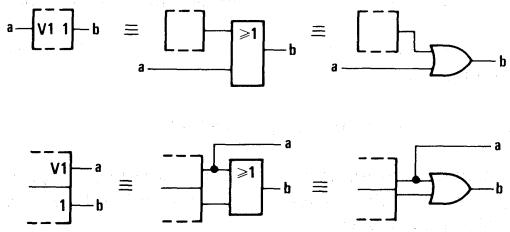
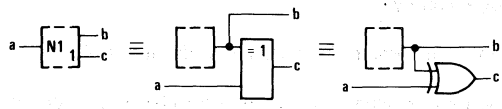


Figure 9. V (OR) Dependency

When a V*m* input or output stands at its internal 1 state, all inputs and outputs affected by V*m* stand at their internal 1 states. When the V*m* input or output stands at its internal 0 state, all inputs and outputs affected by V*m* stand at their normally defined internal logic states.

4.5 N (Negate) (Exclusive-OR) Dependency

The symbol denoting negate dependency is the letter N (Figure 10). Each input or output affected by an N*m* input or output stands in an Exclusive-OR relationship with the N*m* input or output.



If a = 0, then c = b
If a = 1, then c = b

Figure 10. N (Negate) (Exclusive-OR) Dependency

When an N*m* input or output stands at its internal 1 state, the internal logic state of each input and each output affected by N*m* is the complement of what it would otherwise be. When an N*m* input or output stands at its internal 0 state, all inputs and outputs affected by N*m* stand at their normally defined internal logic states.

4.6 Z (Interconnection) Dependency

The symbol denoting interconnection dependency is the letter Z.

4

Interconnection dependency is used to indicate the existence of internal logic connections between inputs, outputs, internal inputs, and/or internal outputs.

The internal logic state of an input or output affected by a Z*m* input or output will be the same as the internal logic state of the Z*m* input or output, unless modified by additional dependency notation (Figure 11).

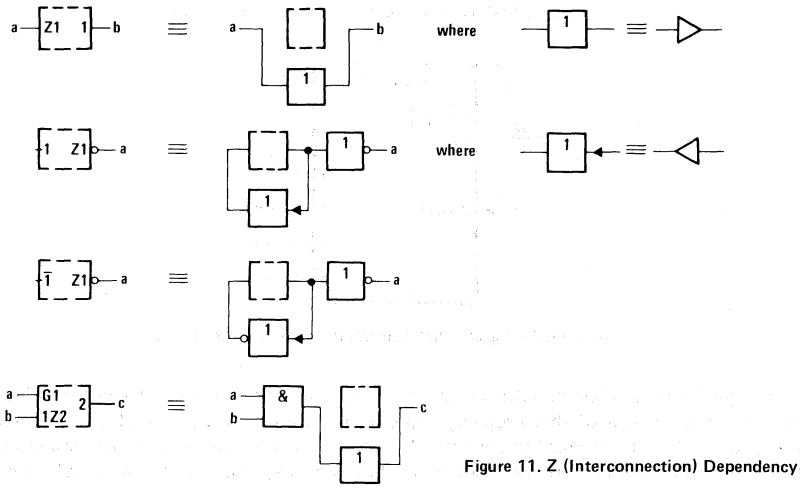
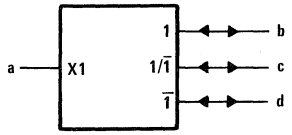


Figure 11. Z (Interconnection) Dependency

4.7 X (Transmission) Dependency

The symbol denoting transmission dependency is the letter X.

Transmission dependency is used to indicate controlled bidirectional connections between affected input/output ports (Figure 12).



If a = 1, there is a bidirectional connection between b and c.

If a = 0, there is a bidirectional connection between c and d.

Figure 12. X (Transmission) Dependency

When an X*m* input or output stands at its internal 1 state, all input-output ports affected by this X*m* input or output are bidirectionally connected together and stand at the same internal logic state or analog signal level. When an X*m* input or output stands at its internal 0 state, the connection associated with this set of dependency notation does not exist.

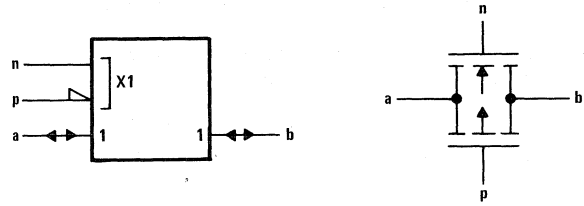


Figure 13. CMOS Transmission Gate Symbol and Schematic

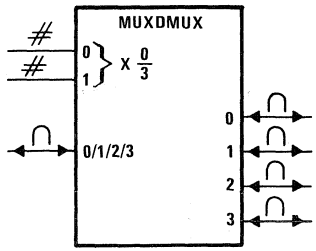


Figure 14. Analog Data Selector (Multiplexer/Demultiplexer)

Although the transmission paths represented by X dependency are inherently bidirectinal, use is not always made of this property. This is analogous to a piece of wire, which may be constrained to carry current in only one direction. If this is the case in a particular application, then the directional arrows shown in Figures 12, 13, and 14 would be omitted.

4.8 C (Control) Dependency

The symbol denoting control dependency is the letter C.

Control inputs are usually used to enable or disable the data (D, J, K, R, or S) inputs of storage elements. They may take on their internal 1 states (be active) either statically or dynamically. In the latter case the dynamic input symbol is used as shown in the third example of Figure 15.

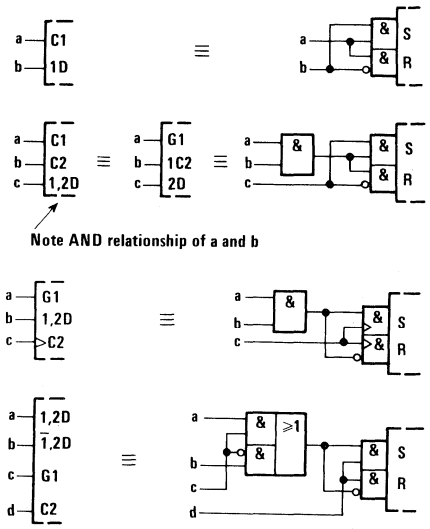


Figure 15. C (Control) Dependency

When a C*m* input or output stands at its internal 1 state, the inputs affected by C*m* have their normally defined effect on the function of the element, i.e., these inputs are enabled. When a C*m* input or output stands at its internal 0 state, the inputs affected by C*m* are disabled and have no effect on the function of the element.

4.9 S (Set) and R (Reset) Dependencies

The symbol denoting set dependency is the letter S. The symbol denoting reset dependency is the letter R.

Set and reset dependencies are used if it is necessary to specify the effect of the combination R = S = 1 on a bistable element. Case 1 in Figure 16 does not use S or R dependency.

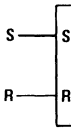
When an S*m* input is at its internal 1 state, outputs affected by the S*m* input will react, regardless of the state of an R input, as they normally would react to the combination S = 1, R = 0. See cases 2, 4, and 5 in Figure 16.

When an R*m* input is at its internal 1 state, outputs affected by the R*m* input will react, regardless of the state of an S input, as they normally would react to the combination S = 0, R = 1. See cases 3, 4, and 5 in Figure 16.

When an S*m* or R*m* input is at its internal 0 state, it has no effect.

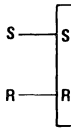
Note that the noncomplementary output patterns in cases 4 and 5 are only pseudo stable. The simultaneous return of the inputs to S = R = 0 produces an unforeseeable stable and complementary output pattern.

CASE 1



S	R	Q	Q̄
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	?	?

CASE 2

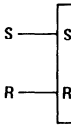


S	R	Q	Q̄
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	1	0

CASE 3

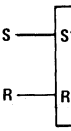
S	R	Q	Q̄
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	0	1

CASE 4



S	R	Q	Q̄
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	1	1

CASE 5



S	R	Q	Q̄
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	0	0

0 = external 0 state
1 = external 1 state
nc = no change
? = unspecified

Figure 16. S (Set) and R (Reset) Dependencies

4.10 EN (Enable) Dependency

The symbol denoting enable dependency is the combination of letters EN.

An EN*m* input has the same effect on outputs as an EN input, see 3.1, but it affects only those outputs labeled with the identifying number *m*. It also affects those inputs labeled with the identifying number *m*. By contrast, an EN input affects all outputs and no inputs. The effect of an EN*m* input on an affected input is identical to that of a C*m* input (Figure 17).

When an EN*m* input stands at its internal 1 state, the inputs affected by EN*m* have their normally defined effect on the function of the element and the outputs affected by this input stand at their normally defined internal logic states, i.e., these inputs and outputs are enabled.

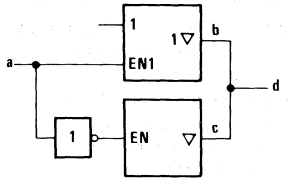


Figure 17. EN (Enable) Dependency

When an EN*m* input stands at its internal 0 state, the inputs affected by EN*m* are disabled and have no effect on the function of the element, and the outputs affected by EN*m* are also disabled. Open-collector outputs are turned off, three-state outputs stand at their normally defined internal logic states but externally exhibit high impedance, and all other outputs (e.g., totem-pole outputs) stand at their internal 0 states.

4

4.11 M (MODE) Dependency

The symbol denoting mode dependency is the letter M.

Mode dependency is used to indicate that the effects of particular inputs and outputs of an element depend on the mode in which the element is operating.

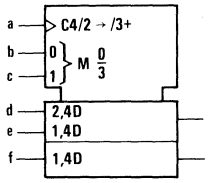
If an input or output has the same effect in different modes of operation, the identifying numbers of the relevant affecting M*m* inputs will appear in the label of that affected input or output between parentheses and separated by solidi (Figure 22).

4.11.1 M Dependency Affecting Inputs

M dependency affects inputs the same as C dependency. When an M*m* input or M*m* output stands at its internal 1 state, the inputs affected by this M*m* input or M*m* output have their normally defined effect on the function of the element, i.e., the inputs are enabled.

When an M*m* input or M*m* output stands at its internal 0 state, the inputs affected by this M*m* input or M*m* output have no effect on the function of the element. When an affected input has several sets of labels separated by solidi (e.g., C4/2→/3+), any set in which the identifying number of the M*m* input or M*m* output appears has no effect and is to be ignored. This represents disabling of some of the functions of a multifunction input.

The circuit in Figure 18 has two inputs, **b** and **c**, that control which one of four modes (0, 1, 2, or 3) will exist at any time. Inputs **d**, **e**, and **f** are D inputs subject to dynamic control (clocking) by the **a** input. The numbers 1 and 2 are in the series chosen to indicate the modes so inputs **e** and **f** are only enabled in mode 1 (for parallel loading) and input **d** is only enabled in mode 2 (for serial loading). Note that input **a** has three functions. It is the clock for entering data. In mode 2, it causes right shifting of data, which means a shift away from the control block. In mode 3, it causes the contents of the register to be incremented by one count.



Note that all operations are synchronous.

In MODE 0 (b = 0, c = 0), the outputs remain at their existing states as none of the inputs has an effect.

In MODE 1 (b = 1, c = 0), parallel loading takes place thru inputs e and f.

In MODE 2 (b = 0, c = 1), shifting down and serial loading thru input d take place.

In MODE 3 (b = c = 1), counting up by increment of 1 per clock pulse takes place.

Figure 18. M (Mode) Dependency Affecting Inputs

4.11.2 M Dependency Affecting Outputs

When an M*m* input or M*m* output stands at its internal 1 state, the affected outputs stand at their normally defined internal logic states, i.e., the outputs are enabled.

When an M*m* input or M*m* output stands at its internal 0 state, at each affected output any set of labels containing the identifying number of that M*m* input or M*m* output has no effect and is to be ignored. When an output has several different sets of labels separated by solidi (e.g., 2,4/3,5), only those sets in which the identifying number of this M*m* input or M*m* output appears are to be ignored.

Figure 19 shows a symbol for a device whose output can behave like either a 3-state output or an open-collector output depending on the signal applied to input **a**. Mode 1 exists when input **a** stands at its internal 1 state and, in that case, the three-state symbol applies and the open-element symbol has no effect. When **a** = 0, mode 1 does not exist so the three-state symbol has no effect and the open-element symbol applies.

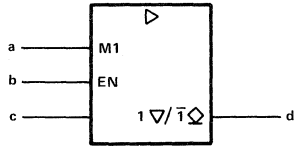


Figure 19. Type of Output Determined by Mode

In Figure 20, if input **a** stands at its internal 1 state establishing mode 1, output **b** will stand at its internal 1 state only when the content of the register equals 9. Since output **b** is located in the common-control block with no defined function outside of mode 1, the state of this output outside of mode 1 is not defined by the symbol.

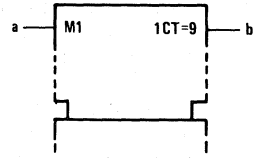


Figure 20. An Output of the Common-Control Block

In Figure 21, if input **a** stands at its internal 1 state establishing mode 1, output **b** will stand at its internal 1 state only when the content of the register equals 15. If input **a** stands at its internal 0 state, output **b** will stand at its internal 1 state only when the content of the register equals 0.

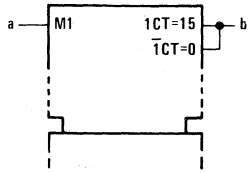


Figure 21. Determining and Output's Function

In Figure 22 inputs **a** and **b** are binary weighted to generate the numbers 0, 1, 2, or 3. This determines which one of the four modes exists.

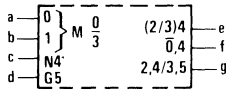


Figure 22. Dependent Relationships Affected by Mode

At output **e** the label set causing negation (if **c** = 1) is effective only in modes 2 and 3. In modes 0 and 1 this output stands at its normally defined state as if it had no labels. At output **f** the label set has effect when the mode is not 0 so output **e** is negated (if **c** = 1) in modes 1, 2, and 3. In mode 0 the label set has no effect so the output stands at its normally defined state. In this example $\overline{0}$,4 is equivalent to (1/2/3)4. At output **g** there are two label sets. The first set, causing negation (if **c** = 1), is effective only in mode 2. The second set, subjecting **g** to AND dependency on **d**, has effect only in mode 3.

Note that in mode 0 none of the dependency relationships has any effect on the outputs, so **e**, **f**, and **g** will all stand at the same state.

4.12 A (Address) Dependency

The symbol denoting address dependency is the letter A.

Address dependency provides a clear representation of those elements, particularly memories, that use address control inputs to select specified sections of a multildimensional arrays. Such a section of a memory array is usually called a word. The purpose of address dependency is to allow a symbolic presentation of the entire array. An input of the array shown at a particular

element of this general section is common to the corresponding elements of all selected sections of the array. An output of the array shown at a particular element of this general section is the result of the OR function of the outputs of the corresponding elements of selected sections.

Inputs that are not affected by any affecting address input have their normally defined effect on all sections of the array, whereas inputs affected by an address input have their normally defined effect only on the section selected by that address input.

An affecting address input is labeled with the letter A followed by an identifying number that corresponds with the address of the particular section of the array selected by this input. Within the general section presented by the symbol, inputs and outputs affected by an A*m* input are labeled with the letter A, which stands for the identifying numbers, i.e., the addresses, of the particular sections.

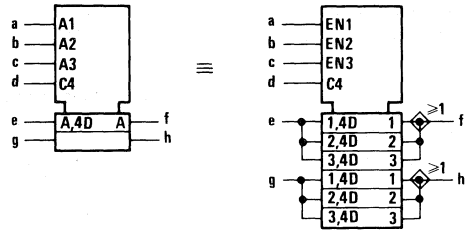


Figure 23. A (Address) Dependency

Figure 23 shows a 3-word by 2-bit memory having a separate address line for each word and uses EN dependency to explain the operation. To select word 1, input **a** is taken to its 1 state, which establishes mode 1. Data can now be clocked into the inputs marked "1,4D." Unless words 2 and 3 are also selected, data cannot be clocked in at the inputs marked "2,4D" and "3,4D." The outputs will be the OR functions of the selected outputs, i.e., only those enabled by the active EN functions.

The identifying numbers of affecting address inputs correspond with the addresses of the sections selected by these inputs. They need not necessarily differ from those of other affecting dependency-inputs (e.g., G, V, N, . . .), because in the general section presented by the symbol they are replaced by the letter A.

If there are several sets of affecting A*m* inputs for the purpose of independent and possibly simultaneous access to sections of the array, then the letter A is modified to 1A, 2A, ... Because they have access to the same sections of the array, these sets of A inputs may have the same identifying numbers. The symbols for 'HC170 or SN74LS170 make use of this.

Figure 24 is another illustration of the concept.

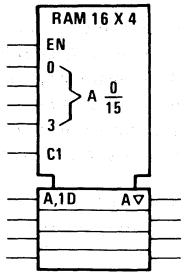


Figure 24. Array of 16 Sections of Four Transparent Latches with 3-State Outputs Comprising a 16-Word X 4-Bit Random-Access Memory

Table IV. Summary of Dependency Notation

TYPE OF DEPENDENCY	LETTER SYMBOL*	AFFECTING INPUT AT ITS 1-STATE	AFFECTING INPUT AT ITS 0-STATE
Address	A	Permits action (address selected)	Prevents action (address not selected)
Control	C	Permits action	Prevents action
Enable	EN	Permits action	Prevents action of inputs ◇outputs off ▽outputs at external high impedance, no change in internal logic state Other outputs at internal 0 state
AND	G	Permits action	Imposes 0 state
Mode	M	Permits action (mode selected)	Prevents action (mode not selected)
Negate (Ex-OR)	N	Complements state	No effect
Reset	R	Affected output reacts as it would to S = 0, R = 1	No effect
Set	S	Affected output reacts as it would to S = 1, R = 0	No effect
OR	V	Imposes 1 state	Permits action
Transmission	X	Bidirectional connection exists	Bidirectional connection does not exist
Interconnection	Z	Imposes 1 state	Imposes 0 state

*These letter symbols appear at the AFFECTING input (or output) and are followed by a number. Each input (or output) AFFECTED by that input is labeled with that same number. When the labels EN, R, and S appear at inputs without the following numbers, the descriptions above do not apply. The action of these inputs is described under "Symbols Inside the Outline," see 3.3.

5.0 BISTABLE ELEMENTS

The dynamic input symbol, the postponed output symbol, and dependency notation provide the tools to differentiate four main types of bistable elements and make synchronous and asynchronous inputs easily recognizable (Figure 25). The first column shows the essential distinguishing features; the other columns show examples.

Transparent latches have a level-operated control input. The D input is active as long as the C input is at its internal 1 state. The outputs respond immediately. Edge-triggered elements accept data from D, J, K, R, or S inputs on the active transition of C. Pulse-triggered elements

require the setup of data before the start of the control pulse; the C input is considered static since the data must be maintained as long as C is at its 1 state. The output is postponed until C returns to its 0 state. The data-lock-out element is similar to the pulse-triggered version except that the C input is considered dynamic in that shortly after C goes through its active transition, the data inputs are disabled and data does not have to be held. However, the output is still postponed until the C input returns to its initial external level.

Notice that synchronous inputs can be readily recognized by their dependency labels (1D, 1J, 1K, 1S, 1R) compared to the asynchronous inputs (S, R), which are not dependent on the C inputs.

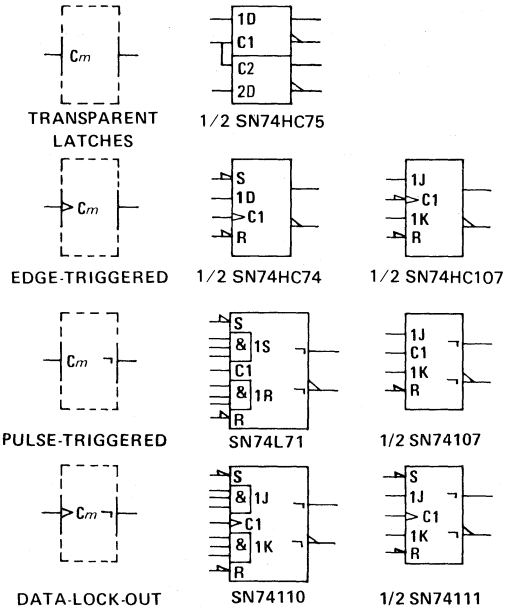


Figure 25. Four Types of Bistable Circuits

6.0 CODERS

The general symbol for a coder or code converter is shown in Figure 26. X and Y may be replaced by appropriate indications of the code used to represent the information at the inputs and at the outputs, respectively.

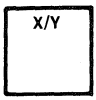


Figure 26. Coder General Symbol

Indication of code conversion is based on the following rule:

> Depending on the input code, the internal logic states of the inputs determine an internal value. This value is reproduced by the internal logic states of the outputs, depending on the output code.

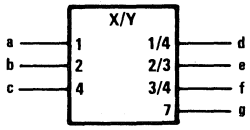
The indication of the relationships between the internal logic states of the inputs and the internal value is accomplished by:

1) labeling the inputs with numbers. In this case the internal value equals the sum of the weights associated with those inputs that stand at their internal 1-state, or by
2) replacing X by an appropriate indication of the input code and labeling the inputs with characters that refer to this code.

The relationships between the internal value and the internal logic states of the outputs are indicated by:

1) labeling each output with a list of numbers representing those internal values that lead to the internal 1-state of that output. These numbers shall be separated by solidi as in Figure 27. This labeling may also be applied when Y is replaced by a letter denoting a type of dependency (see Section 7). If a continuous range of internal values produces the internal 1 state of an output, this can be indicated by two numbers that are inclusively the beginning and the end of the range, with these two numbers separated by three dots (e.g., 4 . . . 9 = 4/5/6/7/8/9) or by
2) replacing Y by an appropriate indiction of the output code and labeling the outputs with characters that refer to this code as in Figure 28.

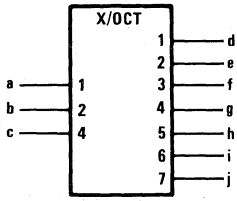
Alternatively, the general symbol may be used together with an appropriate reference to a table in which the relationship between the inputs and outputs is indicated. This is a recommended way to symbolize a PROM after it has been programmed.



FUNCTION TABLE

INPUTS			OUTPUTS			
c	b	a	g	f	e	d
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	0	1	0
0	1	1	0	1	1	0
1	0	0	0	1	0	1
1	0	1	0	0	0	0
1	1	0	0	0	0	0
1	1	1	1	0	0	0

Figure 27. An X/Y Code Converter



FUNCTION TABLE

INPUTS			OUTPUTS						
c	b	a	j	i	h	g	f	e	d
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	0
0	1	1	0	0	0	0	1	0	0
1	0	0	0	0	0	1	0	0	0
1	0	1	0	0	1	0	0	0	0
1	1	0	0	1	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0

Figure 28. An X/Octal Code Converter

7.0 USE OF A CODER TO PRODUCE AFFECTING INPUTS

It often occurs that a set of affecting inputs for dependency notation is produced by decoding the signals on certain inputs to an element. In such a case use can be made of the symbol for a coder as an embedded symbol (Figure 29).

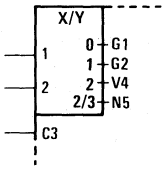


Figure 29. Producing Various Types of Dependencies

If all affecting inputs produced by a coder are of the same type and their identifying numbers shown at the outputs of the coder, Y (in the qualifying symbol X/Y) may be replaced by the letter denoting the type of dependency. The indications of the affecting inputs should then be omitted (Figure 30).

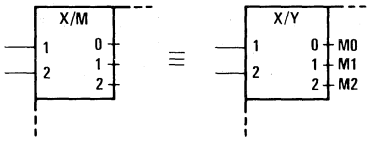


Figure 30. Producing One Type of Dependency

8.0 USE OF BINARY GROUPING TO PRODUCE AFFECTING INPUTS

If all affecting inputs produced by a coder are of the same type and have consecutive identifying numbers not necessarily corresponding with the numbers that would have been shown at the outputs of the coder, use can be made of the binary grouping symbol. k external lines effectively generate 2^k internal inputs. The bracket is followed by the letter denoting the type of dependency followed by m1/m2. The m1 is to be replaced by the smallest identifying number and the m2 by the largest one, as shown in Figure 31.

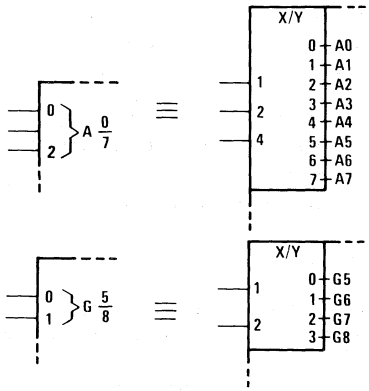


Figure 31. Use of the Binary Grouping Symbol

9.0 SEQUENCE OF INPUT LABELS

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If an input having a single functional effect is affected by other inputs, the qualifying symbol (if there is any) for that functional effect is preceded by the labels corresponding to the affecting inputs. The left-to-right order of these preceding labels is the order in which the effects or modifications must be applied. The affected input has no functional effect on the element if the logic state of any one of the affecting inputs, considered separately, would cause the affected input to have no effect, regardless of the logic states of other affecting inputs.

If an input has several different functional effects or has several different sets of affecting inputs, depending on the mode of action, the input may be shown as often as required. However, there are cases in which this method of presentation is not advantageous. In those cases the input may be shown once with the different sets of labels separated by solidi (Figure 32). No meaning is attached to the order of these sets of labels. If one of the functional effects of an input is that of an unlabeled input to the element, a solidus will precede the first set of labels shown.

If all inputs of a combinational element are disabled (caused to have no effect on the function of the element), the internal logic states of the outputs of the element are not specified by the symbol. If all inputs of a sequential element are disabled, the content of this element is not changed and the outputs remain at their existing internal logic states.

Labels may be factored using algebraic techniques (Figure 33).

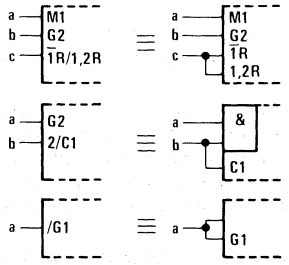

Figure 32. Input Labels

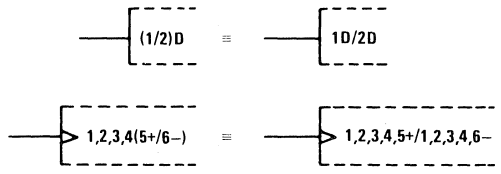

Figure 33. Factoring Input Labels

10.0 SEQUENCE OF OUTPUT LABELS

If an output has a number of different labels, regardless of whether they are identifying numbers of affecting inputs or outputs or not, these labels are shown in the following order:

1) If the postponed output symbol has to be shown, this comes first, if necessary preceded by the indications of the inputs to which it must be applied
2) Followed by the labels indicating modifications of the internal logic state of the output, such that the left-to-right order of these labels corresponds with the order in which their effects must be applied
3) Followed by the label indicating the effect of the output on inputs and other outputs of the element.

Symbols for open-circuit or three-state outputs, where applicable, are placed just inside the outside boundary of the symbol adjacent to the output line (Figure 34).

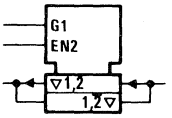

Figure 34. Placement of 3-State Symbols

If an output needs several different sets of labels that represent alternative functions (e.g., depending on the mode of action), these sets may be shown on different output lines that must be connected outside the outline. However, there are cases in which this method of presentation is not advantageous. In those cases the output may be shown once with the different sets of labels separated by solidi (Figure 35).

Two adjacent identifying numbers of affecting inputs in a set of labels that are not already separated by a nonnumeric character should be separated by a comma.

If a set of labels of an output not containing a solidus contains the identifying number of an affecting M*m* input standing at its internal 0 state, this set of labels has no effect on that output.

Labels may be factored using algebraic techniques (Figure 36).

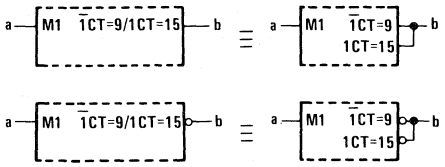

Figure 35. Output Labels

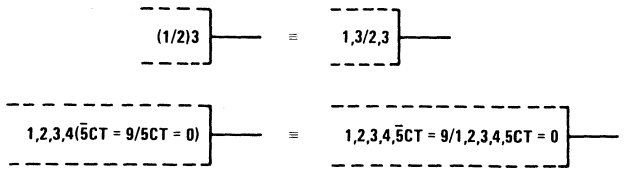

Figure 36. Factoring Output Labels

4

F.A. Mann received his Bachelor of Science degree from the United States Naval Academy, Annapolis, MD in 1953 and his Master's degree in Engineering Administration from Southern Methodist University, Dallas, TX in 1970. He joined Texas Instruments in 1957 and has worked as a Manufacturing Engineer, Product Marketing Engineer, and Semiconductor Data Sheet Manager. Currently, he serves as Technical Advisor for data sheets and other technical documentation for semiconductors. He has served on many JEDEC committees since 1963 and has been a USA delegate to the technical committee for semiconductor devices of the International Electrotechnical Commission since 1970. He is a member of the IEEE committees for Logic Symbols and for Logic Diagrams, and participates in meetings of an international working group on logic symbols.

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The TTL Data Book
Volume 2

Advanced Schottky Family (ALS/AS) Application

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List of Illustrations (Continued)

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INTRODUCTION

The purpose of this Application Report is to assist the designers of high-performance digital logic systems in the use of the new series of Advanced Schottky-clamped* TTL integrated circuits.

Detailed electrical characteristics of these devices are provided and, if available, tables have been included that compare specific parameters of the devices with those of other logic families. In addition, interfamily information is provided to allow system designers to mix logic families in the same circuit. This allows the designer to use the relative merits of each logic family in high preformance state-of-the-art designs.

The major subject areas covered in this Application Report are as follows:

- Advanced Schottky process
- Fanouts
- Transfer characteristics
- Input and output parameters
- Speed and power information
- Noise margins
- Power supply considerations
- Noise sources and their abatement
- Back panel and printed circuit wiring guidelines
- Line driving and receiving

INTRODUCTION TO ADVANCED SCHOTTKY-CLAMPED TTL

Series 54/74 transistor-transistor logic (TTL) has, since its introduction in 1965, become the most popular digital integrated circuit logic family ever offered. Its popularity has allowed the development of high-volume production techniques which have made it the most economical approach to the implementation of major portions of medium-to-high performance digital logic systems. These systems range from simple decision making to highly complex real-time computer installations that handle worldwide data processing.

The proliferation of and economical impact of these digital logic systems has created a demand for constant improvement in efficiency. In response to demand, Texas Instruments examined the advantages gained by Schottky clamping. An increase in speed and performance was discovered in the use of Schottky barrier-diode clamping. The process was patented in the United States and the Schottky series 54S/74S catalog parts were made available in the early 1970s. A series 54LS/74LS was introduced later. The series 54LS/74LS was slower that the 54S/74S series but had a much lower power consumption.

*Integrated Schottky-Barrier-diode-clamped transistor is patented by Texas Instruments Incorporated, U.S. Patent Number 3,463,975.

Recent innovations in integrated circuit design have made it possible to develop two new families: the Advanced Schottky (54AS/74AS) series and the Advanced Low-Power Schottky (54ALS/74ALS) series. The 'ALS and 'AS series provide considerable higher speeds than the 'LS and 'S series, respectively. The 'ALS series offers a substantial reduction in power consumption over the 'LS series, and the 'AS series offers a substantial reduction in power consumption over the 'S series. The 'ALS/'AS series is pin-to-pin compatible with the 'LS/'S series.

SPEED-POWER SLOTS FILLED BY 'ALS AND 'AS TTL

Digital integrated circuits have historically been characterized for both speed and power. The series 54S/74S devices contain 19 mW NAND gates and 125-MHz flip-flops and the series 54LS/74LS devices contain 2-mW NAND gates and 45-MHz flip-flops. Either of these logic families could be used to design a 2-MHz system, therefore categorization strictly on the basis of power and speed is inconclusive with respect to system efficiency. To provide a means of measuring the overall circuit efficiency and performance, a speed-power product efficiency index for integrated circuits was developed. The rating of an integrated circuit is obtained by multiplying the gate propagation delay by the gate power dissipation.

Table I provides propagation delay times, power dissipation, and speed-power product for the Texas Instruments TTL series. In addition, it provides flip-flop frequency for each family as an indicator of system performance. The speed-power product rating system (measured in picojoules) is divided into circuits where speed is the prime factor and circuits where low-power is the prime factor. The 'ALS series speed-power product is approximately 4 times less than that of the 'LS series and the 'AS series speed-power product is approximately 4 times less than the 'S series. Figure 1 is a graphic analysis of the speed-power points for the various TTL families.

ADDITIONAL ADVANTAGES OFFERED BY 'ALS AND 'AS DEVICES

The 'ALS and 'AS devices offer the following additional advantages:

1. TTL compatible with 54/74, 54S/74S, 54L/74L, 54LS/74LS, and 54H/74H series gates for selectively upgrading existing systems
2. Suppresses the effects of line ringing and significantly reduces undershoot
3. Higher thresholds (noise immunity) and better stability across operating free-air temperature range
4. Input current requirement reduced by up to 50%

Table I. Typical Performance Characteristics by TTL Series

CIRCUIT TECHNOLOGY	MINIMIZING POWER					MINIMIZING DELAY TIME				
	FAMILY	PROP DELAY (ns)	PWR DISS (mW)	SPD/PWR PRODUCT (pJ)	MAXIMUM FLIP-FLOP FREQ (MHz)	FAMILY	PROP DELAY (ns)	PWR DISS (mW)	SPD/PWR PRODUCT (pJ)	MAXIMUM FLIP-FLOP FREQ (MHz)
Gold Doped	TTL	10	10	100	35	TTL	10	10	100	35
	L TTL	33	1	33	3	H TTL	6	22	132	50
Schottky Clamped	LS TTL	9	2	18	45	S TTL	3	19	57	125
	'ALS	4	1.2	4.8	70	'AS	1.7	8	13.6	200

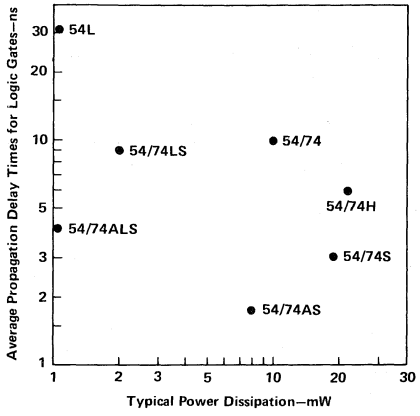

Figure 1. Speed-Power Relationships of Digital Integrated Circuits

5. Fanout is doubled
6. Terminated lines or controlled impedance circuit boards are normally not required.
7. The 'AS series offers shorter propagation delays and higher clock frequencies with relatively low power consumption.
8. The maximum flip-flop frequency has been increased to 200 MHz.

CONCEPTS OF DEFINING SERIES 'AS AND 'ALS

Both the 'ALS and 'AS series are electrically and pinout compatible with existing TTL series. The 'ALS series is suitable for replacing all TTL families except in the very highest frequency applications. Replacement with 'ALS will result in lower power consumption, smaller power supply current spikes, and, in some cases, better noise immunity than the other families. In those cases where a very high operating frequency is required, the 'AS series can be used. The 'AS devices require less than one-half of the supply current of the 'S series and has approximately twice the clocking frequency. The 'ALS devices are ideal for improving effeciency at the lower speeds. The 'AS devices are ideal for replacement of high-speed logic families including ECL 10K series.

Compatibility With Other TTL Families

To ensure complete electrical compatibility in systems using or intending to use a mixture of existing TTL families and the new 'ALS/'AS families, specific guidelines have been implemented. These guidelines ensure the continuation of desirable characteristics and incorporate newer techniques to improve performance and/or simplify the use of TTL families. Figure 2 illustrates the comparison of essential parameters of each family and shows that complete compatibility is maintained throughout the 54/74 families.

Fanout

The compatible ratings for fanout simplify the implementation of logic and provide a freedom of choice in the use of any of the seven performance ranges to design a digital logic system. Any of the Texas Instruments TTL series gates can be used to drive any other gate without the use of an interface or level-shifting circuit. The use of totem-pole-(push-pull) type output stages provides a low output impedance and the capability for both sourcing and sinking current. The output is easily adapted for driving MOS and CMOS circuits as well as the interface circuits between the output and the devices it controls. Figure 3 illustrates fanout capability.

USING THE SCHOTTKY BARRIER DIODE

The Advanced Schottky Family has been developed from two earlier concepts: the Baker Clamp and the Schottky Barrier-Diode (SBD). The use of the Baker Clamp and SBD concepts resulted in the Schottky Clamped Transistor. The Schottky clamped transistor produced the increased switching speed associated with the S series integrated circuits. The additional advances that have led to the development of 'ALS and 'AS gates and the actual gates are discussed later.

Analysis of the Schottky Clamped Transistor

The use of the Baker Clamp, shown in Figure 4, is a method of avoiding saturation of a discrete transistor. The diode forward voltage is 0.3 V to 0.4 V as compared to 0.7 V for the base-emitter junction diode. When the transistor is turned on, base current drives the transistor toward

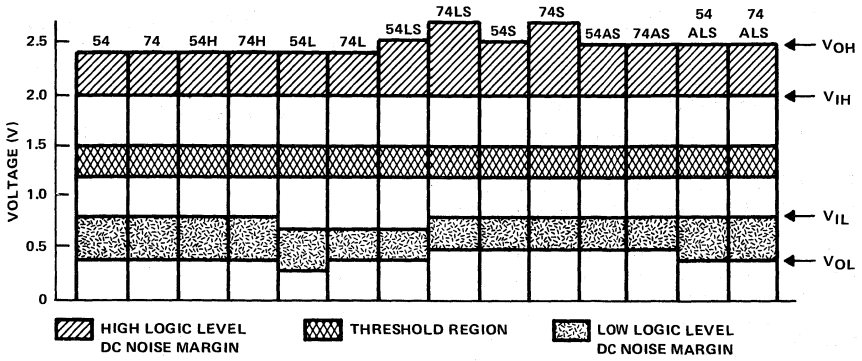

Figure 2. Series 54/74 TTL Family Compatible Levels Showing DC Noise Margins

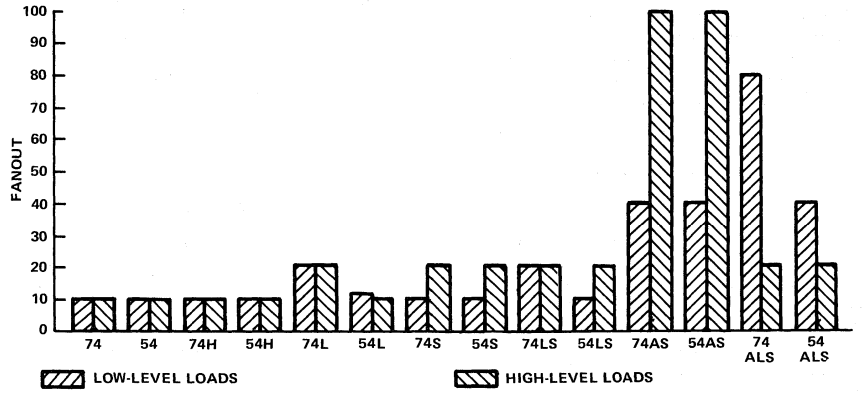

Figure 3. Fanout Capability

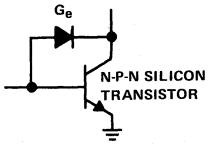

Figure 4. Baker Clamp

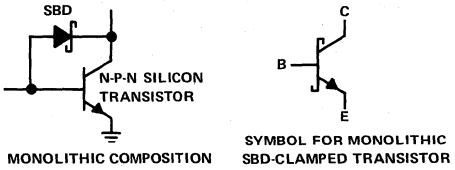

Figure 5. The Schottky-Clamped Transistor

saturation. The collector voltage drops, the germanium diode begins to conduct forward current, and excess base drive is diverted from the base-collector junction of the transistor. This causes the transistor to be held out of deep saturation, the excess base charge to not be stored, and the turn-off time to be dramatically reduced.

A germanium diode cannot be incorporated into a monolithic silicon integrated circuit. Therefore, the germanium diode must be replaced with a silicon diode which has a lower forward voltage drop than the base-collector junction of the transistor. A normal p-n diode will not meet this requirement. The SBD illustrated in Figure 5 can be used to meet the requirement.

The SBD illustrated in Figure 6 is a rectifying metal-semiconductor contact formed between a metal and a highly doped N semiconductor.

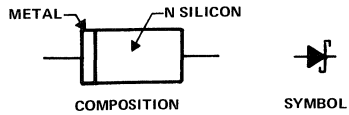

Figure 6. Schottky Barrier-Diode

The qualitative physics of an SBD is illustrated in Figure 7. The valence and conduction bands in a metal overlap make available a large number of free-energy states. The free-energy states can be filled by any electrons which are injected into the conduction band. A finite number of electrons exist in the conduction band of a semiconductor. The number of electrons depends mainly upon the thermal energy and the level of impurity atoms in the material. When a metal-semiconductor junction is formed, free electrons flow across the junction from the semiconductor, via the conduction band, and fill the free-energy states in the metal. This flow of electrons builds a depletion potential across the barrier. This depletion potential opposes the electron flow and, eventually, is sufficient to sustain a balance where there is no net electron flow across the barrier.

Under forward bias (metal positive), there are many electrons with enough thermal energy to cross the barrier potential into the metal. This forward bias is called "hot injection." Because the barrier width is decreased as forward bias V_F increases, forward current will increase rapidly with an increase in V_F.

When the SBD is reverse biased, electrons in the semiconductor require greater energy to cross the barrier. However, electrons in the metal see a barrier potential from the side essentially independent of the bias voltage and a small net reverse current will flow. Since this current flow is relatively independent of the applied reverse bias, the reverse current flow will not increase significantly until avalanche breakdown occurs.

A simple metal-n semiconductor collector contact is an ohmic contact while the SBD contact is a rectifying contact. The difference is controlled by the level of doping in the semiconductor material. As the doping is increased, the contact becomes more ohmic. Figure 8 illustrates the current-voltage characteristics according the doping applied.

Current in the SBD is carried by majority carriers. Current in the p-n junction is carried by minority carriers. The resultant minority carrier storage causes the switching

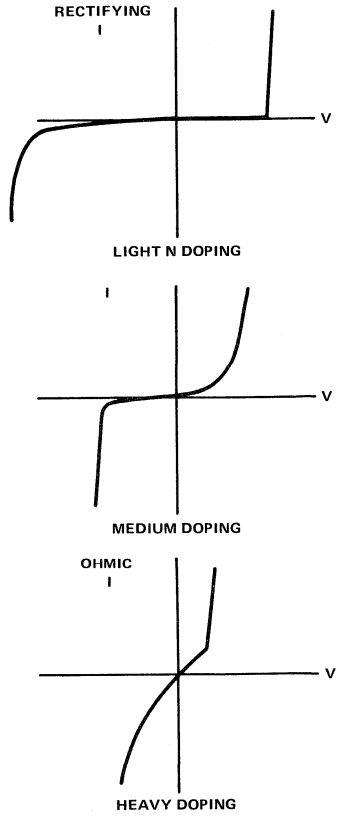

Figure 8. Metal-N Diode Current-Voltage Characteristics

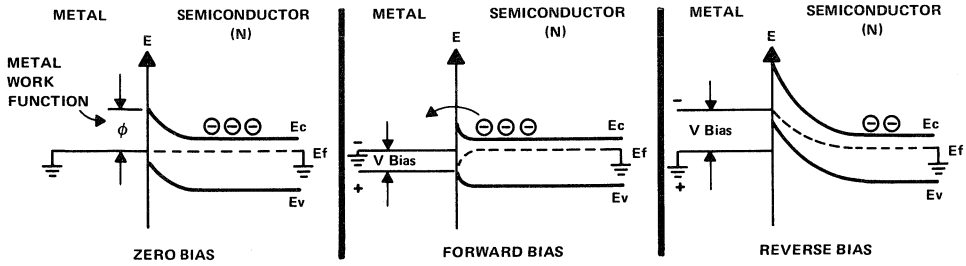

Figure 7. Schottky Barrier-Diode Energy Diagrams

time of a p-n junction to be limited when switched from forward bias to reverse bias. A p-n junction is inherently slower than an SBD even when doped with gold.

Another major difference between the SBD and p-n junction is the forward voltage drop. For diodes of the same surface area, the SBD will have a larger forward current at the same forward bias regardless of the type of metal used. The SBD forward voltage drop is lower at a given current than a p-n junction. Figure 9 illustrates the current carriers and forward current-voltage characteristics differences between the SBD and p-n junction. The SBD meets the requirements of a silicon diode which will clamp a silicon n-p-n transistor out of saturation.

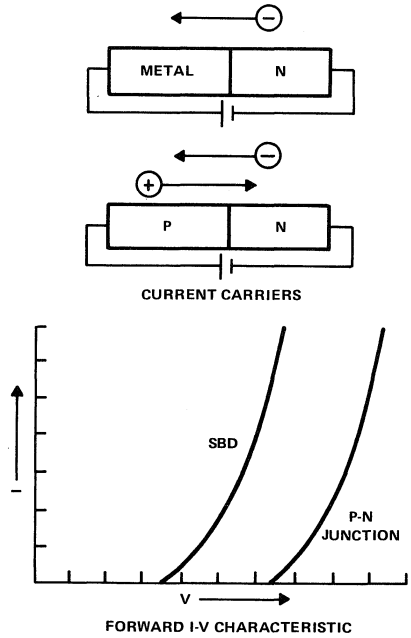

Figure 9. Differences Between P-N and Schottky Barrier-Diodes

The Advanced Schottky process differs from the Schottky process in that it uses ion implantation of impurities instead of diffusion. Ion implantation gives greater control on the depth of doping and resolution. Because of a thinner epitaxial layer and smaller all around geometries, smaller parasitic capacitances are encountered. The performance of the SBD is also enhanced by the use of oxide isolation of the transistors. This reduces the collector-substrate capacitance. Figure 10 illustrates the 'LS/'S process which consists of conventional masks, junction isolation, and a

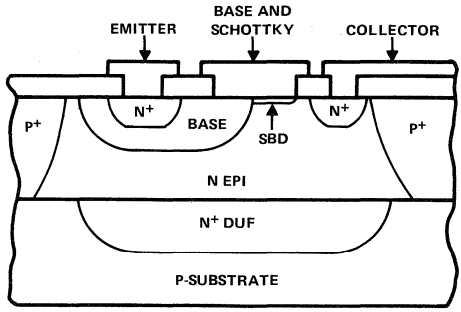

Figure 10. Standard Process ('LS/'S)

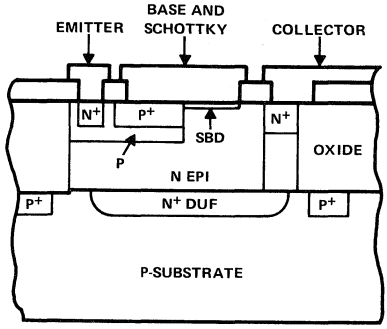

Figure 11. Advanced Process ('ALS/'AS)

standard metal system and Figure 11 illustrates the 'ALS/'AS process which consists of composed masks, ion implantation, oxide isolation, and a standard metal system.

Analysis of 'ALS and 'AS NAND Gates

The 'ALS and 'AS NAND gates in Figures 12 and 13 combine the desirable features of improved TTL circuits with the technological advantages of full Schottky clamping, ion implantation, and oxide isolation to achieve very fast switching times at a reduced speed-power product. The improvements and advantages are as follows:

1. Full Schottky clamping of all saturating transistors virtually eliminates storing excessive base charge and significantly enhances turn-off time of the transistors.
2. Elimination of transistor storage time provides stable switching times across the temperature range.
3. An active turn-off is added to square up the transfer characteristic and provide an improved high-level noise immunity.

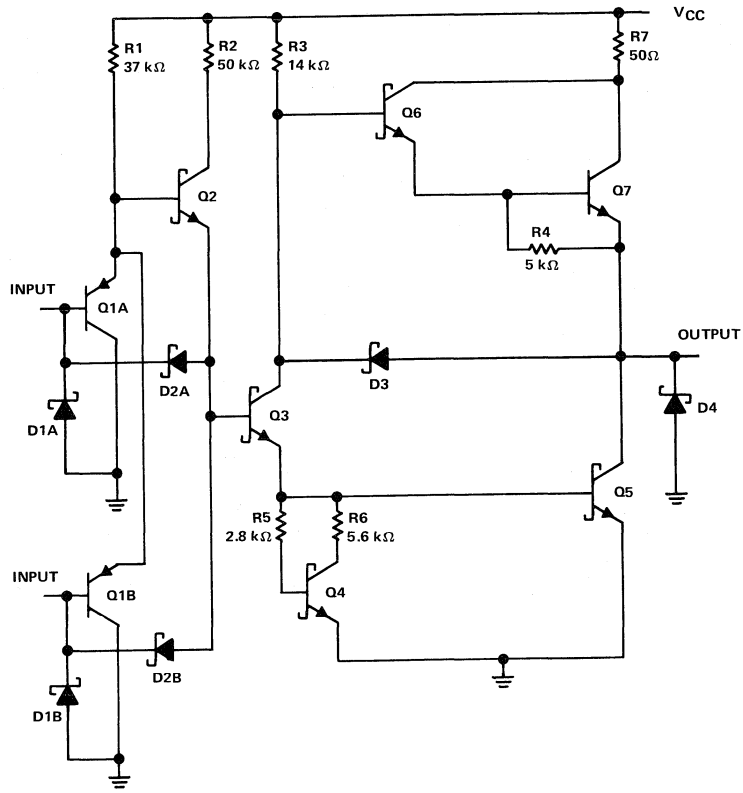

Figure 12. 'ALS00A NAND Gate Schematic

4. Input and output clamping is implemented with Schottky diodes to reduce negative-going excursions on the inputs and outputs. Because of its lower forward voltage drop and fast recovery time, the Schottky input diode provides improved clamping action over a conventional p-n junction diode.
5. The ion implantation process allows small geometries giving less parasitic capacitances so that switching times are decreased.
6. The reduction of the epi-substrate capacitance using oxide isolation also decreases switching times.

A key feature of the 'ALS and 'AS families is the improvement in typical input-threshold voltage. Figure 12 is a schematic diagram of the 'ALS00A NAND gate. Figure 13 is a schematic diagram of the 'AS00 NAND gate. The input threshold voltage of the devices is determined by the equation:

$$VT = V_{BE} \text{ of Q2} + V_{BE} \text{ of Q3} + V_{BE} \text{ of Q5} - V_{BE} \text{ of Q1A (or } V_{BE} \text{ of Q1B)} \quad (1)$$

From Eq. (1) it can be determined that the input threshold voltage is two times V_{BE} or approximately 1.4 V. Low-level input current I_{IL} is reduced in the 'ALS00A/'AS00 gates because of the improved input circuits. Buffering by transistors Q1A (or Q1B) and Q2 causes a significant reduction in low-level input current. Low-level input current is determined by the equation:

$$I_{IL} = V_{CC} - V_{BE} \text{ of Q1A} - V_I/[R(h_{FE} \text{ of Q1A} + 1)] \quad (2)$$

By using Eq. (2) low-level input current is reduced by at least the factor of h_{FE} of Q1A + 1 and is typically -10 μA for the 'ALS00A and -50 μA for the 'AS00. High-level output voltage V_{OH} is determined primarily by V_{CC},

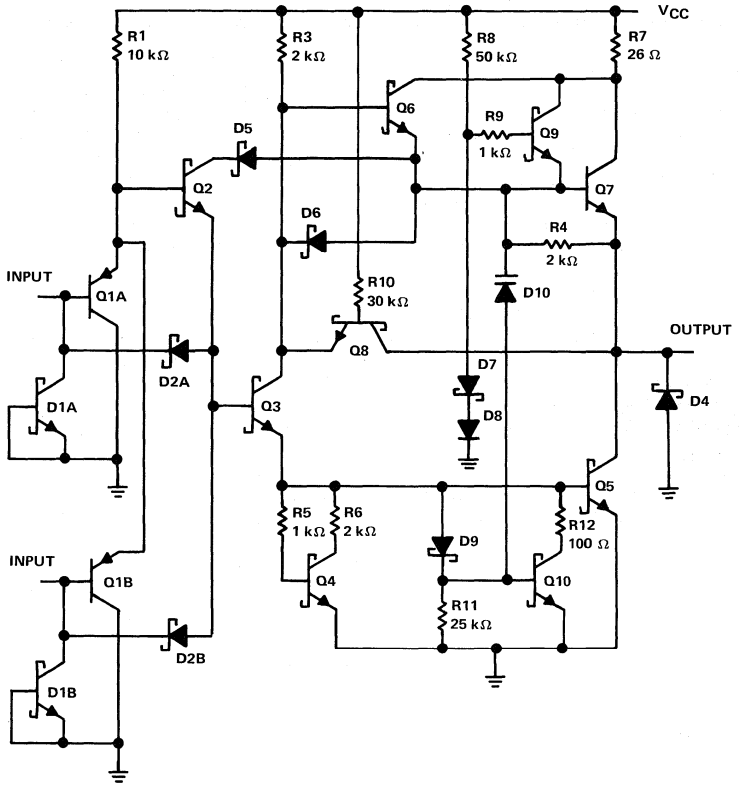

Figure 13. 'AS00 NAND Gate Schematic

resistors R4 and R7, and transistors Q6 and Q7. With no load, the high-level output voltage is approximately equal to $V_{CC} - V_{BE}$ of Q6 because the voltage across resistor R4 is 0 V. For medium-level currents, the high-level output voltage is equal to $V_{CC} - V_{BE}$ of Q6 $- V_{BE}$ of Q7 because of the Darlington gain of transistors Q6 and Q7. The current through resistor R3 is typically less than 1 μA and, therefore, the voltage drop is negligible. As conduction through transistors Q6 and Q7 is increased, the voltage drop across limiting resistor R7 will increase until the Schottky clamping diode of transistor Q6 starts to become forward biased. At this point, the current through resistor R3 (and the voltage drop) is no longer negligible and the high-level output voltage is determined by:

$$V_{OH} = V_{CC} - I_{OH \text{ through } R7} \times R7 - V_{CE} \text{ of Q6} - V_{BE} \text{ of Q7} \quad (3)$$

Low-level output voltage V_{OL} is determined by the turning on of transistor Q5. When the input is high and transistor Q2 is turned on, high-current transistor Q5 is turned on by a current path through transistor Q3 and resistor R3. Sufficient base drive is supplied to keep transistor Q5 fully turned on at an apparent output resistance of 14 Ω for 'ALS and 6Ω for 'AS.

The fanout is up to 40 for a 'S4ALS device that is driving a 'S4ALS device and up to 80 for a '74ALS device, that is driving a '74ALS device and provides a guaranteed low-level output current of 4 mA and 8 mA, respectively.

The increase in speed-power product of 'S4ALS/'74ALS devices, a factor four times better than 'S4LS/'74LS devices, is due to the design consideration of the quiescent and switching operations of the circuit. In the quiescent state, transistor Q2 allows the use of a reduced low-level input current. This reduces the fanout and reduces the overall quiescent current requirements.

The design of diodes D2 and D3 (or transistor Q8) and transistor Q4 enhances the speed-power product of the device. Transistor Q4 reduces the turn-off time and consequently the current transients caused by conduction

overlap of transistor Q5. The same principle is used by diodes D2 and D3 and transistor Q3 in turning off transistor Q7. In addition, the active turn-off design produces a square transfer characteristic.

The 'AS00 gate has additional circuits not on the 'ALS00A gate. The circuits are added to enhance the throughput of the 'AS Family.

Transistor Q10 has been added as a discharge path for the base-collector capacitance of transistor Q5. Without transistor Q10, rising voltages at the collector of transistor Q5 would force current, via the base-collector capacitance, into the base of transistor Q5 causing it to turn on. However, diode D10 causes transistor Q10 to turn on (during rising voltage) and keeps transistor Q5 turned off. Diodes D6 and D9 serve as a discharge path for capacitor-diode D10.

CIRCUIT PARAMETERS

Worst-case testing of 'ALS/'AS devices provides a margin of safety. [All dc limits shown on the data sheet are guaranteed over the entire temperature range ($-55\,°C$ to $125\,°C$) for series 54ALS/54AS and $0\,°C$ to $70\,°C$ for series 74ALS/74AS)]. In addition, the dc limits are guaranteed over the entire supply voltage range (4.5 V to 5.5 V).

Transfer Characteristics

Since the most common application for a logic gate is to drive a similar logic gate, the input and output logic levels must be compatible. The input and output logic levels for 'ALS/'AS devices are as follows:

- V_{IL} — The voltage value required for a low-level input voltage that guarantees operation
- V_{IH} — The voltage value required for a high-level input voltage that guarantees operation
- V_{OL} — The guaranteed maximum low-level output voltage of a gate
- V_{OH} — The guaranteed minimum high-level output voltage of a gate.

With the exception of high-level ouput voltage (which is a direct function of supply voltage), these values remain virtually unchanged over the temperature range and under normal operating conditions of the device.

Analysis of the input and output response characteristics of 'ALS/'AS TTL gates is necessary to understand the operation of these devices in most system applications. The dc response characteristics can best be depicted by an input voltage V_I versus output voltage V_O transfer plot.

Figure 14 plots the 'ALS/'AS characteristics as compared with members of other TTL logic families.

As shown in Figure 14, the 'ALS and 'AS devices exhibit a much better output savings when compared with standard TTL devices. The better high-level output voltage is primarily because of the active turn off of the low-level output transistor. The diode voltage drop in the normal output is replaced by a low-current V_{BE} voltage drop. This provides

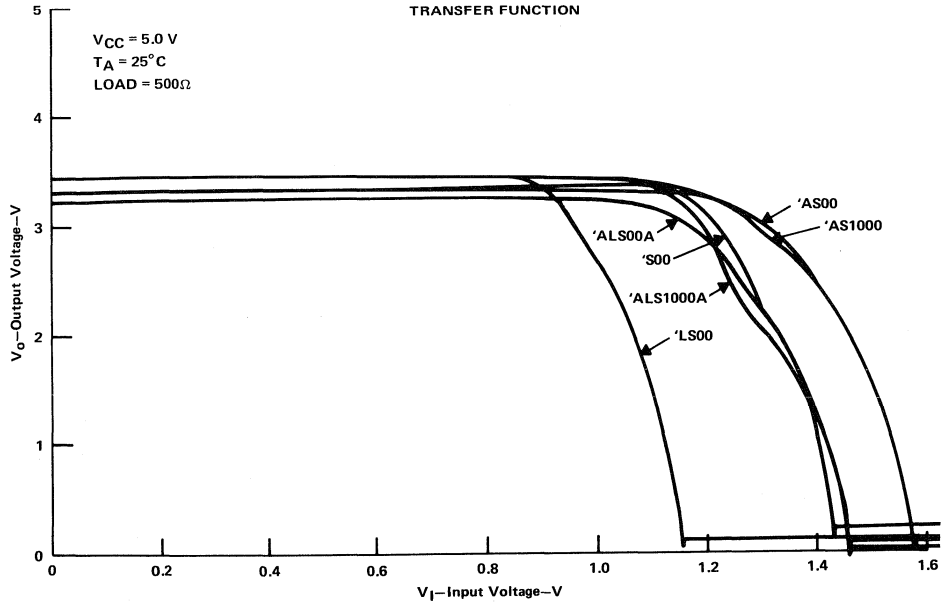

Figure 14. Input Voltage vs Output Voltage of 'ALS/'AS

a better high-level noise immunity in 'ALS and and 'AS over standard TTL devices.

Input Characteristics

To use 'ALS/'AS devices fully, a knowledge of the input and output characteristics is required. This is particularly true when a device interfaces with a device not in the same TTL series. In addition, knowledge of voltage and current relationships for all elements is important for proper design.

Figure 15 illustrates a typical plot for input current I_I versus input voltage, V_I, characteristics for 'ALS/'AS gate inputs during normal operation. A typical series 54/74 characteristic plot is also shown for reference. Any device used to drive a TTL gate must source and sink current. Conventionally, current flowing toward a device input terminal is designated as positive and current flowing out of a device input terminal is designated as negative. Low-level input current is negative current because it flows out of the input terminal. High-level input current is a positive current because it flows into the input terminal.

For transmission line conditions, a more accurate plot of the reverse bias section of these curves is required. These curves, Figure 16, are characteristic of the input clamping diode.

Low-Level Input Current

Figure 17 illustrates the dc equivalent of a standard 'ALS/'AS input circuit and shows the input current paths during a low-level input state. The low-level input current is primarily determined by resistor R1. However, low-level input current is also a function of the supply voltage, the ambient temperature, and the low-level input voltage. To

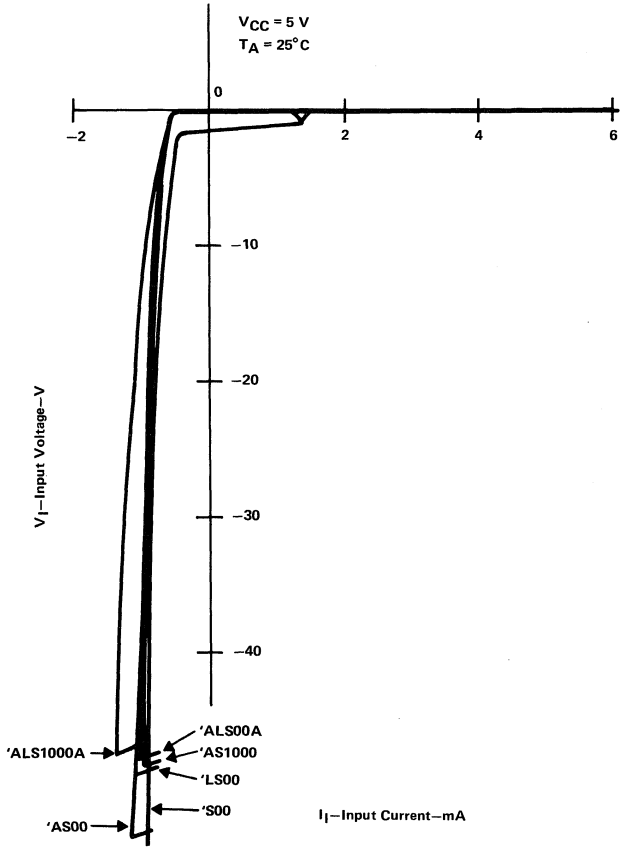

Figure 15. Input Current vs Input Voltage for TTL Families

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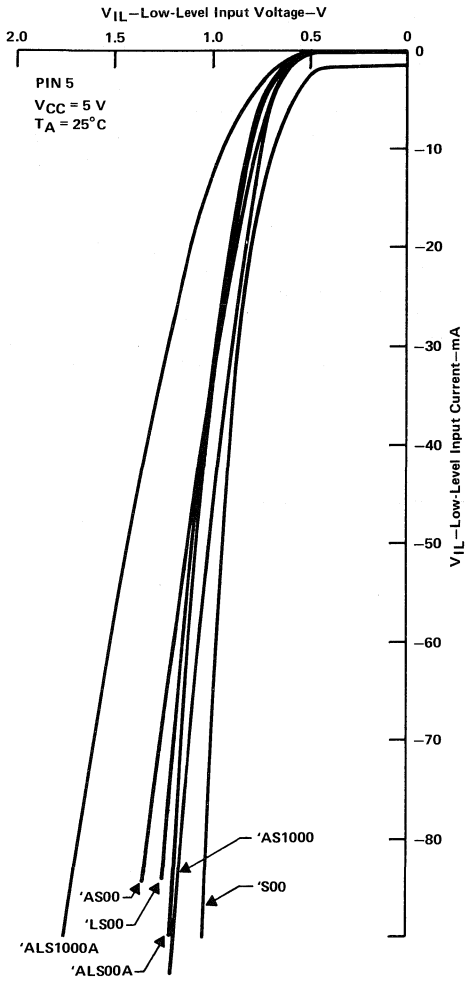

Figure 16. Low-Level Input Current vs High-Level Input Voltage for TTL Families

assure desired device operation under all possible conditions, the worst-case test is performed on all devices. Supply voltage is taken to the highest allowable value to cause the low-level input current to be at a maximum. With the exception of the input under test, all unused inputs are taken to a high level. This enhances any contribution of these inputs to the low-level input current of the emitter under test.

Input Clamping Diode Test

The quality of the input clamping SBD (D2 in Figure 17) is tested by ensuring that the forward voltage drop is not

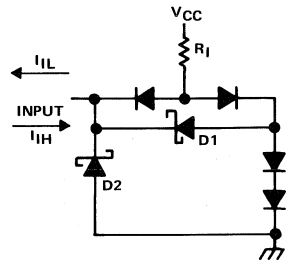

Figure 17. DC Equivalent Input Circuit for Series 'ALS Gate

greater than −1.2 V for 'AS and −1.5 V for 'ALS with a forward current of 18 mA. These values are guaranteed at minimum supply voltage and are valid across the operating temperature range. The characteristic of the input diode is illustrated in Figure 16.

High-Level Input Current

Another input parameter that must be measured and controlled is high-level input current. To ensure desired device operation under all possible conditions, the worst-case test is performed with all unused inputs grounded and supply voltage at its maximum value. This provides the highest value of low-level input current. Those devices with a high-level input current of sufficient magnitude to cause a degradation of high-level output voltage at an output must be screened out.

Input Breakdown Test

An additional high-level input current test is performed to check for base-emitter breakdown under the application of the full range of input voltages. This test is performed under the worst-case supply voltage conditions and is important because the base-emitter junction is small and can easily be overdissipated during the breakdown conditions.

Output Characteristics

The most versatile TTL output configuration is the push-pull (totem-pole) type. The totem-pole output has a low output impedance drive capability at both high and low logic levels. Both 'ALS and 'AS families use this configuration and have fanouts of 40 in both the high- and low-level states.

High-Level Output Characteristics

The ability of the totem-pole output to supply high-level output current is parametrically tested by applying a high-level input current value during measurement of high-level output voltage. However, the quality of the output stage is best indicated by parametrically measuring its current sourcing I_{OS} capability when connected to ground. Figure 18 shows the equivalent output circuit under high-level output conditions.

Figure 19 illustrates typical high-level characteristics. When measuring worst-case high-level output voltage, minimum supply voltage is used. A worst-case low-level

input voltage is applied to an input and all unused inputs are tied to supply voltage.

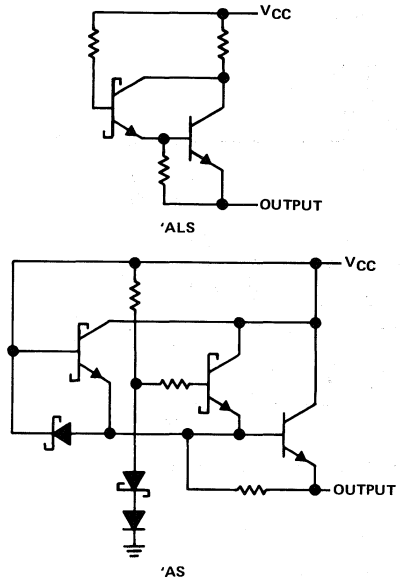

Figure 18. Equivalent Output Circuit for 'ALS/'AS Gates

Low-Level Output Characteristics

Figure 20 shows that section of the output drive circuit which produces a low-level output voltage V_{OL}. This characteristic is also tested at minimum supply voltage. Figure 21 illustrates the typical curve.

Switching Speed

Two switching-speed parameters are guaranteed on Series 'ALS and 'AS gates: propagation delay time for a high-level to a low-level at the output t_{PHL}, and a low-level to high-level transition time t_{PLH}. Both parameters are specified with respect to the input pulse using standard test conditions as follows:

V_{CC} = 4.5 V to 5.5 V
C_L = 50 pF
R_L = 500
T_A = MIN to MAX

Under these conditions, times in the order of 4 ns for 'ALS and 1.7 ns for 'AS are typical. Figures 22 and 23 illustrate how the propagation delay time for 'ALS and 'AS devices vary with load capacitance.

Most current in the output stage is drawn when both output transistors are on (i.e., during output transitions, the average power dissipation of a gate with a totem-pole output increases with operating frequency). This is caused by more high-current transitions per second at the output as the frequency increases. Figure 24 illustrates the effect for both 'ALS and 'AS devices.

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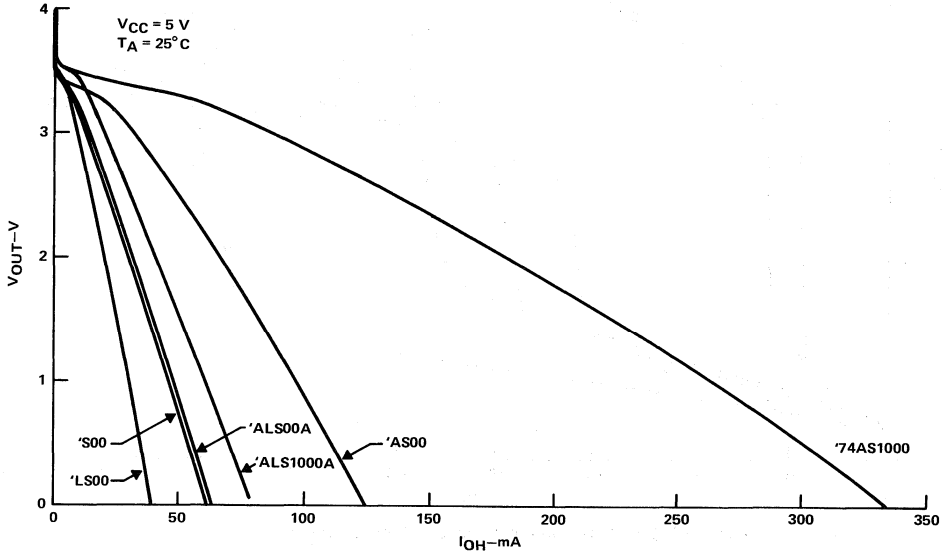

Figure 19. High-Level Output Voltage vs High-Level Output Current

DC Noise Margins

Noise margin is a voltage specification which guarantees the static dc immunity of a circuit to adverse operating conditions. Noise margin is defined as the difference between the worst-case input logic level (V_{IH} minimum or V_{IL} maximum) and the guaranteed worst-case output (V_{OH} minimum or V_{OL} maximum) specified to drive the inputs. Table II lists the worst-case output limits for the 'AS and 'ALS families.

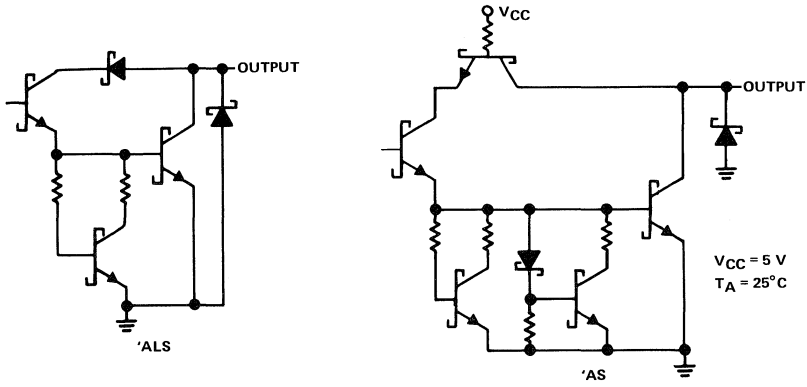

Figure 20. Low-Level Output Circuit for 'ALS/'AS Gates

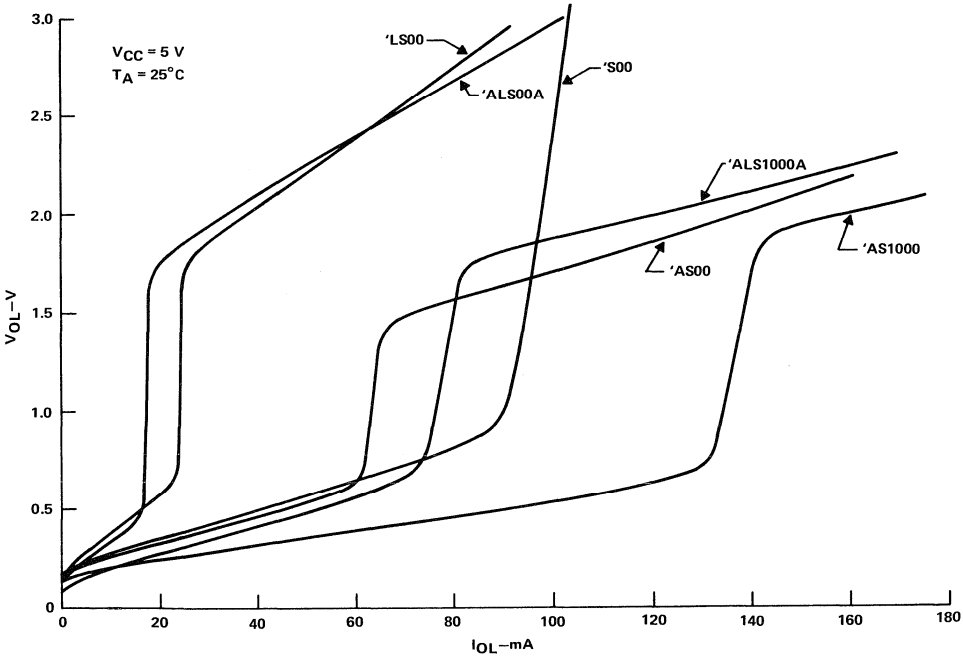

Figure 21. Low-Level Output Voltage vs Low-Level Output Current

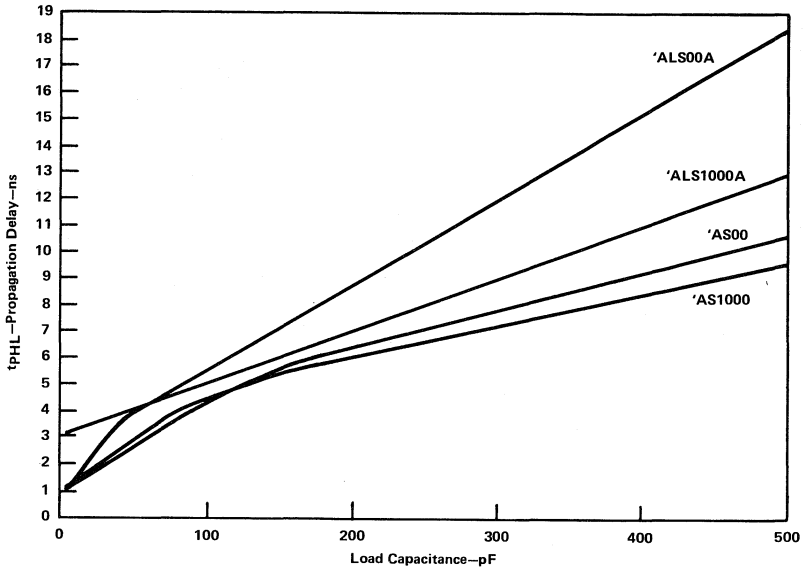

Figure 22. High- to Low-Level Propagation Delay vs Load Capacitance

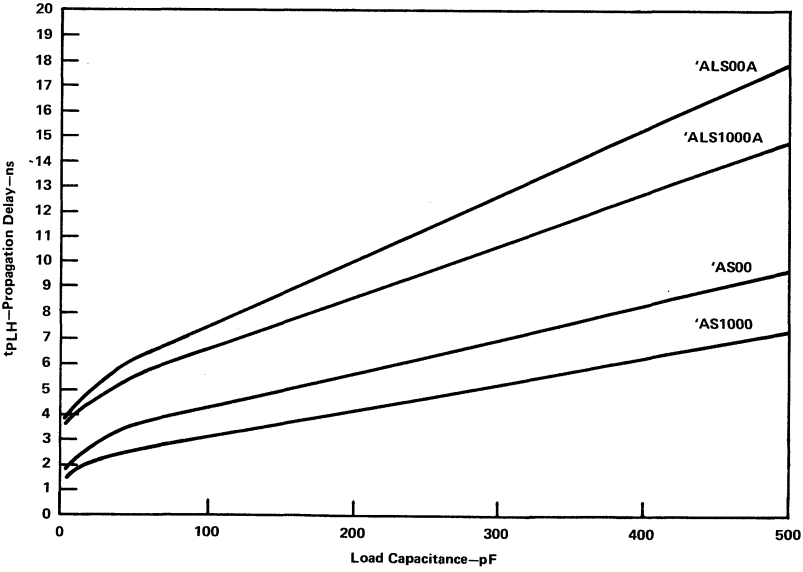

Figure 23. Low- to High-Level Propagation Delay vs Load Capacitance

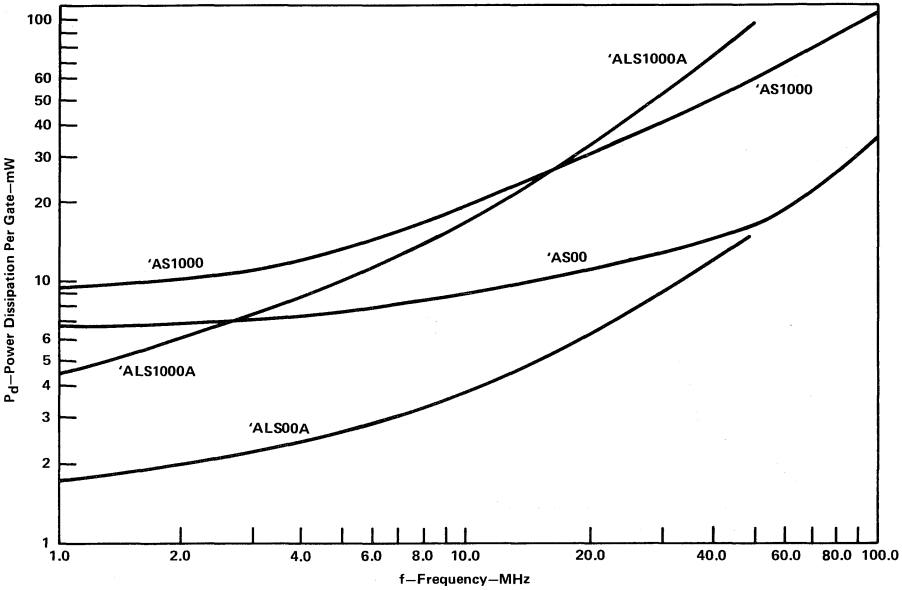

Figure 24. Power Dissipation per Gate vs Frequency

Specified Logic Levels and Thresholds

The high-level noise margin is obtained by subtracting V_{IH} minimum from V_{OH} minimum. The low-level noise margin is obtained by subtracting V_{IL} maximum from V_{OL} maximum. The worst-case high-level noise margin is guaranteed to be at least 500 mV for both 'AS and 'ALS devices and at least 300 mV for low-level noise immunity across the operating free-air temperature ranges.

The usefulness of noise margins at the system design level is the ability of a device to be impervious to noise spikes at the input. The input voltage falls into one of three categories: low-logic state (between ground and 0.8 V), threshold region (between 0.8 V and 2 V), or high-logic state (between 2 V and V_{CC}). If an input voltage remains exclusively in the low-logic or high-logic state, it can undergo any excursions within that state. A level change from 5.5 V to 2 V or from ground to 0.8 V should not affect the output state of the device. To guarantee an expected output level change, the appropriate input has to undergo a change from one input state to the other input state (i.e., a transition through the threshold region). If a device will not remain in the correct state when voltage excursions on the input are occurring, it is violating its truth table.

Noise Rejection

The ability of a logic element to operate in a noise environment involves more than the dc or ac noise margins previously discussed. To present a problem, an externally generated noise pulse must be received into the system and cause a malfunction. Stable logic systems with no storage

Table II. Worst Case Output Parameters

PARAMETER (V)	'AS (0°C to 70°C)	'ALS (0°C to 70°C)	'AS (−55°C to 125°C)	'ALS (−55°C to 125°C)
V_{IH}(MIN)	2	2	2	2
V_{IL}(MAX)	0.8	0.8	0.8	0.8
V_{OH}(MIN) @ $_{CC}$ = 4.5 V*	2.5	2.5	2.5	2.5
V_{OL}(MAX)	0.5	0.5	0.5	0.4
High Level Noise Margin ($V_{OH}-V_{IH}$)	0.5	0.5	0.5	0.5
Low Level Noise Margin ($V_{IL}-V_{OL}$)	0.3	0.3	0.3	0.4

*Actual specification for $V_{OH(min)}$ is V_{CC} − 2 V.

elements are practically impervious to ac noise. However, large dc voltages could cause noise problems. Systems with triggerable storage elements or those operating fast enough for the noise to appear as a signal are much more susceptible to noise.

The noise voltage must be radiated or coupled into the circuit. The amount of noise required to develop a given voltage is a function of the circuit impedance. Because of the low output impedance of TTL circuits, noise immunity is improved. Noise is transferred from the source (with some arbitrary impedance) through a coupling impedance to the impedance of the circuit under consideration.

Figure 25 shows a circuit where the coupling impedance is stray capacitance and the load impedance is provided by the gates. The relatively tight coupling of this circuit and the loading effect on the driving source is significant enough

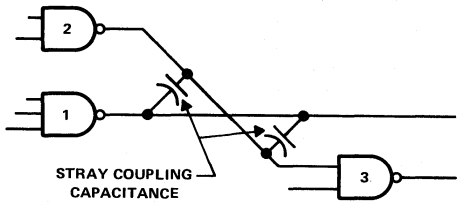

Figure 25. Stray Coupling Capacitance

to be considered. However, since the source effect is difficult to assess and is in a direction to improve rather than degrade the noise rejection, its effects are ignored. This results in a worst-case type of response indication. In the case of radiated noise, the source resistance is a definite factor in noise coupling and essentially replaces the reactive coupling impedance.

By ignoring the driving source impedance to make conditions more nearly standard, it is possible to determine a set of curves relating the developed noise pulse to the noise source amplitude, the noise rise or fall time, the coupling impedance, and the load impedance. Curves have been developed[1] for several different input waveforms. Since the 'ALS waveform is essentially a ramp with a dv/vt of 1 V/ns (approximately 2.5 V/ns for 'AS), the most applicable curve is that for a ramp input.

Figure 26(a) shows the equivalent circuit from which the ramp response plot in Figure 26(b) was developed. The input pulse (shown as a heavy line) is a step signal with a liner rise requiring unit time (normalized). The output pulse is represented analytically by

$$e_0 = \tau(1 - e^{-t/\tau})$$
$$\tau = RC$$

with holding for unit time. This is followed by an exponentially decaying voltage with a time constant τ. Values of τ and i on the figure are normalized by the value of the total rise time of the stimulated noise pulse e_i. Using Figure 26(b), the pulse width and amplitude of the coupled noise pulse can be estimated.

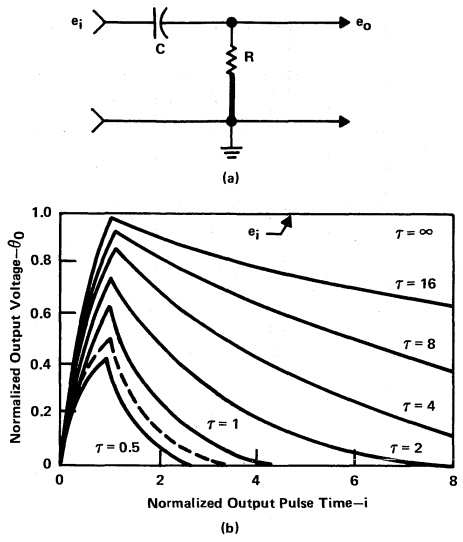

Figure 26. Evaluations of Gate Response to Fast Input Pulses

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As an example, using the circuit shown in Figure 25, apply a noise pulse of 3 V in amplitude and rising at 1 V/ns with gate 2 at a high-logic state. Assume a nominal output impedance of 58 Ω (30 Ω for 'AS) and coupling capacitance of 10 pF. Use the following formula:

$$\tau = RC = (10 \times 10^{-12})(58)$$
$$= 0.58 \times 10^{-9} = 0.58 \text{ ns}$$

$$\text{Total rise time} = \frac{3 \text{ V}}{1 \text{ V/ns}^{**}} = 3 \text{ ns}^{\dagger}$$

**2.5 V/ns for 'AS

†1.2 ns for 'AS

To convert the normalized values of τ and i in Figure 26(b) to actual values, multiply by 3 ns. The output voltage scale will be multiplied by 3 V. Using the $\tau = 0.58$ curve gives a peak e_0 of 1.5 V (0.5 × 3) and a pulse width of 3 ns at the 50% points. To determine whether this pulse will cause interference, enter these values (1.5 V and 3 ns) on the graph shown in Figure 27. Since the gates have approximately 1.8 V of noise immunity at this point, they should not be affected.

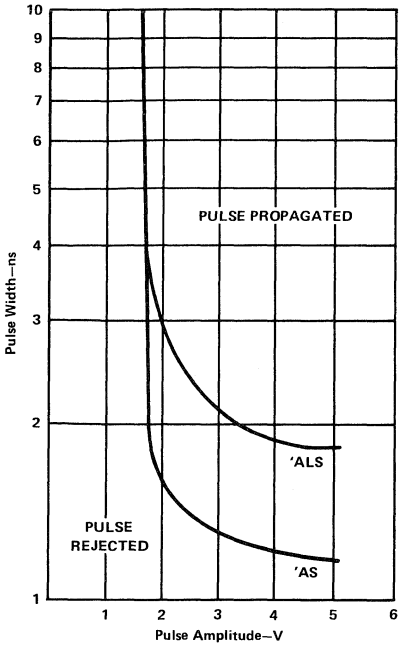


Figure 27. Theoretical Required Pulse Width vs Pulse Amplitude for 'AS and 'ALS Inputs

If an open-collector gate is used with a passive 1 kΩ pull-up resistor, the situation would change. Use the following formula:

$$\tau = (10 \times 10^{-12})(1 \times 10^{3}) = 10 \times 10^{-9} = 10 \text{ ns}$$

$$\text{Total rise time} = \frac{3 \text{ V}}{1 \text{ V/ns}^{**}} = 3 \text{ ns}^{\dagger}$$

**2.5 V/ns for 'AS

†1.2 ns for 'AS

Now the amplitude (from the curves) approaches 3 V (0.96 × 3) and the pulse width at the 50% points is approximately 10 ns (1 × 10). The next gate will propagate this pulse.

This example is an oversimplification. The coupling impedances are complex (but resolvable into RLC series coupling elements) and the gate output impedance changes with load. Our purpose is to show why and how the low impedance of the active TTL output rejects noise and to make a comparison with a passive pull-up.

The ability to operate in a noisy environment is an interaction of the built-in operating margins, the time required for the device to react, and the ease with which a noise voltage is developed. In all cases, except the ability to react to short noise pulses, the TTL design has emhasized noise rejection.

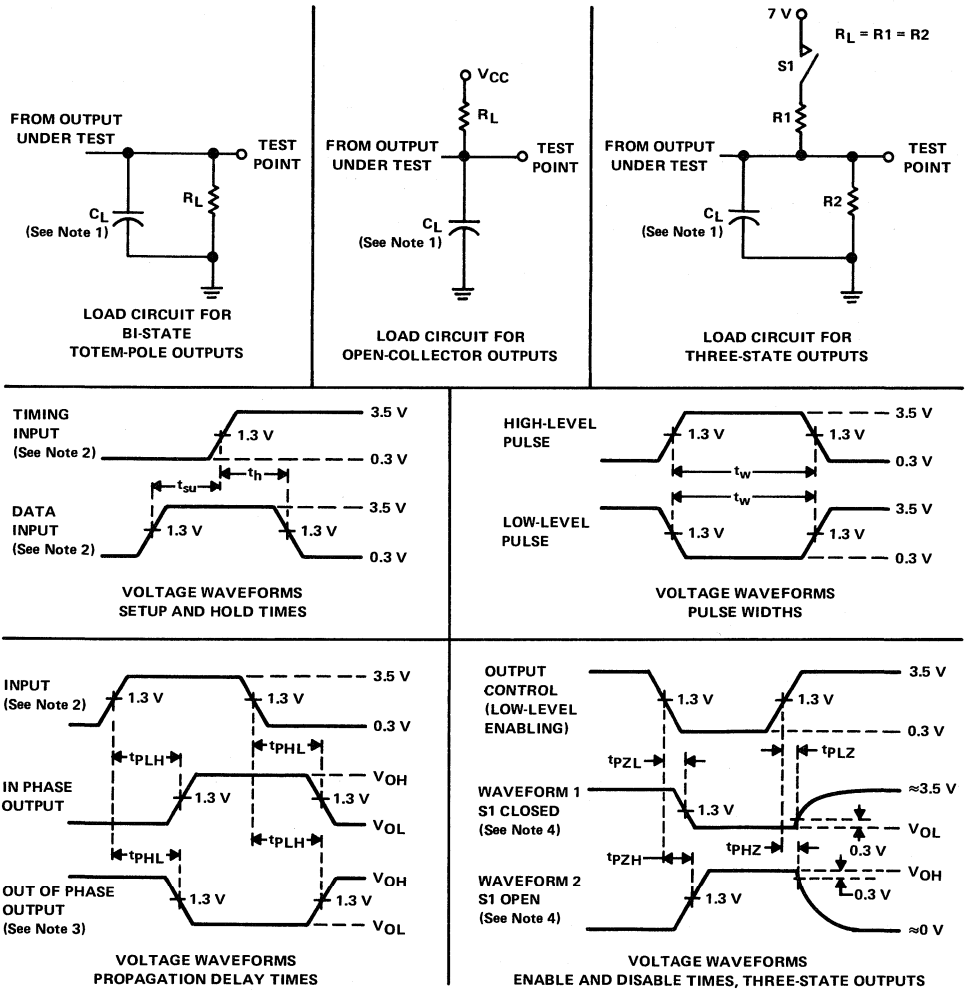
Nothing has been discussed concerning noise in devices other than gate circuits. Many MSI devices are complex gate networks and, because of their small size, are more superior

Table III. Guidelines for Systems Design for Advanced Schottky TTL

ITEM	GUIDELINE
Single wire connections	Wire lengths up to approximately 12 inches may be used. A form of ground plane is desirable. Use point-to-point routing rather than parallel. If the wire is longer than 12 inches, use either a dense ground plane with the wire routed as close to it as possible, or use a twisted-pair cable.
Coaxial and twisted-pair cables	Design around approximately 80 Ω to 100 Ω of characteristic impedance. Cross talk increases at higher impedances. Use a coaxial cable of 93 Ω impedance (e.g., Microdot 293–3913). For twisted-pair cable, use number 26 or number 28 wire with the insulation twisted at the rate of 30 turns per foot.
Transmission-line-ground	Ensure that transmission-line ground returns are carried through at both transmitting and receiving ends. V_{CC} decoupling ground, device ground, and transmission-line ground should have a common tie point.
Cross talk	Use point-to-point back-panel wiring to minimize noise pickup between lines. Avoid long unshielded parallel runs. However, if they must be used, they should carry signals that propagate in the same direction.
Reflections	Reflections occur when data interconnects become long enough that 2-line propagation delays are pulse transition times. For series TTL, reflections are normally of no importance for lines shorter than 12 inches.
Resistive pull-up	If fanout of driving output permits, use approximately 300 Ω of resistive pull-up at the receiving end of long cables. This provides added noise margin and more rapid rise times.

in a noisy environment operation than their discrete gate equivalents. Noise tolerance of latching devices is implied in the setup times, hold times, clock pulse width, data pulse widths, and similar parameters. Output impedances and input noise margins are quite similar to those of the gates and may be treated in a similar manner. If a latching device does become noise triggered, the effective error is stored and does not disappear with the noise.

Parameter measurement information is shown in Figure 28.



NOTES: 1. C_L includes probe and jig capacitance.
2. All input pulses have the following characteristics PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
3. When measuring propagation delay times of 3-state outputs, switch S1 is open.
4. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure 28. Parameter Measurement Information

GUIDELINES FOR SERIES 'ALS/'AS TTL SYSTEM DESIGN

System layout and design requirements for Advanced Schottky TTL circuits are essentially the same as those guidelines which have previously been established and are applicable for all high-performance digital systems. Tables III through VI provide a brief summary of the solutions to most design decisions needed to implement systems using Advanced Schottky TTL. Supplementary data which may be useful for developing specific answers to unique problems is provided later.

POWER SUPPLY REGULATION

Power supply regulation cannot be treated as if it is an independent characteristic of the device involved. Power supply regulation, along with temperature range, affects noise margins, fanout, switching-speed, and several other parameters. The characteristics most affected are noise margin and fanout. When these two parameters are within the specified limits, the power-supply regulation will normally be within specified limits. However, on a device where auxiliary parameters are more critically specified, a more restrictive power-supply regulation is normally required. When power-supply regulation is slightly outside the specified limits for TTL devices, the device may still operate satisfactorily. However, if high ambient-noise levels and extreme temperatures are encountered, failures may occur.

Application of a supply voltage above 7 V (absolute maximum rating) will result in damage to the circuit.

Since power dissipation in the package is directly related to supply voltage, the maximum recommended supply voltage for TTL devices is specified at 5.5 V. This provides an adequate margin to ensure that functional capability and long-term reliability are not jeopardized.

High-level output voltage is almost directly proportional to supply voltage (i.e., a drop in supply voltage causes a drop in high-level output voltage and an increase in supply voltage results in an increase in high-level output voltage). Because of this relationship, high-level output voltage for 'ALS/'AS devices is specified as supply voltage -2 V (V_{CC} -2 V).

Since high-level output voltage is directly related to supply voltage, the output current of the device is also directly related. The output current value is established by choosing output conditions to produce a current that is approximately one-half of the true short-circuit current.

It is advantageous to regulate or clamp the maximum supply voltage at 5.5 V including noise ripple and spikes. When this conditions exists, unused AND and NAND gates can be connected directly to the supply voltage.

SUPPLY VOLTAGE RIPPLE

Ripple in the supply voltage is generally considered a part of the supply voltage regulation. However, when combined with other effects (e.g., slow rise times), ripple voltage is more significant.

The effect of ripple voltage V_R can appear on either the supply voltage V_{CC} or the ground supply GND. When ripple appears on the supply voltage, it causes modulation of the input signal. The extent of the effect depends upon circuit parameters and source impedance.

The turning on of transistor Q5, shown in Figures 12 and 13, is controlled by the voltage at the base of transistor Q2 with respect to ground in accordance with the formula:

$$V_B = V_{BE} \text{ of Q2} + V_{BE} \text{ of Q3} + V_{BE} \text{ of Q5}$$

Table IV. Guidelines for Printed Circuit Board Layout for Advanced Schottky TTL

ITEM	GUIDELINE
Signal connections	Whenever possible, distribute loads along direct connections. Signal leads should be kept as short as possible. However, lead lengths of up to 15 inches will perform satisfactorily. This is especially for large boards that use a ground plane, ground, and/or V_{CC} plane. In addition, it will perform satisfactorily for small boards using ground mesh or grid. In high-frequency applications, avoid radial fanouts and stubs. If they must be used to drive some loads, reduce lead length proportionally and avoid sharp bends. Normal on-board fanouts and interconnections do not require terminations. Response of lines driving large numbers or highly capacitive loads can be improved with terminations of 300 Ω to V_{CC} and 600 Ω to ground in parallel with the last load if fanout of the driving output permits.
Conductor widths	Signal-line widths down to 0.015 inch are adequate for most signal leads.
Signal-line spacing	Signal-lead spacing on any layer down to 0.015 inch can be used especially if care is taken to avoid adjacent use of maximum length and minimum spacing. Increase spacing wherever layout permits. Pay particular attention to clock and/or other sensitive signals.
Insulator material	Thickness of insulation material used for a multilayer board is not critical. If ground and V_{CC} planes or meshes are used, their capacitive proximity can be used to reduce the number of decoupling capacitors needed and this also supplements the supply bypass capacitor.

Table V. Guidelines for General Usage of Advanced Schottky TTL

ITEM	GUIDELINE
Power supply	For RF bypass supply primary, maintain ripple and regulation at less than or equal to 10%.
V_{CC} decoupling	Decouple every 2 to 5 packages with RF capacitors of 0.01 to 0.1 μF. Capacitors should be located as near as possible to the decoupled devices. Decouple line driving or receiving devices separately with 0.1 μF capacitors between V_{CC} and the ground pins.
On-board grounding	A ground plane is essential when the PCB is relatively large (over 12 inches). Smaller boards will work with ground and/or V_{CC} mesh or grid.
System grounding	Try to simulate bus bars with a width to thickness ratio greater than or equal to 4. This can be accomplished by multiple parallel wires or by using flat braid. Performance will be enhanced when a copper or silver-copper bus is used. The width to thickness ratio required will vary between systems, but greater than or equal to 4 will satisfy most systems.

Table VI. Guidelines for Gates and Flip-Flops Using Advanced Schottky TTL

ITEM	GUIDELINE
Data input rise and fall times	Reduce input rise and fall times as driver output impedance increases. Rise and fall times should be equal to or less than 50 ns/V and essentially free of noise ripple.
Unused input of AND and NAND gates and unused preset and clear inputs of flip-flops	Tie the unused input of AND and NAND gates and the unused preset and/or clear inputs of flip-flops as follows: 1. Directly to V_{CC}, if the input voltage rating of 5.5 V maximum is not exceeded. 2. Through a resistor equal to or greater than 1 kΩ to V_{CC}. Several inputs can be tied to one resistor. 3. Directly to a used input of the same gate, if maximum fanout of driving device will not be exceeded. Only the high-level loading of the driver is increased. 4. Directly to an unused gate output, if the gate is wired to provide a constant high-level output. Input voltage should not exceed 5.5 V.
Unused input of NOR gates	Tie unused input to used input of same gate, if maximum fanout of driving device will not be exceeded or tie unused input to ground.
Unused gates	Tie input of unused NAND and NOR gates to ground for lowest power drain. Tie inputs of unused AND gates high and use output for driving unused AND or NAND gate inputs.
Increasing gate/buffer fanout	Connect gates of same package in parallel.
Clock pulse of flip-flops	Drive clock inputs with a TTL output. If not available, rise and fall times should be less than 50 ns/V and free of ripple noise spikes.

5

When ripple voltage is modulated onto the input voltage, the amplitude depends on the source impedance (Figure 29). The amplitude can be determined by the following equation:

$$\Delta V_R = V_R\left(\frac{R1/\beta}{R1/\beta + R2}\right)$$

$$= V_R\left(\frac{R1}{R1 + \beta R2}\right)$$

where R1 = source impedance
β = gain of transistor Q1.

Ripple voltage has the effect of adding extra pulses to the input signal (Figure 30). When ripple voltage appears in the ground supply, the threshold voltage is modulated and extra pulses occur (Figure 31).

Although decreasing the source impedance will reduce the effects of ripple voltage, it cannot be eliminated entirely because the emitter-base junction has an apparent resistance of approximately 30 Ω. Because of cancellation between the

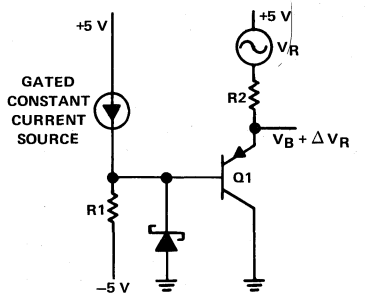


Figure 29. Effect of Source Impedance on Input Noise

driving gate and the driven gate, low-frequency ripple is not a problem.

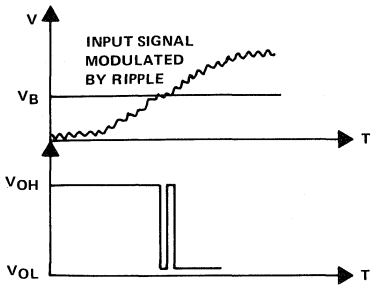


Figure 30. Spurious Output Produced by Supply Voltage Ripple

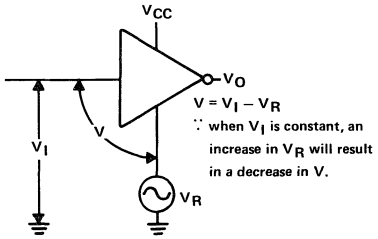


Figure 31. Effect of Ground Noise on Noise Margin

NOISE CONSIDERATIONS

Extraneous voltages and currents (called noise) introduced into a digital logic circuit are discussed in the following paragraphs. Figure 32(a) is a typical digital logic circuit consisting of a NAND gate and a J-K flip-flop. When a small noise pulse is coupled onto the clock input [(Figure 32(b)], the flip-flop does not respond and the Q output is correct. However, when a large noise pulse is coupled onto the clock input [(Figure 32(c)], the flip-flop sees the pulse as a clock transition and an erroneous Q output occurs. Therefore, it is essential to protect digital logic circuits from noise.

Noise Types and Control Methods

The noise types encountered in digital logic systems, their source, and the method of controlling them are as follows:

1. External noise — External noises radiated into the system. The sources include circuit breakers, motor brushes, arcing relay contacts, and magnetic-field-generating. The methods of controlled to be considered are shielding, grounding, or decoupling.
2. Power-line noise — Noise coupled through the ac or dc power distribution system. The initial sources and controlling methods are the same as for external noise.
3. Cross talk — Noise induced into signal lines from adjacent signal lines. Controlling methods to consider are shielding, grounding, decoupling, and, where possible, increasing the distance between the signal lines.
4. Signal-current noise — Noise generated in stray impedances throughout the circuit. The controlling methods to consider are shielding, grounding, decoupling, and, where possible, reduction of stray capacitance in the circuit.
5. Transmission-line reflections — Noise from unterminated transmission lines that cause ringing and overshoot. The method of control is to use, where possible, terminated transmission lines.
6. Supply-current spikes — Noise caused by switching several digital loads simultaneously. The controlling method is to design, where possible, the system so that digital loads are not switched simultaneously.

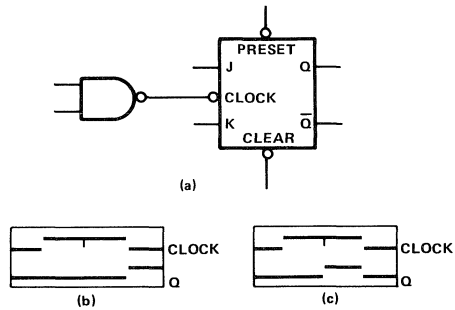


Figure 32. Typical Logic Circuit with Noisy Input

Shielding

In addition to its own internally generated noise, electrical equipment must operate in an extremely noisy environment. Noise pulses, which may come from a number of sources, consist of an electrostatic field, and electromagnetic field, or both. The noise waveform must be prevented from entering the equipment. This is accomplished by shielding. Since the noise fields are usually changing at a rapid rate, the shield required to exclude them may be very small. For effective exclusion, the sensitive circuits must be completely shielded.

Aluminum or similar materials are effective in stopping electrostatic noise. However, only a ferrous metal can successfully protect equipment against magnetic fields. While it is helpful to connect the system to earth ground, the shield

system must be complete and must be grounded to the system ground to prevent the shield from coupling noise into the system.

External noise may be conducted into the system by the power lines. Decoupling and filtering of these lines should be standard design procedure.

Grounding and Decoupling

The total propagation delay is of secondary importance in generation of internal noise. The actual transition time determines the amplitude and frequency spectrum of the generated signal at the higher harmonics. Application of the Fourier integral to series 'ALS/'AS waveforms shows frequency components of significant amplitude that exceed 100 MHz. Because of the frequency spectrum generated when an 'ALS/'AS device switches, a system using these devices must consider problems caused by radio frequency (RF) even though the repetition rates may be only a few megahertz. The transient currents generated by charging capacitors, changes in the levels of dc, line driving, etc., must be considered. In Figure 33 for example, a gate driving a transmission line is represented by a voltage source E, having an output impedance Z_S connected to an impedance Z_0, and loaded with a resistance R_L.

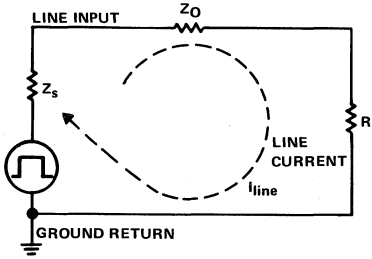


Figure 33. Diagram Representing a Gate Driving a Transmission Line

Until after a reflected pulse returns from the termination of the transmitting device, line termination is not a factor in drive current. In a practical TTL circuit, the line termination must be high relative to the line impedance. For explanation purposes, assume that the source voltage is 5 V in amplitude, the output impedance of the source is 50 Ω and the line impedance is 50 Ω. When the source voltage makes the transition from 0 V to 5 V, the voltage across the input of the line V_I is determined by the following equation:

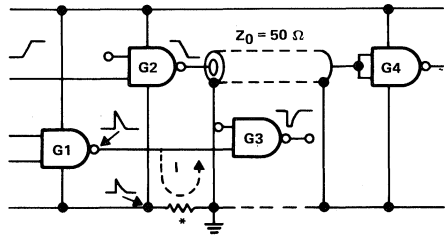
$$V_I = E \frac{Z_0}{Z_S + Z_0} = 2.5 \text{ V}$$

where E = source voltage
Z_0 = line impedance
Z_S = source impedance

For the 50 Ω line to become charged, the current that must flow onto the line is determined by the following equation:

$$I_{line} \frac{V_{in}}{Z_0} = \frac{2.5}{50} = 50 \text{ mA}$$

In addition, this current flows in the ground return, which, in this case, is the transmission-line ground. If the line and return are originated and terminated close to the driving and receiving devices, there is no discontinuity in the line. Where the ground is poorly returned, the current flow sees the discontinuity in the cable as a high impedance and a noise spike is generated (i.e., the ground current sees a low impedance and a current cancellation if the ground is properly carried through and, if not, it sees a high impedance). Figure 34 presents a specific example. Assume that the gate driving the line is switched from the high to low state. Current flow is indicated by the arrow marked with an I. Since the line is improperly returned to the driver, a pulse is developed across the impedance. A possible consequence is the false output of gate 3 (G3).



*Impedance of poor ground return

Figure 34. Noise Generation Caused by Poor Transmission-Line Return

If the ground return is properly connected, the proper results are obtained. The impedance discontinuity is eliminated and current cancellation occurs at the ground point. Undesirable voltage spikes are then eliminated. Two empirical rules to reduce transmission-line currents have been established and have been found to be effective (Figure 35).

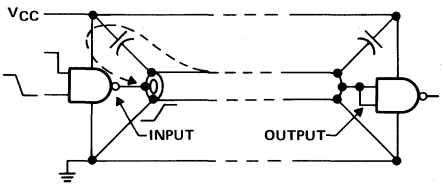
1. Carry all returns, including twisted pair and coaxial cables, to a good ground termination. Ground line returns close to the driving and receiving devices.
2. Decouple the supply voltage of line-driving and line-receiving gates with a 0.1-μF disk ceramic capacitor.

As the devices change state, current levels change because of the different device currents required in each state, the external loading, the transients caused by charging and

discharging capacitive loads, and the conduction overlap in the totem-pole output stage. When a gate changes states, its internal supply current changes from high to low (these values are stated on the data sheet for each device). In addition, any capacitance, stray or otherwise, must be charged or discharged for a logic state change. The capacitance must be charged by a current determined by

$$I = C \frac{dv}{dt} \quad (4)$$

If the total stray capacitance on a gate output, the logic-level voltage excursion, and the associated rise or fall times are known, then the ideal-case instantaneous current during the transition can be calculated.

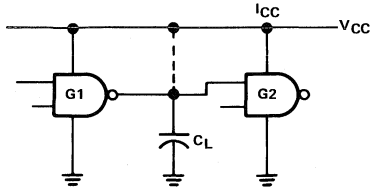


Broken arrow shows path of line-charging current

Figure 35. Ideal Transmission-Line Current Handling

From Eq. (4) it can be determined that the current transient for charging load capacitance will increase with higher speed TTL circuits. Therefore, the Series 54ALS/74ALS devices will have lower transient current than the Series 54AS/74AS devices. Another parameter that should be considered is the value of R7 (shown in Figures 12 and 13). Resistor R7 acts as a limit on the charging current.

The current required for charging load capacitance C_L (Figure 36) is supplied by the supply voltage when the transition is from logic low to logic high at the output of gate 1 (G1). When the output of G1 goes from high to low, the load capacitance is shorted to ground by transistor Q5 (shown in Figures 12 and 13) and has no effect on supply current.



C_L includes all capacitance: stray, device, etc.

Figure 36. Circuit with Effective Capacitive Loading

A characteristic common to all TTL totem-pole output stages contributes an additional current transient when the output changes from a logic low to a logic high. This transient, or spike, is caused by the overlap in conduction of the output transistors Q7 and Q5 (shown in Figures 12 and 13). The situation arises because transistor Q7 can turn on faster than transistor Q5 can turn off. This places a direct circuit consisting of transistors Q7 and Q5 and resistor R4 between supply voltage and ground. For all series 'ALS TTL circuits, the maximum possible peak current can be determined by

$$I_{CCmax} = \frac{V_{CC} - V_{CEQ6} - V_{BEQ7} - V_{CEQ5}}{R7}$$

However, due to the active turnoff circuit (consisting of R5, R6, and Q4), Q5 will be only slightly in the linear region and the current spike will be less.

The total supply-current switching transient is then a combination of three major effects: the difference in high-level and low-level supply current, the charging of load capacitance, and the conduction overlap. Tests were performed to demonstrate these effects. The results are shown in Figure 37. Six types of series TTL devices were tested with no load (i.e., the oscilloscope was connected to the output only when measuring V_O and the photographs were double exposed). This was to approximate the effects of conduction overlap isolated from the transient caused by charging load capacitance. Different vertical scales were used on some of the photographs.

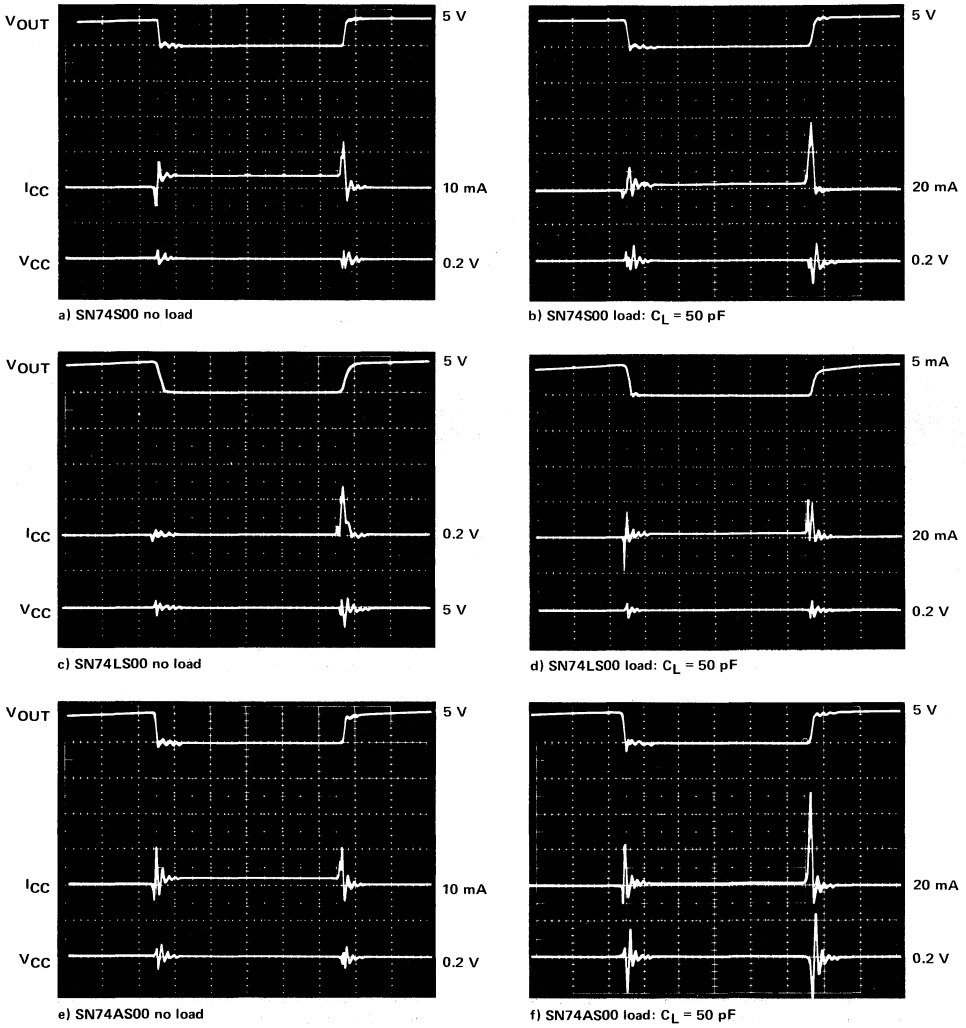
The results are almost as predicted. The low-power devices have the lower transients. Since it is the fastest circuit, the SN74AS00 device should be highest. However, a decrease is shown, and the reason for the decrease is explained (Figure 39). The additional circuits to reduce conduction overlap of the output transistors result in a smaller transient even though the typical switching time is 1.7 ns compared to 9 ns for the Series 54/74LS.

The second series of tests shown in Figure 37 cover a capacitive load of 50 pF. For this test, all of the supply current transient peaks increase in amplitude and width.

Because of the larger transient currents, voltage spikes on the supply voltage measured at the IC package are also increased.

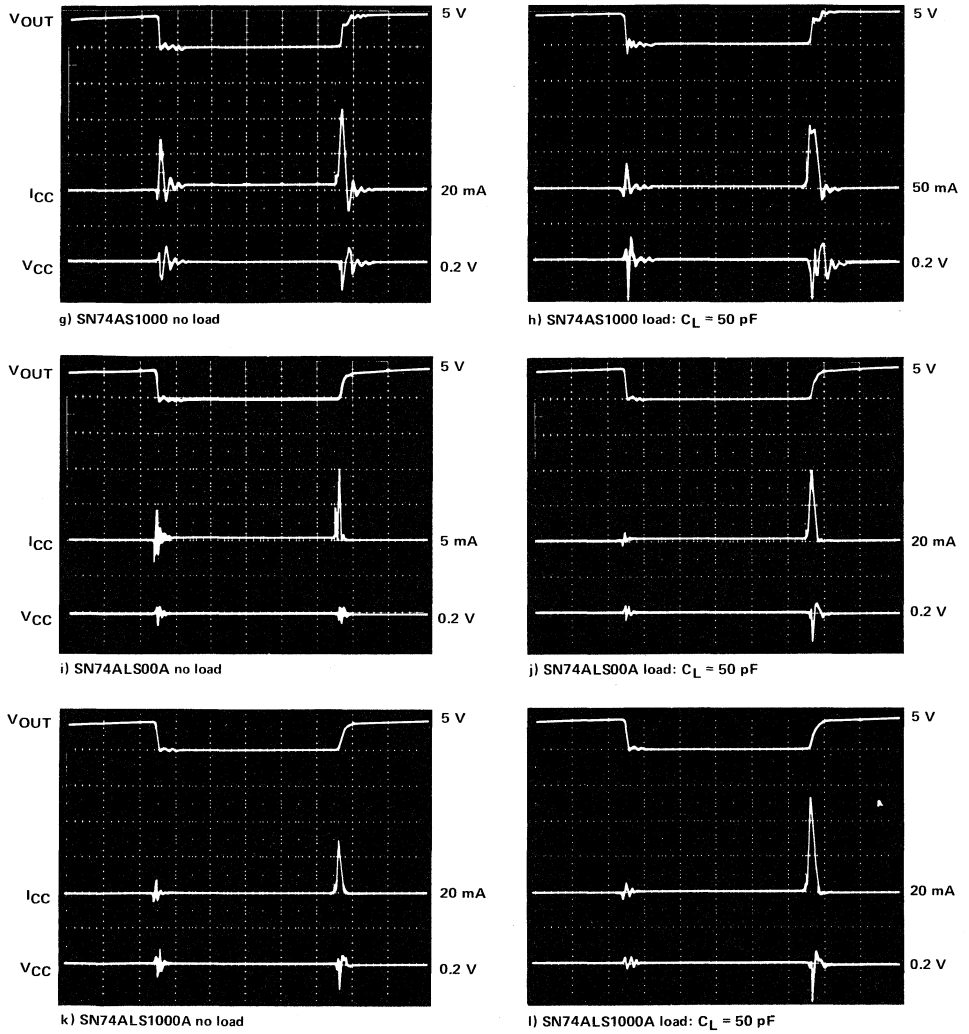
From these tests, it can be concluded that the condition to be avoided (the only one that can be avoided) is unnecessary stray capacitance in circuit wiring. The charging of load capacitance, in most cases, overshadows the other two effects with respect to noise produced on the supply voltage line by switching current transients.

The flow paths of these currents have been investigated to determine the grounding and decoupling necessary to counteract their effects. Supply voltage decoupling may be accomplished by one of two methods. Maintaining low impedance from the individual circuit supply voltage to



NOTES: 1. V_{CC} = 5 V
2. Sweep is 50 ns/division
3. Rise and fall times of input pulse are 1 ns
4. Vertical scales are in units shown per division

Figure 37(a). Supply-Current Transient Comparisons



NOTES: 1. V_{CC} = 5 V
2. Sweep is 50 ns/division
3. Rise and fall times of input pulse are 1 ns
4. Vertical scales are in units shown per division

Figure 37(b). Supply-Current Transient Comparisons

ground is common to both methods. In the first method, the supply voltage line may be considered as a transmission line back to a low impedance supply. The positive bus can be laminated with a ground bus to form a strip transmission line of extremely low impedance. This line can be electrically approximated with lumped capacitances as shown in Figure 38. The inductances are usually a distributed component which must be minimized to lower the line impedance.

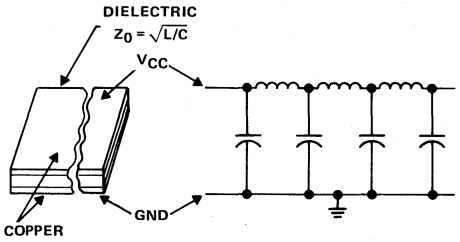


Figure 38. Transmission-Line Power Buses

The second method is to consider the supply voltage bus as a dc connecting element only and to provide a low-impedance path near the devices for the transient currents to be grounded (Figure 39).

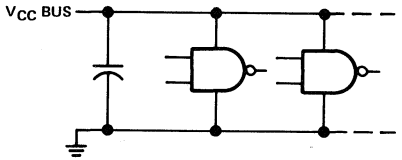


Figure 39. Capacitive Storage Supply Voltage System

For effective filtering and decoupling, the capacitors must be able to supply the change in current for a period of time greater than the pulse width of this current. Since the problem is essentially one of dc changes due to logic state coupled with high-frequency transients associated with the changes, two different values of time constant must be considered. Capacitors combining the high capacitance required for long periods with the low series reactance required for fast transients are prohibitive in cost and size. A good compromise is the arrangement shown in Figure 40.

The typical component values may be found for the RF capacitor C2 by assuming that the parameters have common values as follows:

$\Delta I_{CC} = 50$ mA
$\Delta V = 0.1$ V
$\Delta T = 20$ ns

Then the equation is as follows:

$$C2 = \frac{\Delta I_{CC}}{\Delta V/\Delta T} = \frac{(50)(20) \times 10^{-12}}{0.1/(20 \times 10^{-9})}$$

$$= \frac{50 \times 10^{-3}}{0.1} = 10{,}000 \times 10^{-12}$$

$$= 0.01\ \mu F$$

The same method may be used for the low-frequency capacitor C1. However, the factor ΔT, which was a worst-case transient time for calculating C1, now becomes a bit ambiguous. An analysis of the current cycling on a statistical basis is the best method in all but the simplest systems. The recommended procedure is to decouple using 10 μF to 50 μF capacitors.

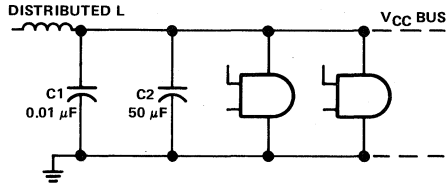


Figure 40. Commonly Used Power Distribution and Decoupling System

A discrete inductance of 2 μH to 10 μH is sometimes used for additional decoupling. However, its benefits are questionable and its usefulness should be evaluated for the individual system. The low-pass filter formed must be capable of keeping the transients confined and off the distribution bus. The possibility of resonance in the inductor or LC combination must be considered.

Noise spikes on the supply voltage line that do not force the gate output below the threshold level do not present a serious problem. Downward spikes as large as 3 V can be tolerated on the supply voltage line without propagating through the logic system. The system designer can be confident that supply voltage noise can be handled even with minimal consideration.

Ground noise, however, cannot be treated lightly. Pulses on a high-impedance ground line can easily exceed the noise threshold. Only if a good ground system is maintained can this problem be overcome. If proper attention is paid to the ground system, noise problems can be minimized.

The concept of a common-ground-plane structure as used in RF and high-speed digital systems is quite different from the concept of the common-ground point as used in low-frequency circuits. The more closely the chassis and ground can approach to being an integral unit, the better the noise suppression characteristics of the system. Consequently, all

parts of the chassis and ground bus system must be bound tightly together both electrically and mechanically. Floating or poorly grounded sections not only break the integrity of the ground system, but may actually act as a noise distribution system.

For grounds and decoupling on printed circuit boards, the most desirable arrangement is a double-clad or multilayer board with a solid ground plane or a mesh. Where component density prohibits this, the ideal should be relaxed only as far as necessary. Cross talk and ground noise can be reduced on large boards with a ground plane. Some suggestions for board grounds where a plane is not practical are as follows:

1. Use as wide a ground strap as possible.
2. Form a complete loop around the board by bringing both sides of the board through separate pins to the system ground.

The supply voltage line can provide part of the ground mesh on the board, provided it is properly decoupled. For a TTL system, a good guideline is 0.01 μF per synchronously driven gate and at least 0.1 μF for each 20 gates, regardless of synchronization. This capacitance may be lumped, but is more effective if distributed over the board. A good rule is to permit no more than 5 inches of wire between any two package supply-voltage points. Radio-frequency-type capacitors must be used for decoupling. Disk ceramics are best. It is sometimes a good practice to decouple the board from the external supply-voltage line with a 2.2 μF capacitor. However, this is optional and the RF capacitors are still required. In addition, it is recommended that gates driving long lines have the supply voltage decoupled at the gate supply voltage terminal and that the capacitor ground, device ground, and transmission-line ground be connected to a common point.

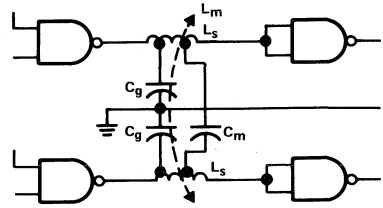
Cross Talk

When currents and voltages are impressed on a connecting line in a system, it is impossible for adjacent lines to remain unaffected. Static and magnetic fields interact and opposing ground currents flow, creating linking magnetic fields. These cross-coupling effects are lumped together and called cross talk.

Back-Panel Interconnections

Interconnecting signal lines can be grouped into three broad categories: coaxial lines, twisted-pair lines, and straight wire lines. Because of the low impedance and shielding characteristics of coaxial cable, its cross talk is minimal and is not a problem with TTL.

Figure 41 illustrates a practical type of signal transmission line. The mutual reactances L_m and C_m which form the noise coupling paths and the line parameters L_s and C_g which govern the line impedance, will vary with the type of line used. Since cross talk is a function of the ratio of the mutual impedances to the line characteristic impedances, the selection of transmission-line type must be at least partially a factor in cross-talk considerations.

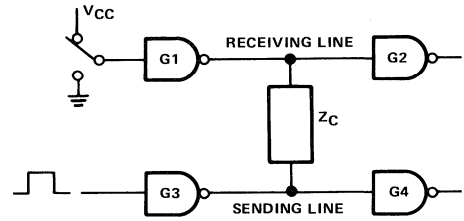


ALL GATES SN74ALS00

Figure 41. Equivalent Circuit for Sending Line

The use of direct-wired connections is the simplest and lowest cost method, but they are also the poorest for noise rejection. If the lead is not cabled tightly together with similar leads, direct leads up to 12 inches in length can be used.

When the length of the signal line is increased, the line impedance is seen by the driving and receiving gates. As shown in Figure 42, a pulse sent along the sending line G3 and G4 will be coupled via the coupling impedance Z_C onto the receiving line G1 and G2, which can be in either of the two logic states. The extent to which cross talk will occur depends on the type of lines used and their relationship to each other.



(Z_C) – COUPLING IMPEDANCE

Figure 42. Equivalent Circuit for Cross Talk

The voltage impressed on the sending line by gate G3 is determined by the equation:

$$V_{SL} = \frac{V_{G3}Z_0}{R_{S3} + Z_0} \quad (5)$$

where

V_{G3} = open-circuit logic voltage swing generated by gate G3
R_{S3} = output impedance of gate G3
Z_0 = line impedance
V_{SL} = voltage impressed on the sending line.

The relationship for the equation is illustrated in Figures 43 and 44.

The coupling from the sending line to the receiving line can be represented by taking coupling impedance Z_C into

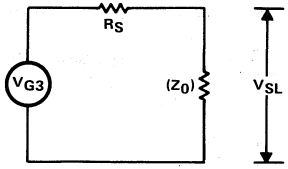


Figure 43. Capacitive Cross Talk Between Two Signal Lines

account. An equivalent circuit to represent the coupling from the sending line to the receiving line is shown in Figure 44.

As the voltage impressed on the sending line propagates farther along the line, it can be represented as voltage source V_{SL} with a source impedance of Z_{01} (Figure 45). V_{SL} is then coupled to the receiving line via the coupling capacitance, where the impedance looking into the line is line impedance in both directions. Therefore the equation becomes

$$V_{RL} = V_{SL} \frac{\frac{Z_0}{2}}{(1.5\ Z_0 + Z_c)}$$

The voltage impressed on the receiving line (V_{RL}) then propagates along the receiving line to gate G2 which can be considered as an open circuit and voltage doubling occurs. Therefore:

$$V_{in(2)} = 2\ V_{RL} = V_{G3}\left(\frac{1}{1.5 + \frac{Z_c}{Z_0}}\right)\left(\frac{Z_0}{RS3 + Z_0}\right)$$

In the switching period, the transistor has a very low output impedance. Then $R_{S3} \ll Z_0$ and $V_{in(2)}$ can be simplified to the following:

$$V_{in(2)} = V_{G3}\left(\frac{1}{1.5 + \frac{Z_c}{Z_0}}\right)$$

The term $V_{in(2)}/V_{G3}$ can be defined as the cross-talk coupling constant.

The worst-case for signal line cross talk occurs when sending and receiving lines are close together but widely separated from a ground return path. The lines then have a high characteristic impedance and a low coupling impedance.

For example, if we assume a coupling impedance of 50 pF at 150 MHz with a line impedance of approximately 200 Ω then:

$$\frac{V_{in(2)}}{V_{G3}} = 0.62$$

This level is unsatisfactory because none of the very high-speed logic circuits has a guaranteed noise margin greater than one-third of the logic swing. Such potential cross talk can be avoided by not using the close spacing of conductors.

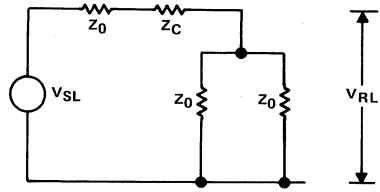


Figure 45. Equivalent Cross-Talk Network

Mutual coupling can be reduced by using coaxial cable or shielded twisted pairs. When mutual inductance and capacitance are decreased, line capacitance is increased and imposes restrictions on the driver. Coaxial cable combines very high mutual impedance with low characteristic impedance and shielding. It effectively eliminates cross talk, but is necessary in only the noisiest environments. Twisted pairs are adequate for most applications and are typically less expensive and easier to use.

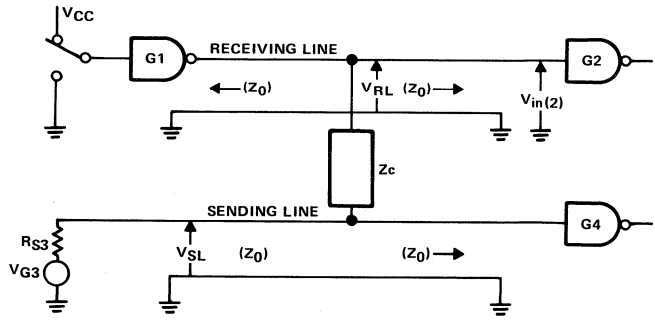


Figure 44. Coupling Impedances Involved in Cross Talk

Printed Circuit Card Conductors

Signal interconnections on a two-sided or multilayer printed circuit card can be grouped into two general categories: microstrip lines and strip lines. The microstrip line (Figure 46) consists of a signal conductor separated from a ground plane by a dielectric insulating material. A strip line (Figure 47) consists of a signal conductor within a dielectric insulating material and the conductor being centered between two parallel conductor planes. The important features of these type of printed circuit conductors are that the impedances are highly predictable, can be closely controlled, and the process is relatively inexpensive because standard printed circuit board manufacturing techniques are used. Typical impedances of these types of conductors with respect to their physical size and relative spacings are shown in Tables VII and VIII.

Table VII. Typical Impedance of Microstrip Lines

Dimensions		Line Impedance	Capacitance
H (mils)	W (mils)	Z_O (Ω)	per Foot (pF)
6	20	35	40
6	15	40	35
15	20	56	30
15	15	66	26
30	20	80	20
30	15	89	18
60	20	105	16
60	15	114	14
100	20	124	13
100	15	132	12

Relative dielectric constant ≈ 5

Table VIII. Typical Impedance of Strip Lines

Dimensions		Line Impedance	Capacitance
H'a = H'b = (mils)	W (mils)	Z_O (Ω)	per Foot (pF)
6	20	27	80
6	15	32	70
10	20	34	67
10	15	40	56
12	20	37	57
12	15	43	48
20	20	44	48
20	15	51	42
30	20	55	39
30	15	61	35

Relative dielectric constant ≈ 5, and H'a = H'b

Cross talk on a printed circuit board is also a function of the mutual reactances and the line parameters which govern the line impedance. A microstrip line and a strip line are, by definition, conductors placed relatively close to a ground plane. Therefore, they have at least one inherent property which tends to reduce cross talk. In addition, the thickness (H) of the dielectric and the spacing (S) of the conductors can be implemented selectively to reduce the amount of possible cross talk. The effects of these two dimensions on cross talk have been evaluated and are shown graphically in Figure 48. The data shown can be used to estimate the maximum crosstalk which will be encountered under the most unfavorable conditions.

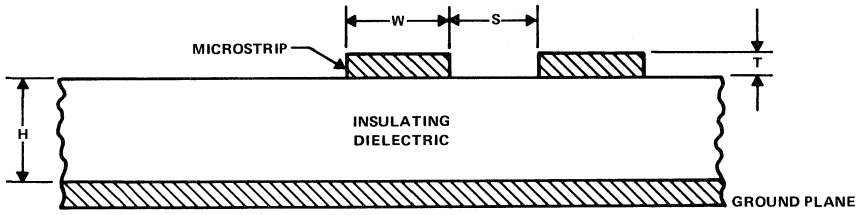


Figure 46. Microstrip Line

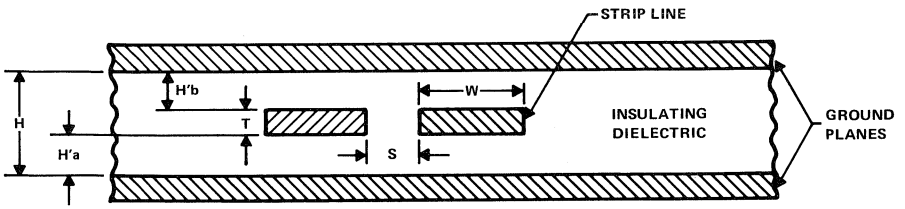


Figure 47. Strip Line

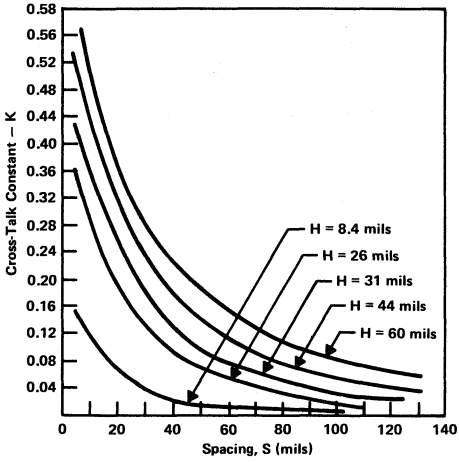


Figure 48. Line Spacing Versus Cross-Talk Constant

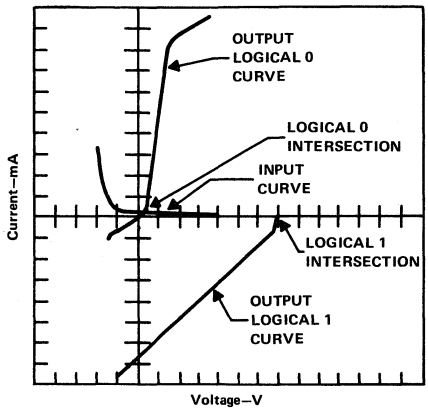


Figure 49. TTL Bergeron Diagram

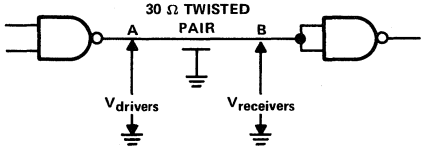


Figure 50. 'ALS/'AS Driving Twisted Pair

Transmission-Line Driving Reflections

When the interconnections used to transfer digital information become long enough so that line propagation delay is equal to or greater than the pulse transition times, the effects of reflections must be considered. These reflections are created because most TTL interconnections are not terminated in their characteristic impedance. Reflections lead to reduced noise margins, excessive delays, ringing, and overshoot. Some method must be used to analyze these reflections. Because neither the gate input nor output impedance is linear, basic transmission-line equations are applicable but unwieldy. Transmission-line characteristics of TTL interconnections can be analyzed by using a simple graphic technique.

Figure 49 shows piecewise linear plots of a gate input and both (logic-high and logic-low) states of the output for a typical TTL device. The output curves are plotted with positive slopes. The input is inverted because it is at the receiving end of a transmission line. The logic-high and logic-low intersections are indicated on the plot. These points are the steady-state values which will be observed on a lossless transmission line (Figure 50).

Figure 50 shows a typical TTL interconnection using a twisted-pair cable which, in this example, has a characteristic impedance of approximately 30 Ω. To evaluate a logic-high to logic-low 'AS transition see Figures 51 and 52. The equation $-1/Z_0$ (Z_0 = 30 Ω), which represents the transmission line, is superimposed on the output characteristic curves in the Bergeron plot. Since evaluation of a logic-high to logic-low transition is desired, the $-1/Z_0$ line starts at the point of intersection of the impedance curves of the input and output for a logic-high state. The slope $-1/Z_0$ then proceeds toward the logic-low output curve. At time t_0, the driver output voltage is determined by the intersection of $-1/Z_0$ and the logic-low output curve (1.2 V). The transmission-line slope now becomes $1/Z_0$ and is drawn toward the input curve. At time t_1 [$t_{(n+1)} - t_n$ = time delay of line], the receiving gate sees −1.7 V. Now the line slope changes back to $-1/Z_0$ and the output curve for a logic low is approached. This action continues until the logic-low intersection is reached. Figure 52 plots driver and receiver voltages versus time for this example.

A logic-low to logic-high transition is treated in approximately the same manner (Figure 53). The Bergeron line $-1/Z_0$ starts at the intersection for a logic low. At time t_0, the driver output rises to 2.2 V and, at time t_1, the receiving gate input goes to approximately 4.35 V. Both output and input voltages are plotted in Figure 54.

Figures 55 through 58 illustrate 'ALS transitions and are treated in the same manner as the 'AS.

The scope photographs in Figures 59 through 66 show the effectiveness of the graphic techniques. In most cases, the calculated and experimental values of voltage steps agree within reason. The ringing that appears for the open wire is not immediately obvious. This is because the input and output curves in this region lie practically along the positive horizontal axis. At the scale used for graphic analysis, it is difficult to go much beyond the first few reflections. The graphic analysis is idealized and stray capacitance and inductance are not considered.

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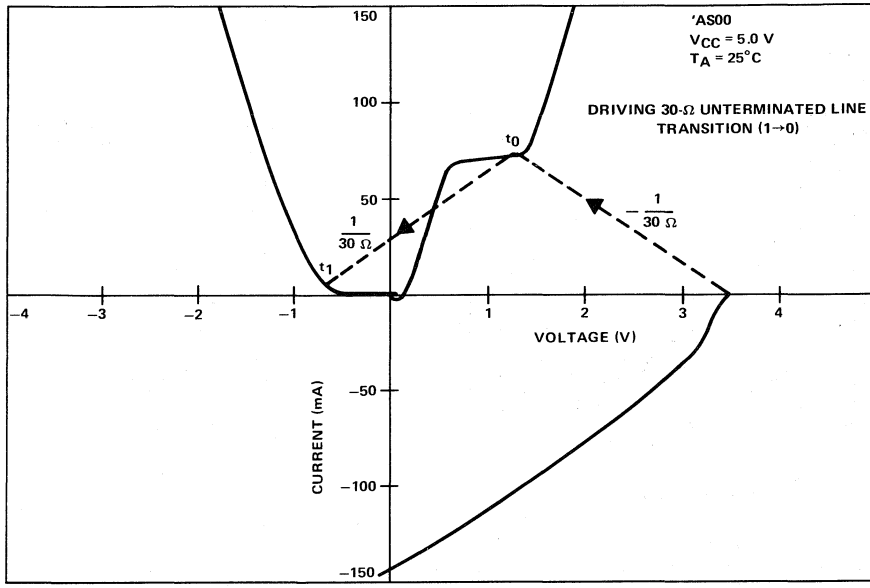

Figure 51. 'AS −ve Transition Bergeron Diagram

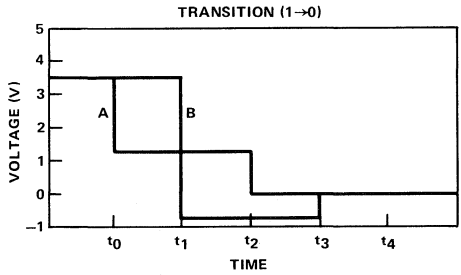

Figure 52. 'AS −ve Voltage/Time Plot

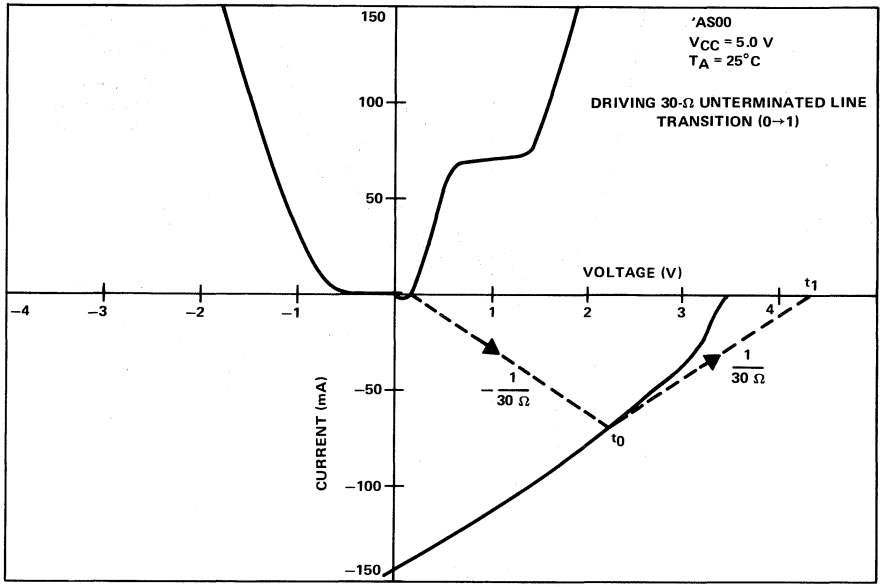

Figure 53. 'AS +ve Transition Bergeron Diagram

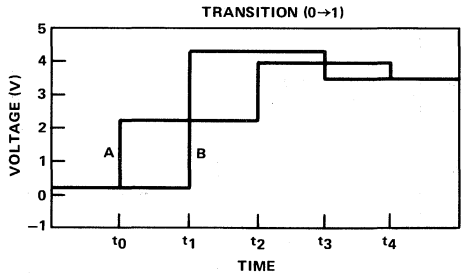

Figure 54. 'AS +ve Voltage/Time Plot

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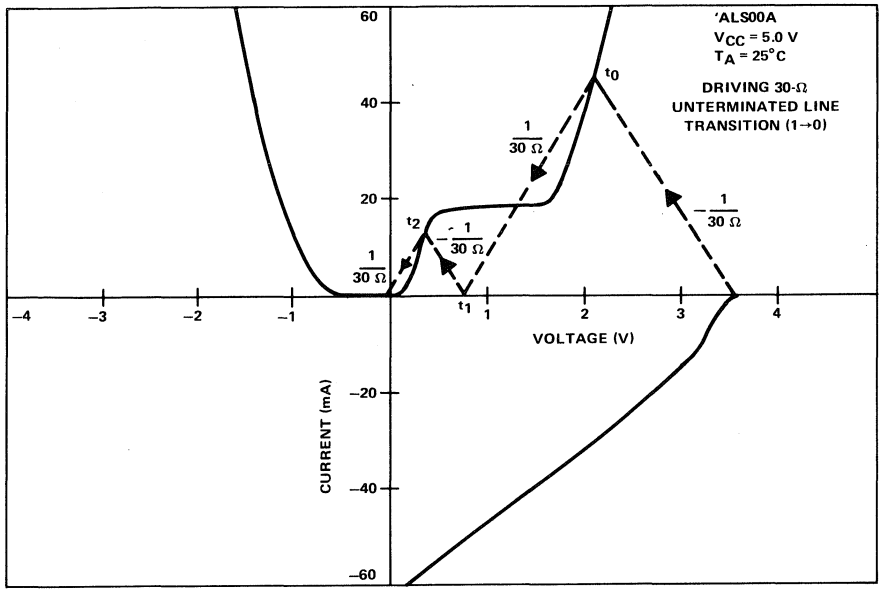

Figure 55. 'ALS −ve Transition Bergeron Diagram

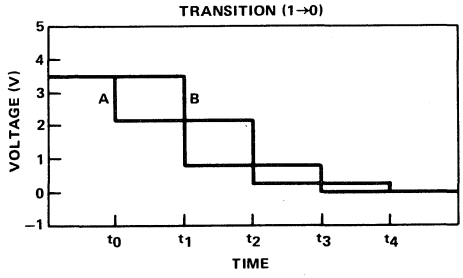

Figure 56. 'ALS −ve Voltage/Time Plot

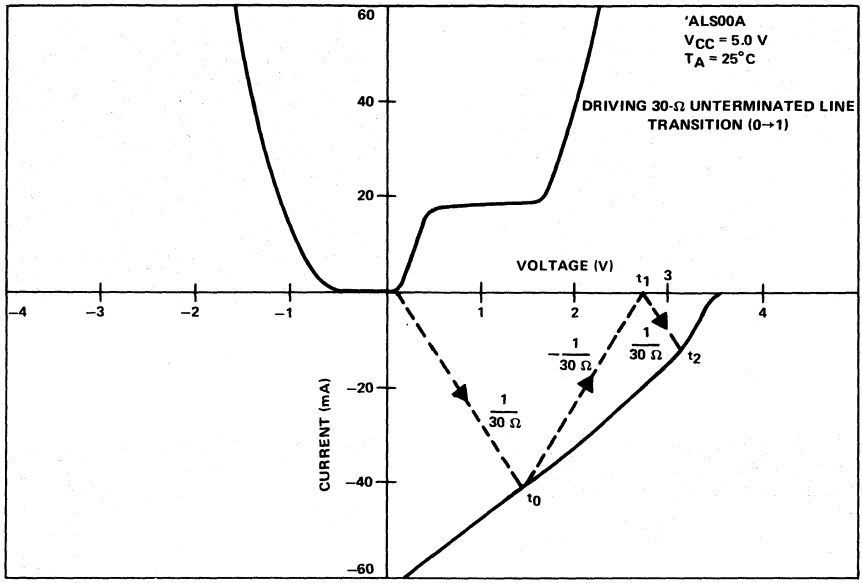

Figure 57. 'ALS +ve Transition Bergeron Diagram

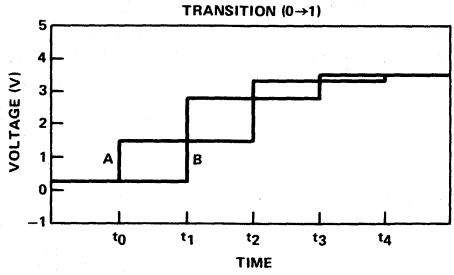

Figure 58. 'ALS +ve Voltage/Time Plot

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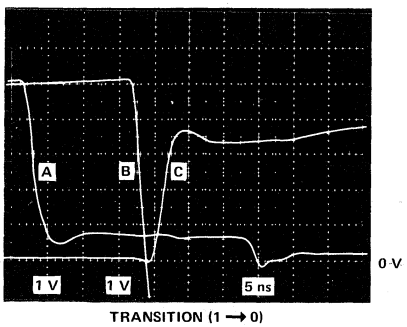

Figure 59. Oscilloscope Photograph of 'AS001 – ve Transition Using 50-Ohm Line

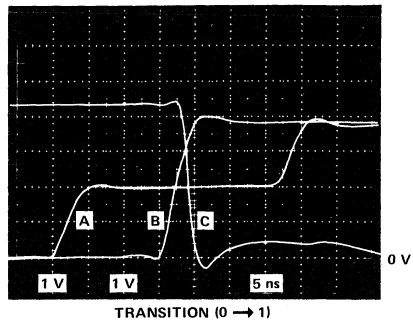

Figure 62. Oscilloscope Photograph of 'AS00 + ve Transition Using 25-Ohm Line

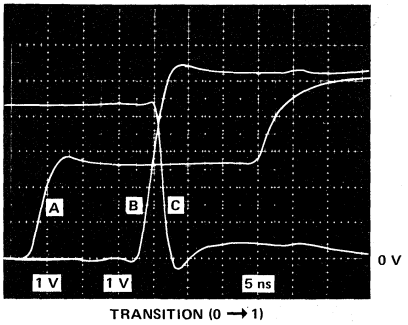

Figure 60. Oscilloscope Photograph of 'AS00 + ve Transition Using 50-Ohm Line

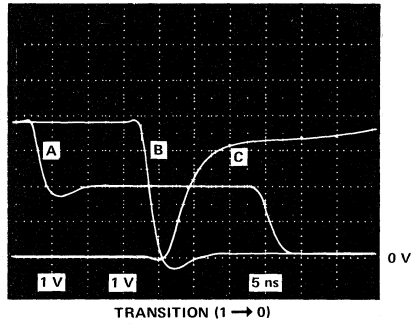

Figure 63. Oscilloscope Photograph of 'ALS00A – ve Transition Using 50-Ohm Line

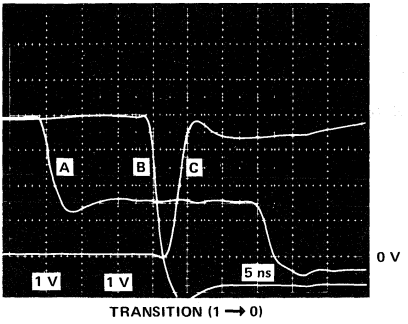

Figure 61. Oscilloscope Photograph of 'AS00 – ve Transition Using 25-Ohm Line

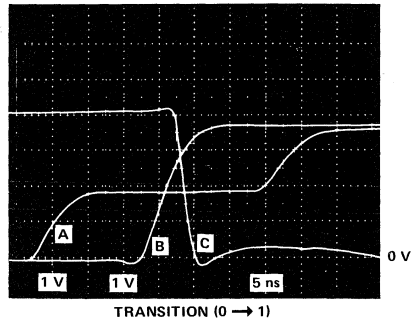

Figure 64. Oscilloscope Photograph of 'ALS00A + ve Transition Using 50-Ohm Line

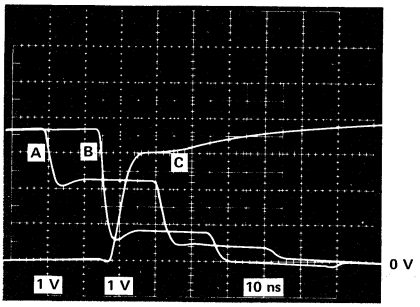

Figure 65. Oscilloscope Photograph of 'ALS00A −ve Transition Using 25-Ohm Line

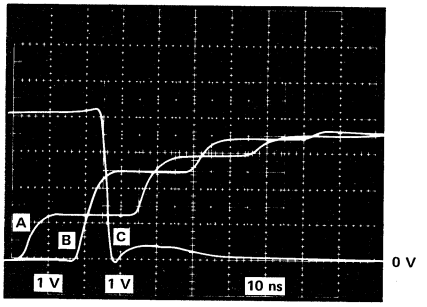

Figure 66. Oscilloscope Photograph of 'ALS00A +ve Transition Using 25-Ohm Line

References

1. W.C. Elmore and M. Sands, *Electronics Experimental Techniques,* McGraw-Hill Book Co., New York, 30ff. (1949).
2. M. Williams and S. Miller, *Series 54ALS/74ALS Schottky TTL Applications B215*, Texas Instruments Limited, Bedford, England, August 1982.

Acknowledgment

This application report is an updated version of Reference 2 with significant contributions by the technical engineering staff at Texas Instruments and particularly by Rock Cozad, Rich Moore, and Bob Strong.

Appendix A
Normalized Load Factors

Normalizing output drive capability and input current requirements can be very useful to designers of systems using two or more of the TI TTL series of devices. It provides a set of load factors (input cuurent requirements in Table A-I), which can be summed and compared directly to the fanout capability (see Table A-II) of the output being considered. The load factor values shown are valid for any input rated at one unit load.

The loading of these type of outputs can be checked from any column. However, most designs use one of the series as the basic building block and, since the tables cover each series individually, the designer has the choice of working from the column containing the normalized fanout. As an example, the designers of a system using series 'AS as the basic circuit will probably find that the use of the 'AS00 and 'AS1000 columns will suit best because both fanout and load factors are expressed for these series of devices.

The use of these simple and easy-to-remember numbers was developed within each series to make the verification of output loading a matter of counting the number of inputs connected to a particular output. When mixtures of series are used, a common denominator (normalized factor) becomes useful.

USE OF TABLES A-I AND A-II

Every possible combination of the seven 54/74 TTL families is included in these tables. If, for example, the existing system used 74S series logic and it is desired that some of it be replaced by series 74ALS logic, a quick check should be made on whether the 'ALS can be supplied with sufficient input current. By taking the 74S row and 'ALS, column figures of 2.5 and 20 are obtained for high- and low-level loads, respectively (see Table A-I). This indicates that, for high logic levels, two and one-half 'ALS gates can be driven for each 'S series gate removed. However, if more 74S series gates are being driven by this 'ALS device, the fanout between 'ALS and 'S series gate is required, you can now use Table A-II.

The 'ALS row and the 'S column are chosen. The figures are 8 for the high-logic level and 4 for the low-logic level. In this case the lowest figure is taken so that the interconnection is reliable for both logic states. So each 'ALS gate inserted will drive 4 'S series gates.

Table A-I is normally used (in combination with Table A-II) when replacing one logic family with another in an existing system.

Table A-II is normally used when originally designing a system which employs several TTL families to optimize performance.

5

Table A-I. Normalized Input Currents

SERIES	I/O	INPUT CURRENT (mA)	INPUT CURRENT NORMALIZED								
			'00	'H00	'L00	'LS00	'S00	'AS00	'ALS00A	'AS1000	'ALS1000A
54/7400	HI	0.04	1	0.8	4	2	0.8	2	2	2	2
54/7400	LO	1.6	1	0.8	8.89	4	0.8	3.2	16	3.2	16
54H/74H00	HI	0.05	1.25	1	5	2.5	1	2.5	2.5	2.5	2.5
54H/74H00	LO	2	1.25	1	11.11	5	1	4	20	4	20
54/74L00	HI	0.01	0.25	0.2	1	0.5	0.2	0.5	0.5	0.5	0.5
54/74L00	LO	0.18	0.11	0.09	1	0.45	0.09	0.36	1.8	0.36	1.8
54LS/74LS00	HI	0.02	0.5	0.4	2	1	0.4	1	1	1	1
54LS/74LS00	LO	0.4	0.25	0.2	2.22	1	0.2	0.8	4	0.8	4
54S/74S00	HI	0.05	1.25	1	5	2.5	1	2.5	2.5	2.5	2.5
54S/74S00	LO	2	1.25	1	11.11	5	1	4	20	4	20
54AS/74AS00	HI	0.02	0.5	0.4	2	1	0.4	1	1	1	1
54AS/74AS00	LO	0.5	0.31	0.25	2.78	1.25	0.25	1	5	1	5
54ALS/74ALS00A	HI	0.02	0.5	0.4	2	1	0.4	1	1	1	1
54ALS/74ALS00A	LO	0.1	0.06	0.05	0.56	0.25	0.05	0.2	1	0.2	1
54AS1000	HI	0.02	0.5	0.4	2	1	0.4	1	1	1	1
54AS1000	LO	0.5	0.31	0.25	2.78	1.25	0.25	1	5	1	5
54ALS1000A	HI	0.02	0.5	0.4	2	1	0.4	1	1	1	1
54ALS1000A	LO	0.1	0.06	0.05	0.56	0.25	0.05	0.2	1	0.2	1

Table A-II. Fanout Capability (Output Currents Normalized to Input Currents)

SERIES	I/O	OUTPUT CURRENT (mA)	OUTPUT DRIVE NORMALIZED								
			'00	'H00	'L00	'LS00	'S00	'AS00	'ALS00A	'AS1000	'ALS1000A
			*HI 0.04	0.05	0.01	0.02	0.05	0.02	0.02	0.02	0.02
			†LO 1.6	2	0.18	0.4	2	0.5	0.1	0.5	0.1
54/7400	HI	0.4	10	8	40	20	8	20	20	20	20
54/7400	LO	16	10	8	88.89	40	8	32	160	32	160
54H/74H00	HI	0.5	12.5	10	50	25	10	25	25	25	25
54H/74H00	LO	20	12.5	10	111.11	50	10	40	200	40	200
54L00	HI	0.1	2.5	2	10	5	2	5	5	5	5
54L00	LO	2	1.25	1	11.11	5	1	4	20	4	20
74L00	HI	0.2	5	4	20	10	4	10	10	10	10
74L00	LO	3.6	2.25	1.8	20	9	1.8	7.2	36	7.2	36
54LS/74LS00	HI	0.4	10	8	40	20	8	20	20	20	20
54LS00	LO	4	2.5	2	22.22	10	2	8	40	8	40
74LS00	LO	8	5	4	44.44	20	4	16	80	16	80
54S/74S00	HI	1	25	20	100	50	20	50	50	50	50
54S/74S00	LO	20	12.5	10	111.11	50	10	40	200	40	200
54AS/74AS00	HI	2	50	40	200	100	40	100	100	100	100
54AS/74AS00	LO	20	12.5	10	111.11	50	10	40	200	40	200
54ALS/74ALS00A	HI	0.4	10	8	40	20	8	20	20	20	20
54ALS00A	LO	4	2.5	2	22.22	10	2	8	40	8	40
74ALS00A	LO	8	5	4	44.44	20	4	16	80	16	80
54AS1000	HI	40	1000	800	4000	2000	800	2000	2000	2000	2000
54AS1000	LO	40	25	20	222.22	100	20	80	400	80	400
74AS1000	HI	48	1200	960	4800	2400	960	2400	2400	2400	2400
74AS1000	LO	48	30	24	266.67	120	24	96	480	96	480
54ALS1000A	HI	1	25	20	100	50	20	50	50	50	50
54ALS1000A	LO	12	7.5	6	66.67	30	6	24	120	24	120
74ALS1000A	HI	2	65	52	260	130	52	130	130	130	130
74ALS1000A	LO	24	15	12	133.33	60	12	48	240	48	240

*Input Current HI
†Input Curent LO

Appendix B

Letter Symbols, Terms, and Definitions

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronics Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use. The definitions are grouped into sections applying to voltages, currents, switching characteristics, and classification of circuit complexity.

VOLTAGES

V_{IH} High-level input voltage
An input voltage level within the more positive (less negative) of the two ranges of values used to represent the binary variables. A minimum value is specified which is the least-positive (most-negative) value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL} Low-level input voltage
An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables. A maximum value is specified which is the most-positive (least-negative) value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{T+} Positive-going threshold voltage
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

V_{T-} Negative-going threshold voltage
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

V_{OH} High-level output voltage
The voltage at an output terminal for a specified output current I_{OH} with input conditions applied that according to the product specification will establish a high level at the output.

V_{OL} Low-level output voltage
The voltage at an output terminal for a specified output current I_{OL} with input conditions applied that according to the product specification will establish a low level at the output.

$V_{O(on)}$ On-state output voltage
The voltage at an output terminal for a specified output current with input conditions applied that according to the product specification will cause the output switching element to be in the on state.

Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

$V_{O(off)}$ Off-state output voltage
The voltage at an output terminal for a specified output current with input conditions applied that according to the specification will cause the output switching element to be in the off state.

Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

CURRENT

I_{IH} High-level input current
The current flowing into* an input when a specified high-level voltage is applied to that input.

I_{IL} Low-level input current
The current flowing into* an input when a specified low-level voltage is applied to that input.

*Current flowing out of a terminal is a negative value.

I_{OH} **High-level output current**
The current flowing into* the output with a specified high-level output voltage V_{OH} applied.

Note: This parameter is usually specified for open-collector outputs intended to drive other logic circuits.

$I_{O(off)}$ **Off-state output current**
The current flowing into* an output with a specified output voltage applied and input conditions applied that according to the product specification will cause the output switching element to be in the off state.

Note: This parameter is usually specified for open-collector outputs intended to drive devices other than logic circuits or for three-state outputs.

I_{OS} **Short-circuit output current**
The current flowing into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

I_{CCH} **Supply current, output(s) high**
The current flowing into* the V_{CC} supply terminal of a circuit when the reference output(s) is (are) at a high-level voltage.

I_{CCL} **Supply current, output(s) low**
The current flowing into* the V_{CC} supply terminal of a circuit when the reference output(s) is (are) at a low-level voltage.

DYNAMIC CHARACTERISTICS

f_{max} **Maximum clock frequency**
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause a change of output state with each clock pulse.

t_{HZ} **Output disable time (of a three-state output) from high level**
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

t_{LZ} **Output disable time (of a three-state output) from low level**
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

t_{PLH} **Propagation delay time, low-to-high-level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

t_{PHL} **Propagation delay time, high-to-low-level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{TLH} **Transition time, low-to-high-level output**
The time between a specified low-level voltage and a specified high-level voltage on a waveform that is changing from the defined low level to the defined high level.

t_{THL} **Transition time, high-to-low-level output**
The time between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from the defined high level to the defined low level.

t_w **Average pulse width**
The time between 50% amplitude points (or other specified reference points) on the leading and trailing edges of a pulse.

*Current flowing out of a terminal is a negative value.

t_h **Hold time**
The time interval for which a signal or pulse is retained at a specified input terminal after an active transition occurs at another specified input terminal.

$t_{release}$ **Release time**
The time interval between the release from a specified input terminal of data intended to be recognized and the occurrence of an active transition at another specified input terminal.

Note: When specified, the interval designated "release time" falls within the setup interval and constitutes, in effect, a negative hold time.

t_{su} **Setup time**
The time interval for which a signal is applied and maintained at a specified input terminal before an active transition occurs at another specified input terminal.

t_{ZH} **Output enable time (of a three-state output) to high level**
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.

t_{ZL} **Output enable time (of a three-state output) to low level**
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.

CLASSIFICATION OF CIRCUIT COMPLEXITY

Gate equivalent circuit
A basic unit-of-measure of relative digital-circuit complexity. The number of gate equivalent circuits is that number of individual logic gates that would have to be interconnected to perform the same function.

LSI **Large-scale integration**
A concept whereby a complete major subsystem or system function is fabricated as a single microcircuit. In this context a major subsystem or system, whether logical or linear, is considered to be one that contains 100 or more equivalent gates or circuitry of similar complexity.

MSI **Medium-scale integration**
A concept whereby a complete subsystem or system function is fabricated as a single microcircuit. The subsystem or system is smaller than for LSI, but whether digital or linear, is considered to be one that contains 12 or more equivalent gates or circuitry of similar complexity.

SSI **Small-scale integration**
Integrated circuits of less complexity than medium-scale integration (MSI).

*Current flowing out of a terminal is a negative value.

The TTL Data Book
Volume 2

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The Advanced Schottky Family of Bus Transceivers

W. T. Greer, Jr. and Rich Moore

6

TEXAS INSTRUMENTS

Contents

List of Illustrations

The Advanced Schottky Family of Bus Transceivers

INTRODUCTION

The Advanced Schottky family offers the system designer many high-performance digital logic solutions to achieve optimum system bus interfacing. This application report will assist designers of high-performance digital logic systems with the different applications of the Advanced Schottky family of bus transceivers. Texas Instruments offers these products in various functional, speed, power, and drive options which this report will highlight. Also, this report will extend data book explanations of the product characteristics and circuitry used to achieve these characteristics.

HISTORY

The industry's first octal bus transceiver, the 'LS245, was introduced by Texas Instruments in 1977. Since that time the popularity of the product has driven other technologies to incorporate the pinout and functionality of the original '245, and led to the current development of a new family of Advanced Low-Power Schottky (ALS) and Advanced Schottky (AS) family of bus transceivers. These transceivers are used to transfer information, typically on a bus configured architecture, from a source to one or more designated destinations. Therefore, to better understand the operation of the '245 and other bus transceivers, there is a need to understand the basic structure of a bus transceiver and its role in the system. Figure 1 shows the three external interfaces of a bus transceiver: data bus A, data bus B, and the control bus. The internal block is a common data input/output path usually containing a simple true or inverted logic configuration with associated control logic. This very simple logic has evolved into a family of products that interface the boundary between many different devices in the execution of the address, data, and control functions in a system.

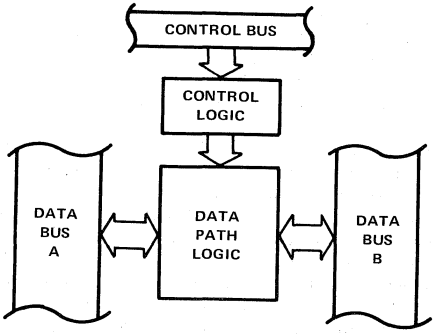
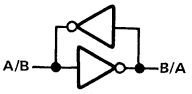


Figure 1. Bus Transceiver Architecture

ALS/AS BUS TRANSCEIVER FAMILY

The Advance Schottky family of bus transceivers has evolved from the original 'LS245 architecture. The bus interface options available to implement system needs requires an understanding of these architectures. To simplify this, separate the structure of bus transceivers into data I/O and control logic. The data I/O logic usually contains simple true or inverted logic. Figure 2 has the logic diagram, function table, and the Boolean function for both the inverter and noninverter (true) function. Two output options have been included in the family, three-state, and open collector.

LOGIC DIAGRAM FOR INVERTER

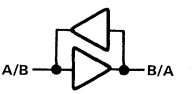


FUNCTION TABLE

INPUT	OUTPUT
A/B	B/A
H	L
L	H

$A/B = \overline{B/A}$

LOGIC DIAGRAM FOR NONINVERTER



FUNCTION TABLE

INPUT	OUTPUT
A/B	B/A
L	L
H	H

A/B = B/A

Figure 2. Inverter and Noninverter Logic

The three-state outputs allow the user to directly connect the outputs of the bus transceiver with a system bus that has other devices connected in parallel. To isolate all but one device on the system bus, the unwanted devices need to represent an open circuit or high impedance to the bus. The three-state output option is available with different control logic configurations.

Another popular technique used to isolate different bus transceiver outputs is the open-collector. Figure 3 shows a simplified logic diagram of an open-collector output circuit. When the input on the base of the transistor causes current to flow, the open-collector output transistor saturates and pulls the output voltage to ground or logic level 0. If no base current flows, the output transistor acts like an open circuit (logic level 1). A resistor is required from V_{CC} to the output of the transceiver to provide the required logic level 1. With this principle in mind, simple true or invert open-collector logic gates can be configured into bus transceivers. Figure 4 shows the four different logic configurations that are implemented with the Advanced Schottky family of bus transceivers.

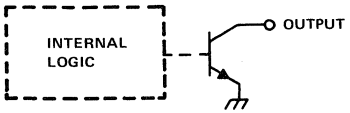
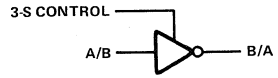
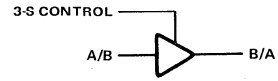


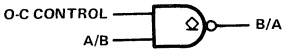
Figure 3. Open Collector Output Circuit



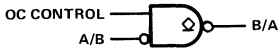
(a) INVERT LOGIC WITH 3-STATE OUTPUT



(b) NONINVERT LOGIC WITH 3-STATE OUTPUT



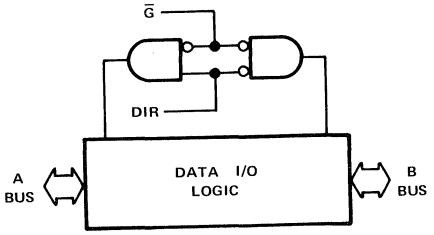
(c) INVERT LOGIC WITH OPEN-COLLECTOR OUTPUT



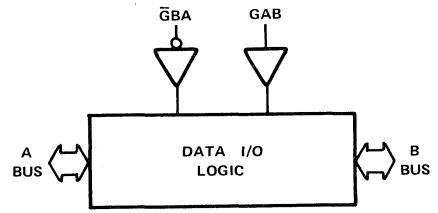
(d) NONINVERT LOGIC WITH OPEN-COLLECTOR OUTPUT

Figure 4. Bus Transceiver Logic Configuration

The control logic used with the bus transceivers provides for direction and output control. The two different control logic configurations are shown in Figure 5. The first control configuration allows the data I/O logic to transmit data from the A bus to the B bus or from the B bus to the A bus depending on the the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so the buses are effectively isolated. The second control configuration uses two enable inputs ($\overline{G}$BA and GAB) to control data transmission from the A bus to the B bus or from the B bus to the A bus. The enable inputs can be used



(a) SINGLE ENABLE



(b) DUAL ENABLE

Figure 5. Control Logic Configurations

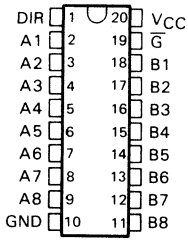
to disable the device so the bus is effectively isolated from the device. The dual enable configuration also gives the bus transceivers the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at a high impedance, both sets of bus lines (16 in all) will remain at their last state.

Figures 6 through 9 highlight by device type the pinout (a), function table (b), output option (c), logic diagram (d), and logic symbol (e) of many of the popular ALS/AS bus transceivers offered.

BUS TRANSCEIVERS WITH SERIES DAMPING RESISTORS

Along with the bus transceivers described above, TI also offers a group of bus transceivers with series damping resistors on the outputs. Figure 10 shows the equivalent output of this family. These octal bus transceivers are designed to drive the inputs of MOS devices in a typical dynamic RAM environment. The outputs are designed to mimimize overshoots on the low-to-high transitions and undershoots on the high-to-low transitions which may cause a false read at the inputs of DRAMs. This group of transceivers are designated as a 26XX series where the 6XX relates to the functional device in the above family descriptions. Currently, 'AS2620, 'AS2623, 'AS2640,and 'AS2645, are available. Figure 11 shows the output response of the'AS640 versus the 'AS2640. When a significant inductance is combined with a large capacitance, the series

TOP VIEW



(a) PINOUT

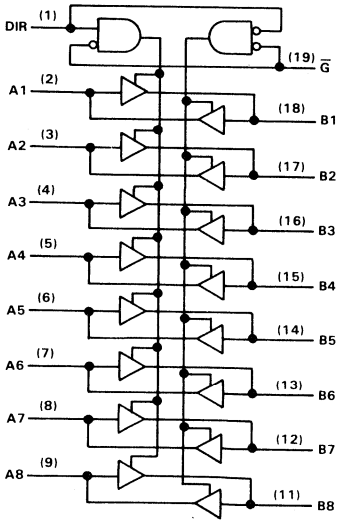
ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

(b) FUNCTION TABLE

DEVICE	OUTPUT	LOGIC
'ALS245A, 'AS245	3-State	True

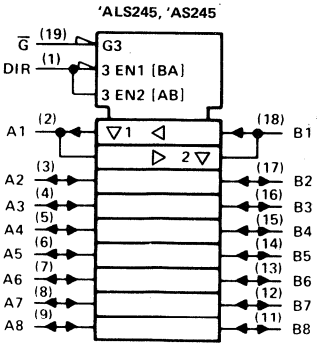
(C) OUTPUT OPTIONS

'ALS245, 'AS245



(d) LOGIC DIAGRAM (POSITIVE LOGIC)

'ALS245, 'AS245

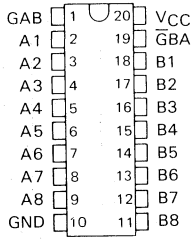


(e) LOGIC SYMBOL

Pin numbers shown are for J and N packages.

Figure 6. 'ALS245A and 'AS245 Octal Bus Transceivers with Three-State Outputs (True)

TOP VIEW



(a) PINOUT

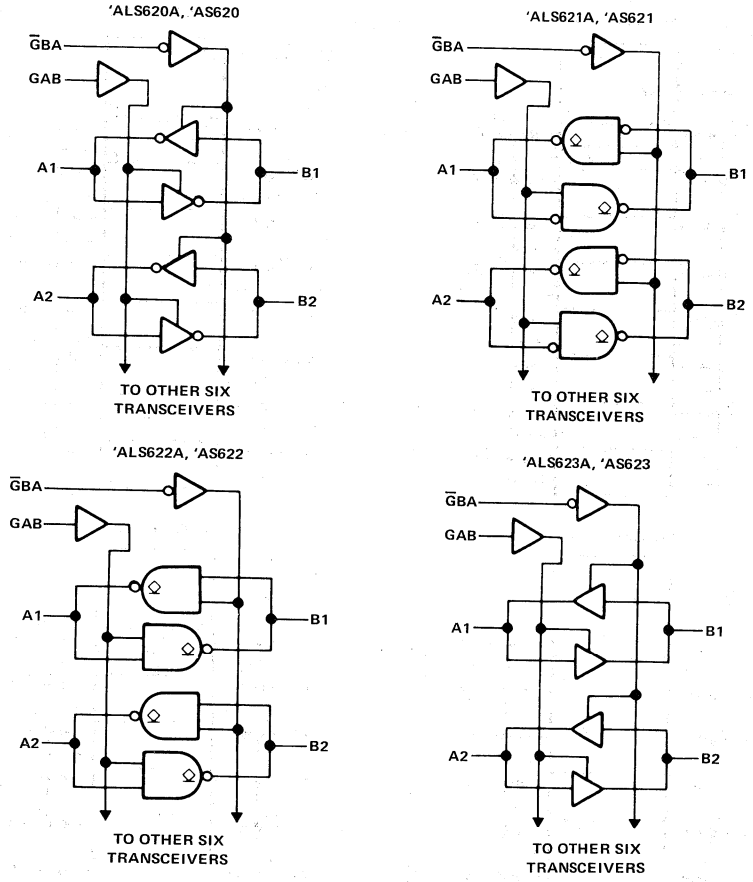
ENABLE INPUTS		OPERATION	
$\overline{G}BA$	GAB	'ALS620A, 'ALS622A 'AS620, 'AS622	'ALS621A, 'ALS623A 'AS621, 'AS623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Isolation	Isolation
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus	B data to A bus, A data to B bus

(b) FUNCTION TABLE

DEVICE	OUTPUT	LOGIC
'ALS620A, 'AS620	3-State	Inverting
'ALS621A, 'AS621	Open-Collector	True
'ALS622A, 'AS622	Open-Collector	Inverting
'ALS623A, 'AS623	3-State	True

(c) OUTPUT OPTIONS

Figure 7. 'ALS620A, 'AS620 thru 'ALS623A, 'AS623 Octal Bus Tranceivers with Three-State or Open-Collector Outputs (True or Inverting)

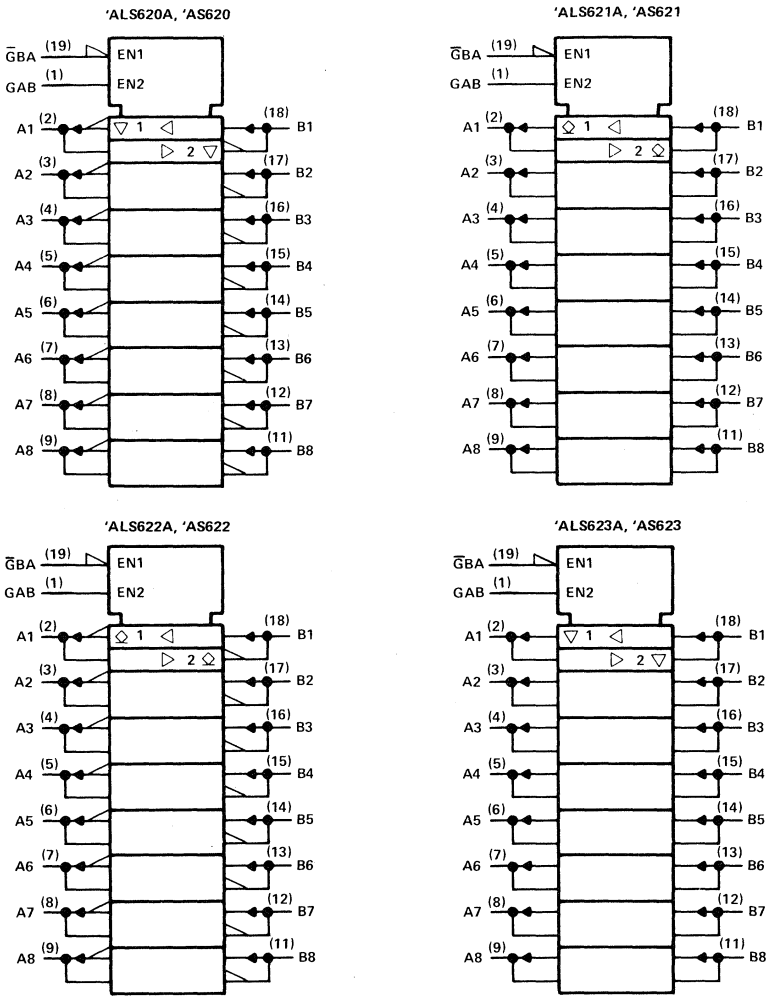


Pin numbers shown are for J and N packages.

(d) LOGIC DIAGRAMS (POSITIVE LOGIC)

Figure 7. 'ALS620A, 'AS620 thru 'ALS623A, 'AS623 Octal Bus Tranceivers with Three-State or Open-Collector Outputs (True or Inverting) (Continued)

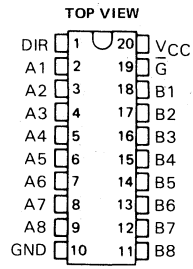
6



Pin numbers shown are for J and N packages.

(e) LOGIC SYMBOLS

Figure 7. 'ALS620A, 'AS620 thru 'ALS623A, 'AS623 Octal Bus Tranceivers with Three-State or Open-Collector Outputs (True or Inverting) (Concluded)



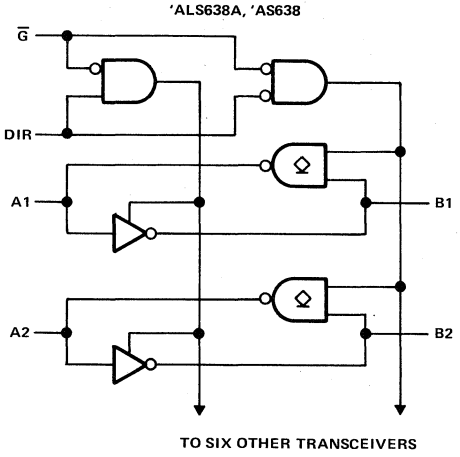
(a) PINOUT

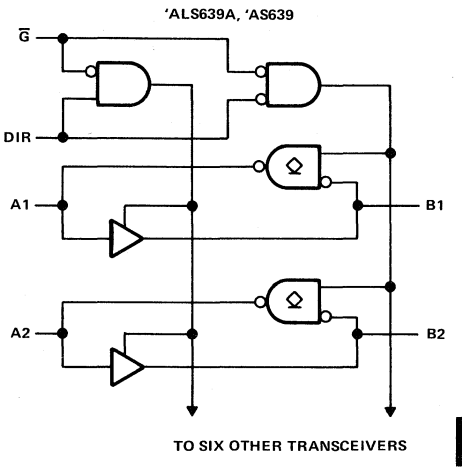
CONTROL INPUTS		OPERATION	
		'ALS638A 'AS638	'ALS639A 'AS639
$\overline{G}$	DIR		
L	L	$\overline{B}$ data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus
H	X	Isolation	Isolation

(b) FUNCTION TABLE

DEVICE	A OUTPUT	B OUTPUT	LOGIC
'ALS638A, 'AS638	Open-Collector	3-State	Inverting
'ALS639A, 'AS639	Open-Collector	3-State	True

(c) OUTPUT OPTIONS



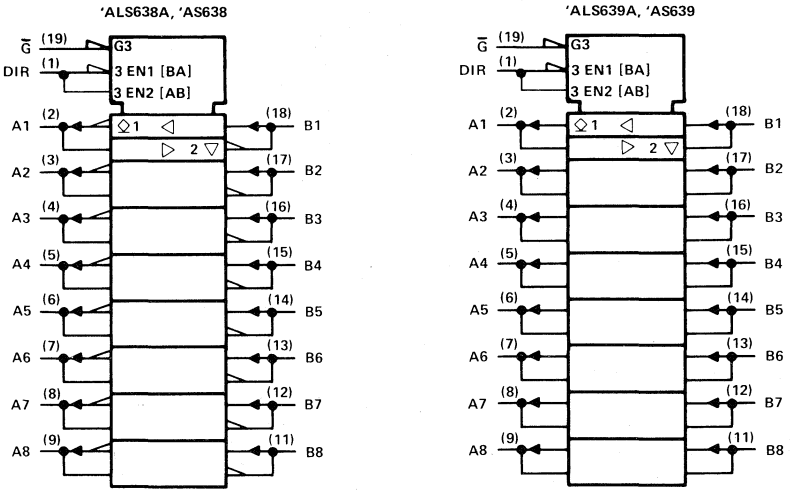


Pin numbers shown are for J and N packages.

(d) LOGIC DIAGRAMS (POSITIVE LOGIC)

Figure 8. 'ALS638A, 'AS638, 'ALS639A, and 'AS639 Octal Bus Transceiver with Three-State and Open-Collector Outputs (True or Inverting)

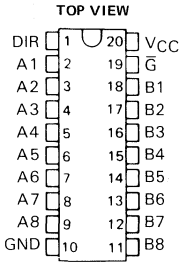
6



Pin numbers shown are for J and N packages.

(e) LOGIC SYMBOLS

Figure 8. 'ALS638A, 'AS638, 'ALS639A, and 'AS639 Octal Bus Transceiver with Three-State and Open-Collector Outputs (True or Inverting) (Concluded)



(a) PINOUT

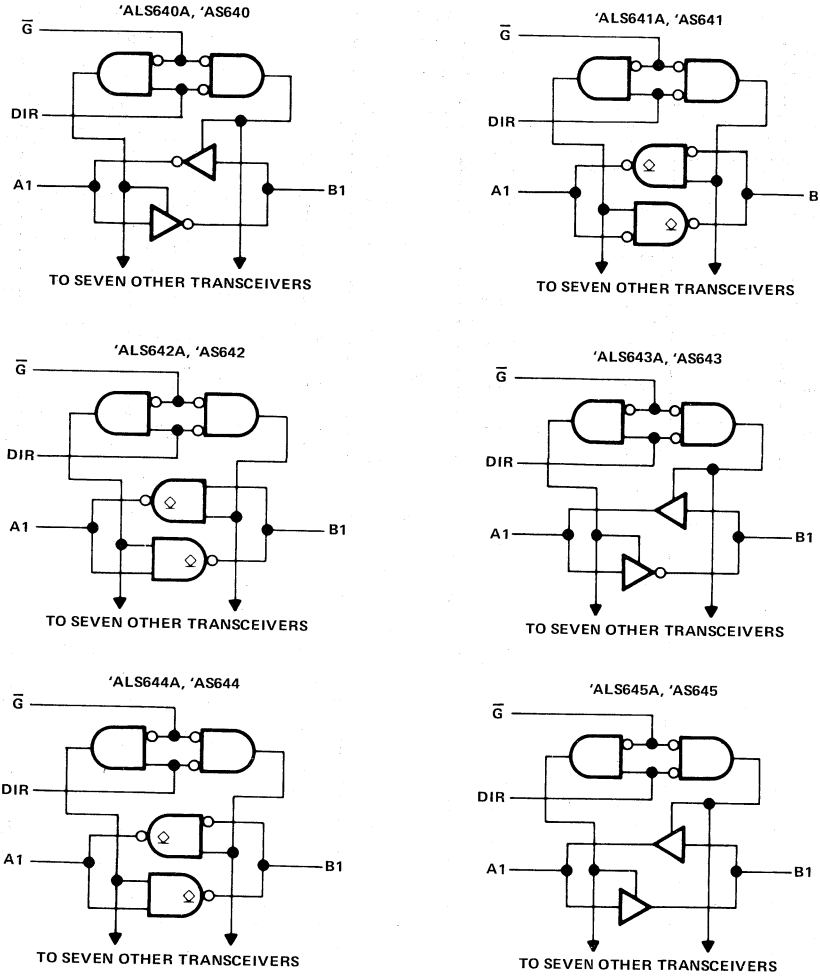
CONTROL INPUTS		OPERATION		
$\overline{G}$	DIR	'ALS640A, 'AS640 'ALS642A, 'AS642	'ALS641A, 'AS641 'ALS645A, 'AS645	'ALS643A, 'AS643 'ALS644A, 'AS644
L	L	$\overline{B}$ data to A bus	B data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus	$\overline{A}$ data to B bus
H	X	Isolation	Isolation	Isolation

(b) FUNCTION TABLE

DEVICE	OUTPUT	LOGIC
'ALS640A, 'AS640	3-State	Inverting
'ALS641A, 'AS641	Open-Collector	True
'ALS642A, 'AS642	Open-Collector	Inverting
'ALS643A, 'AS643	3-State	True and Inverting
'ALS644A, 'AS644	Open-Collector	True and Inverting
'ALS645A, 'AS645	3-State	True

(c) OUTPUT OPTIONS

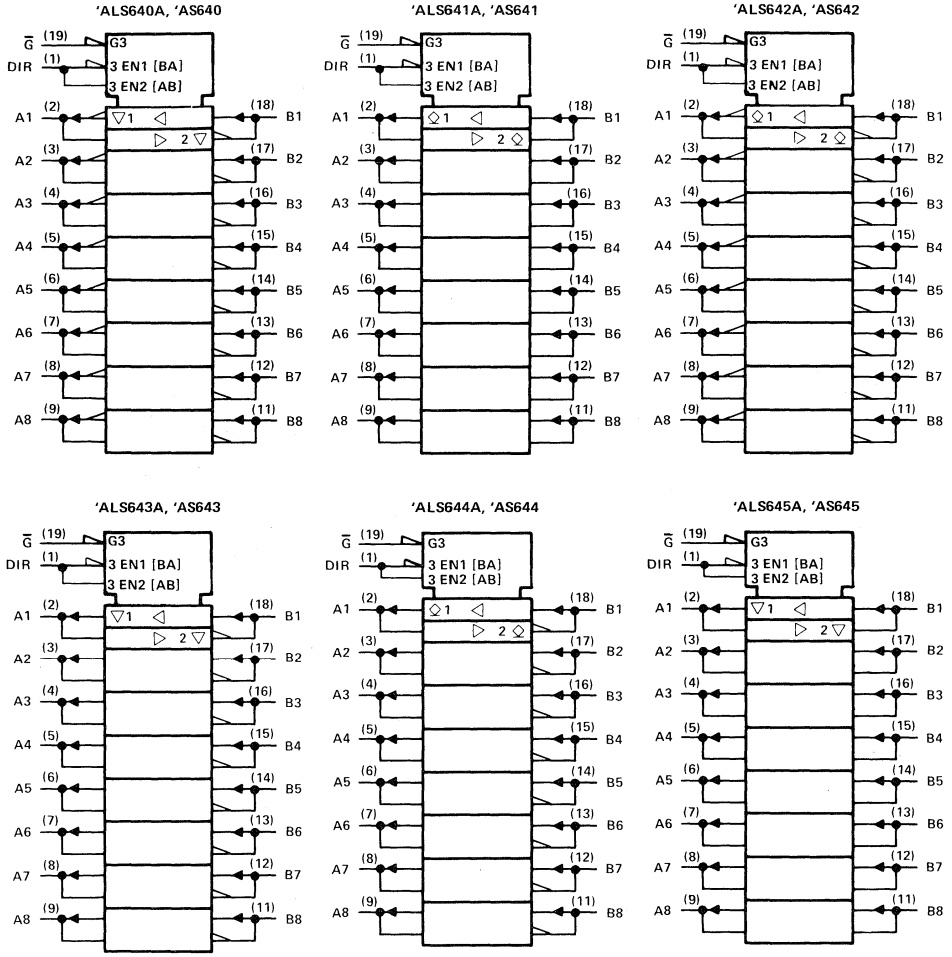
Figure 9. 'ALS640A, 'AS640 thru 'ALS645A, 'AS645 Octal Bus Transceivers with Three-State or Open-Collector Outputs (True and/or Inverting)



Pin numbers shown are for J and N packages.

(d) LOGIC DIAGRAMS (POSITIVE LOGIC)

Figure 9. 'ALS640A, 'AS640 thru 'ALS645A, 'AS645 Octal Bus Transceivers with Three-State or Open-Collector Outputs (True and/or Inverting) (Continued)



Pin numbers shown are for J and N packages.

(e) LOGIC SYMBOLS

Figure 9. 'ALS640A, 'AS640 thru 'ALS645A, 'AS645 Octal Bus Transceivers with Three-State or Open-Collector Outputs (True and/or Inverting) (Concluded)

damping resistors reduced the undershoot by 58%. These devices are also useful when driving long lines (when the rise/fall times are faster than the delay associated with the line being driven).

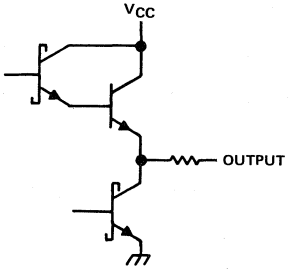


Figure 10. 'AS26XX Series Output Configuration

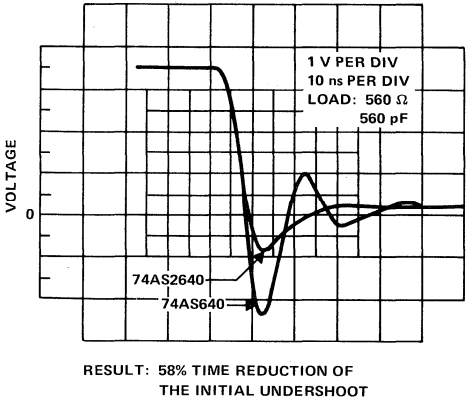


Figure 11. Effectiveness of Series Damping Resistors

IMPROVED ELECTRICAL CHARACTERISTICS

The 'ALS/'AS6XX family of bus transceivers includes many of the advancements designed into the TI Advanced Schottky family of ALS/AS that not only contribute to improved performance, but help overcome many system problems that have nagged designers for years. The inputs are P-N-P transistors to help reduce dc loading. Input thresholds have been raised on most devices to 1.4 V, typically. Output transistors have been designed to handle heavily capacitive bus loads. The minimum source current specification for the 'ALS/'AS6XX series three-state outputs is -15 mA for I_{OH} The minimum sink current for 'ALS6XX series is 24 mA, with a dash one (-1) series that offers 48 mA. The 'AS6XX series has a minimum I_{OL} specification of 64 mA.

All family members have improved input and output clamps, which include protection from electrostatic discharge (ESD) up to 2000 V when applied according to MIL-STD-883, Method 3015. Grounded guard rings are also included on all input and output transistors to block potential substrate leakage paths and eliminate system latch-up problems.

Other new circuit features include "Miller-Killer" circuitry for both ac and dc conditions. Figure 12 shows both the standard pull-down circuit and the ac Miller-Killer circuit used on ALS/AS circuits. The ac Miller-Killer circuit turns off the sink transistor (Q4) in the output circuit much faster than the active pull-down circuit. This faster turnoff of the sink transistor (Q4) minimizes the amplitude and duration of the current spike caused by having the upper and lower output transistor on during the low-to-high transition.

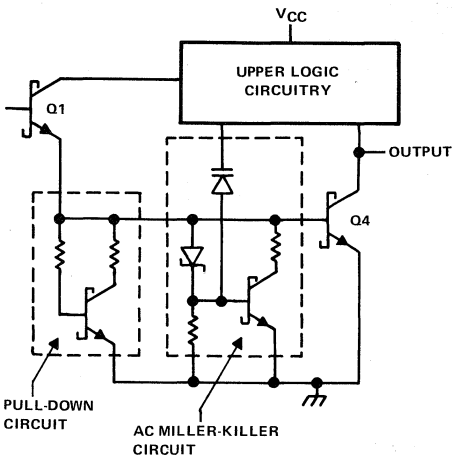


Figure 12. AC Miller-Killer Circuit

A dc Miller-Killer has also been incorporated on all ALS/AS bus transceivers to minimize the effect of the Miller capacitance in three-state devices on the system bus. Under dynamic conditions, a three-state device can load down a system bus with approximately 60 pF of capacitance per output due to leakage currents from the collector to base of the output sink transistor. This leakage current is multiplied by the h_{FE} of the transistor; hence Miller capacitance. The dc Miller-Killer circuitry is shown in Figure 13. The level shifter is connected to the circuit via the additional phase splitter, Q2. When the base of the phase splitter is pulled low, Q2's collector voltage rises. This voltage is applied through the level shifter to Q3's base. Both the input stage and the three-state control connect to the the base of Q2, thus the Miller-Killer is activated and shorts the leakage current on the sink transistor. The three-state loading is less than 10 pF per output, which greatly reduces the ac loading on the system bus.

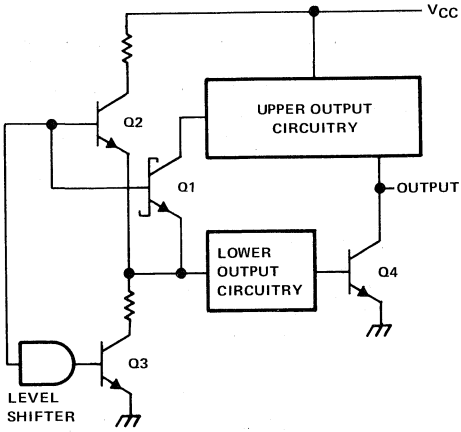
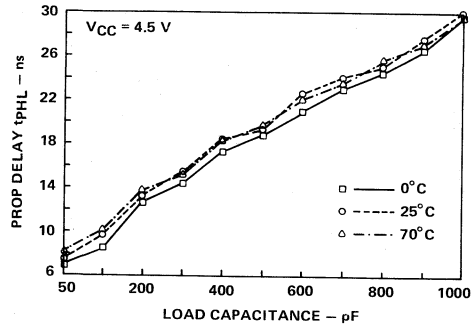


Figure 13. DC Miller-Killer Circuit

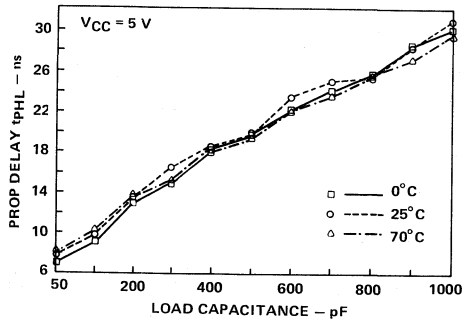
SPECIFICATIONS

The Advanced Schottky family is designed to operate over both the full military temperature range of −55 °C to + 125 °C and the commercial range of 0 °C to 70 °C. The power supply ranges are based on the more demanding 5 V ±10% range. Parametric limits are specified over the full V_{CC} variations, with ac loads of 50 pF versus 15 pF in previous TTL logic families. In addition all ac specifications now have a minimum performance limit to decrease system timing problems. Also, all ac values are now guaranteed over the full temperature range.

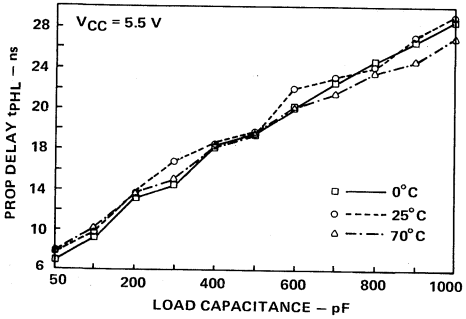
Included in this publication are propagation delay versus load capacitance curves (Figure 14 through 19) to assist the designer in calculating typical performance of the bus transceiver family beyond our guaranteed specification range. These curves present propagation delay at 0 °C, 25 °C, and 70 °C for V_{CC} of 4.5 V, 5 V, and 5.5 V with loads from 50 pF to 1000 pF. Performance at lower capacitance loads can be determined by calculating the slope of the line and extrapolating the propagation delay line with this calculated slope.



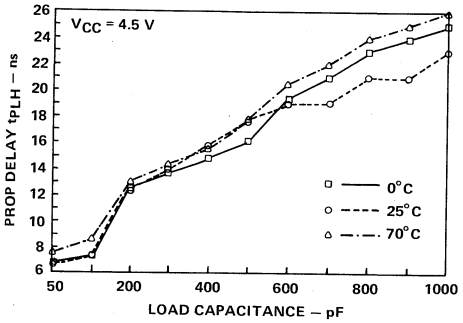
(a)



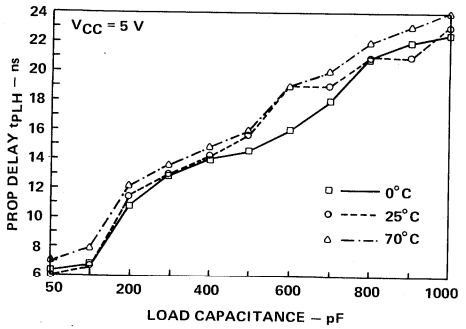
(b)



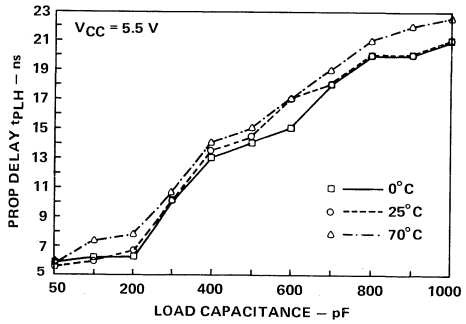
(c)



(d)

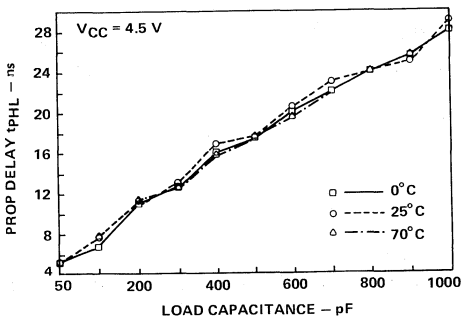


(e)

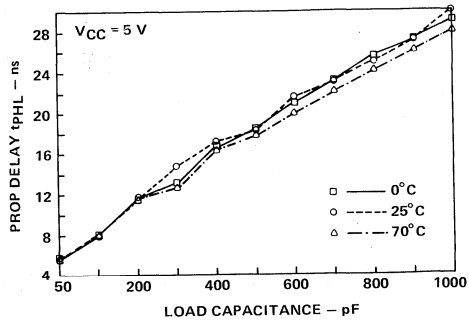


(f)

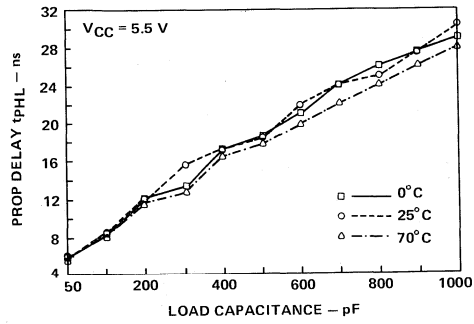
Figure 14. SN74ALS245A Propagation Delay vs Capacitance



(a)



(b)



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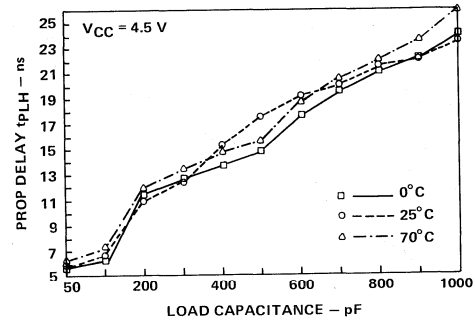

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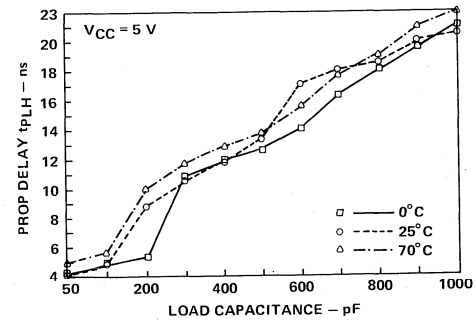
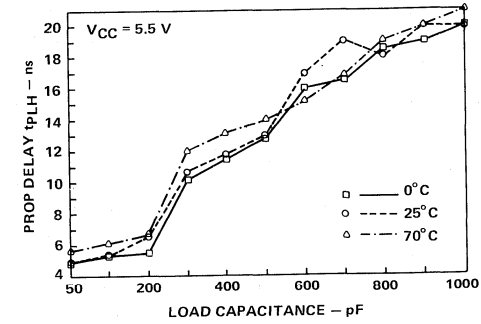
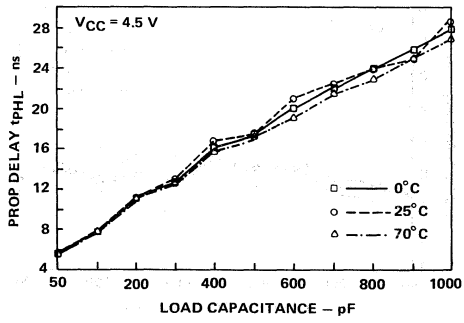


(e)

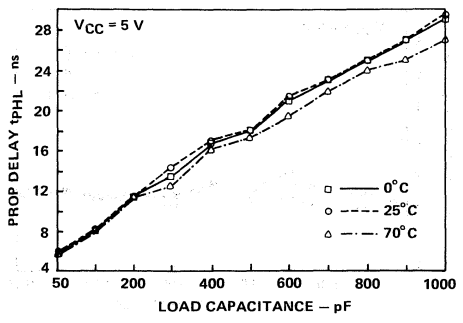


(f)

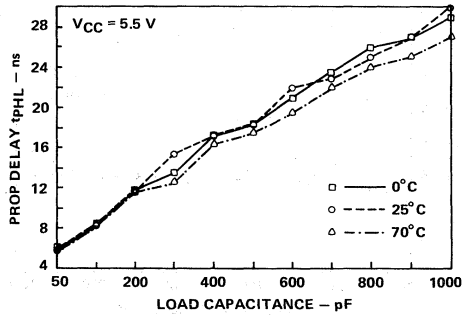
Figure 15. SN74ALS620A Series Propagation Delay vs Capacitance



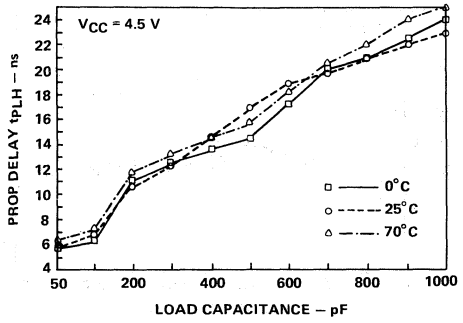
(a)



(b)



(c)



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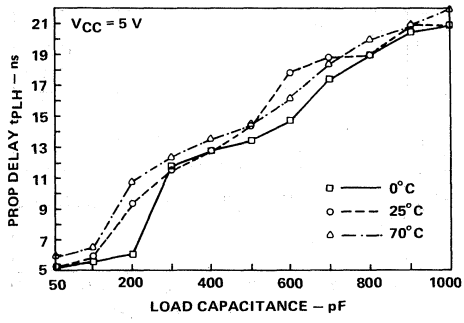
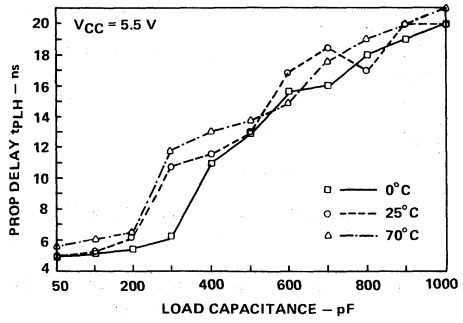


(e)



(f)

Figure 16. SN74ALS640A Series Propagation Delay vs Capacitance

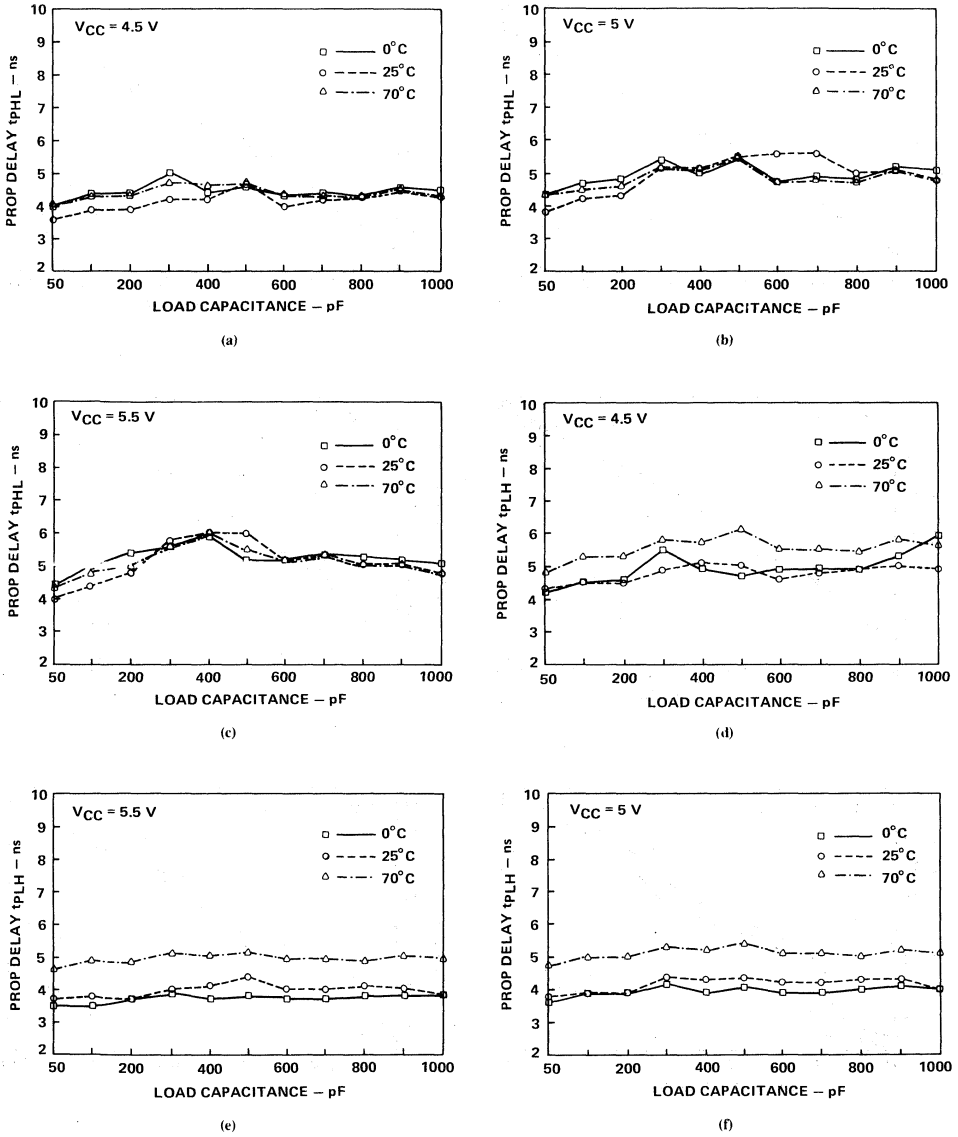
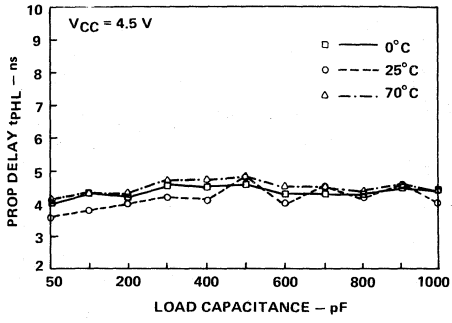
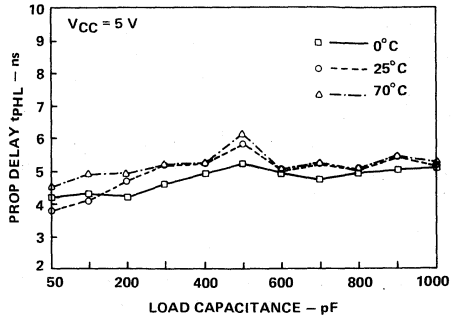


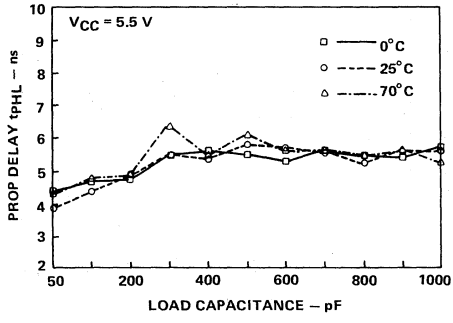
Figure 17. SN74AS620 Series Propagation Delay vs Capacitance



(a)



(b)



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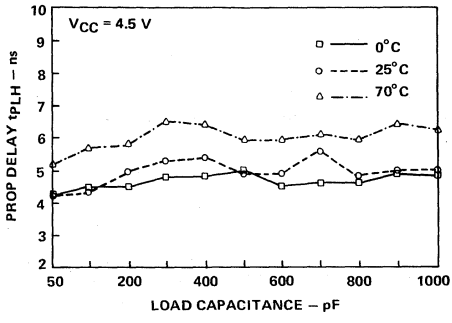

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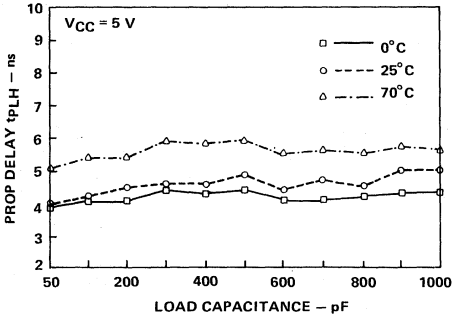

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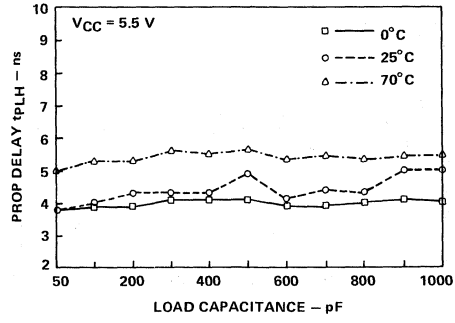

(f)

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Figure 18. SN74AS640 Series Propagation Delay vs Capacitance

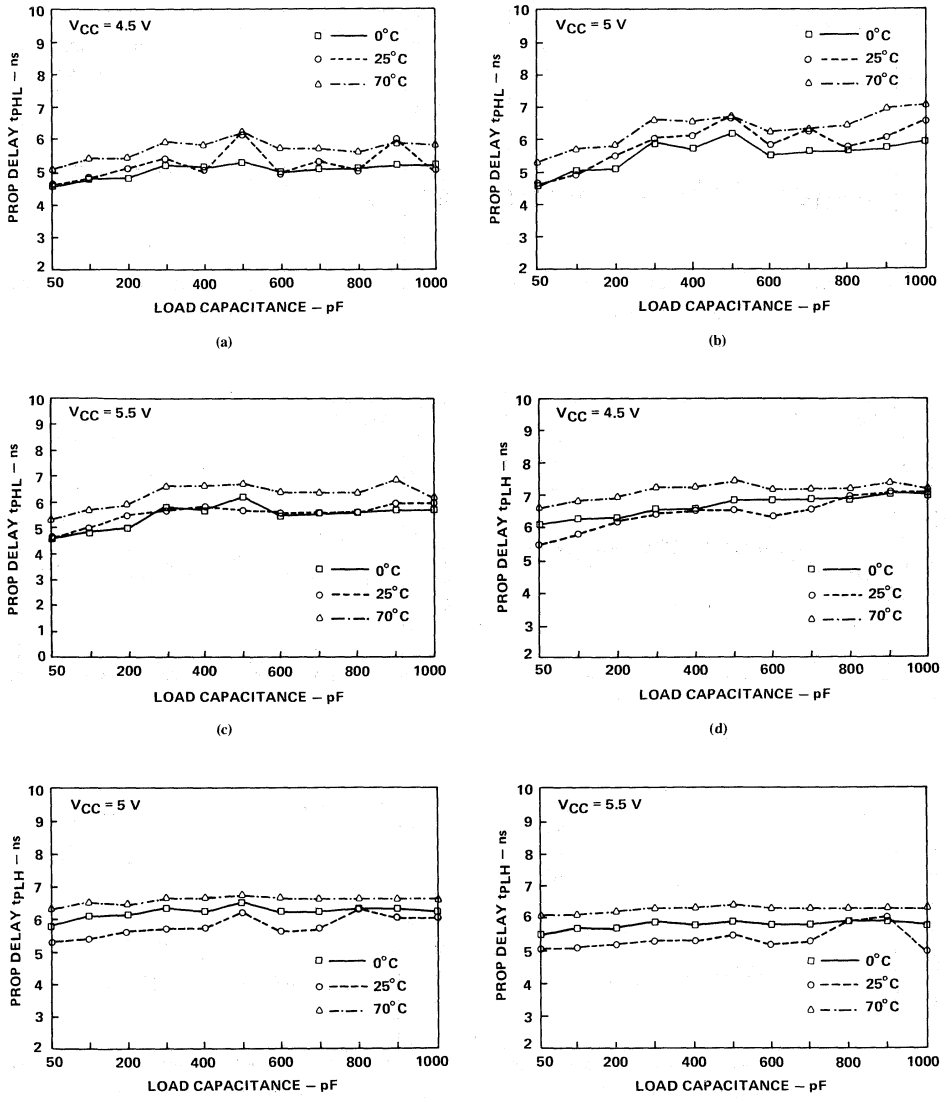

Figure 19. SN74AS645 Propagation Delay vs Capacitance

CONCLUSION

The Advanced Schottky family of bus transceivers are an integral part of a rapidly growing family of high-performance products. This family includes Advanced Low-Power Schottky (ALS) and Advanced Schottky (AS) TTL, programmable logic arrays, FPLAs, PROMs, 8-Bit Slice, and other LSI/VLSI products. Texas Instruments is providing the solutions to meet your new design challenges.

APPENDIX

'245/'645 BUS TRANSCEIVER COMPARISON

The SN74ALS/AS645 is functionally and schematically the same as the SN74ALS/'AS245, respectively. In other words, the 'ALS245 and 'ALS645 are fabricated from the same die. The 'XX645 device number came about because the 'LS245 was redesigned to improve its output characteristic. The redesigned function was so different in character, that a new number was given the device to totally eliminate application confusion. The 'LS645 was designed to improve the dynamic output capacitance of the transceiver function. This was done by changing the output circuitry. A passive pull-down (resistor) was used in the output stage of the 'LS645, whereas the classical transistor/resistor active pull-down arrangement was used in the 'LS245 circuit design. This active pull-down arrangement tends to have a higher output capacitance (Miller effect) than the passive pull-down output stage. In the ALS/AS family a totally different circuit is being used which reduces this output capacitance to typically 10 pF per output. Additional information concerning this reduction in capacitance is provided in this application report.

The TTL Data Book
Volume 2

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Metastable Characteristics of Texas Instruments Advanced Bipolar Logic Families

Robert K. Breuninger and Kevin Frank

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TEXAS INSTRUMENTS

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List of Illustrations

INTRODUCTION

At some point in every system designers career, they are faced with the problem of synchronizing two digital signals operating at two different frequencies. This problem is typically solved by synchronizing one of the signals, to the local clock, through a flip-flop. However, this solution presents an awkward dilemma, the setup and hold time specifications associated with the flip-flop are sure to be violated. The metastable characteristics of the flip-flop used can influence overall system reliability. The purpose of this application report is to give the system designer a better understanding of the metastable characteristics pertaining to Texas Instruments Advanced Schottky Bipolar Logic Family.

METASTABLE DEFINITION

Whenever a flip-flops setup and hold time is violated, the flip-flops output response is uncertain. Presently, there is no circuit that can 100% guarantee its response. This is why the device manufacturer does not guarantee its operation. Specifically, the metastable state is defined as that time period when the output of a digital logic device, is not at a logic level 1 (V_{out} less than 2 V) or a logic level 0 (V_{out} greater than 0.8 V), but instead between 0.8 V and 2 V. Since the input data is changing at the time of being clocked, the system designer does not care if the flip-flop goes to either a high or low logic level, just so long as the output does not hang up in the metastable region. The metastable characteristics for a particular flip-flop will determine how long the device stays in the metastable region. This concept is illustrated in the timing diagram of Figure 1.

METASTABLE EVALUATION

Anyone who has tried to evaluate the metastable characteristics for a particular flip-flop, has probably found it is not an easy task. The number of times the output hangs up in the metastable region is extremely small when compared to total number of clock transitions. In addition, the amount of time the output is actually in the metastable region is a variable and dependent on the type of flip-flop used (LS, ALS, AS, etc.).

From the design engineers viewpoint, when using a flip-flop as a data synchronizer, they can no longer use the specified data sheet maximum for propagation delay. Instead, to guarantee reliable system operation, they need to know how long after the specified data sheet maximum they need to wait before using the data. Conventional test equipment is not designed to measure these parameters, so a special test circuit is required for characterizing MTBF (Mean Time Between Failures) and Δt (time between CLK and Q valid). With these two parameters specified, the system designer can make a rational decision about what type of flip-flop to use, and how long to wait before using the data.

Circuit Description

The circuit in Figure 2 can be used in evaluating MTBF and Δt for a selected flip-flop (DUT, Device Under Test). Two 'AS04s are used to detect whenever the Q output of the DUT is in the metastable region. This is accomplished by adjusting the input threshold to 2 V on one inverter and 0.8 V on the other. Notice that input thresholds are adjusted by referencing the ground input pins to 0.6 V and −0.6 V respectively. Therefore, whenever the Q output of the DUT

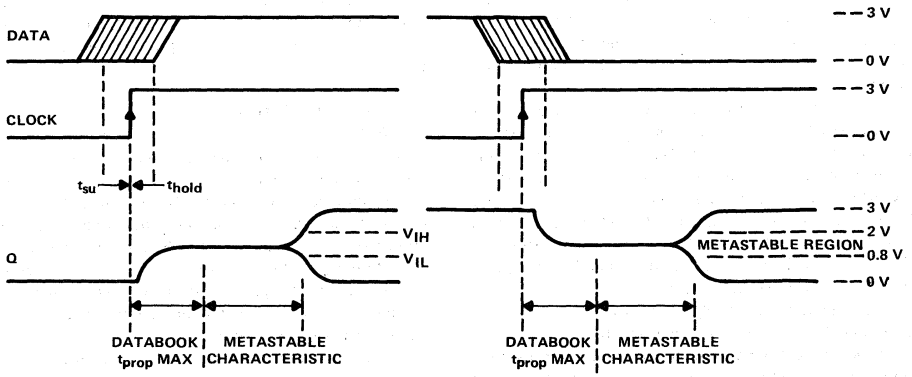

Figure 1. Metastable Timing Diagram

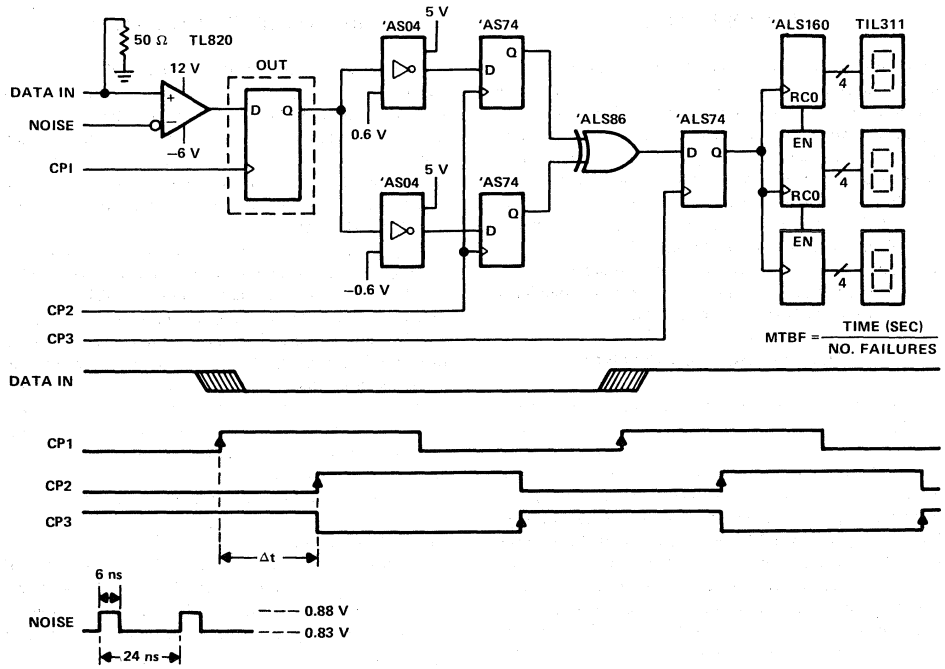

Figure 2. Metastable Evaluation Test Circuit

is between 0.8 V and 2 V, the inverters will be in opposite states. Whenever the Q output of the DUT is higher than 2 V or lower than 0.8 V, both inverters will be at the same logic level. The outputs of the 'AS04s are then clocked (CP2) into two 'AS74s a selected time (Δt) after the DUT clock (CP1). The outputs of the 'AS74s are compared through an 'ALS86 and clocked (CP3) into another 'ALS74. This guarantees against any false clocking by the evaluation circuit. The output of the 'ALS74 is then feed to a series of three 'ALS160 counters, and on into three TIL311s for counter display.

In order to maximize the possibility of forcing the DUT into a metastable state, the input data signal must jitter around the threshold of the input clock. The width of the jitter should equal, or exceed the setup and hold time specification for the device. In our evaluation circuit, this is accomplished by feeding a low level noise signal into the negative input of a TIL820 operational amplifier. The pictures shown in Figure 3 show the noise generated around the DUT clock (CP1) for both input data transitions.

It should be intuitively obvious that the worst-case condition, for any specified input data frequency, will be when the input data **always violates the data setup and hold times**. This condition is shown in the timing diagram of Figure 2. Any other relationship of CP1 to DATA IN, would provide less chance for the device to enter the metastable state. Therefore, it can be concluded that the worst-case condition for a given input data frequency, will be 0.5 times the DUT clock rate where the input data always violates the setup and hold time.

By using the described circuit, MTBF can be determined for several different values of Δt. Plotting this information on semilog paper reveals the metastable characteristics, for the selected flip-flop, at the desired input data frequency.

Test Circuit Limitations

Before we proceed to the AS/ALS test results, it is important to analyze the limitations of our test circuit. In this way, we can better understand its effects on the test results. Two major areas which can greatly affect the test results are not centering the jitter around the input clock, and propagation delay of the 'AS04s. By not centering the jitter around the input clock, the risk of entering the metastable state is reduced. Proper care must be taken to ensure that the jitter is always centered around the input clock to guarantee worst-case conditions.

The propagation delay of the 'AS04s affect the test results because they add propagation delay between the output of the DUT, and the data being clocked into the 'AS74s. For

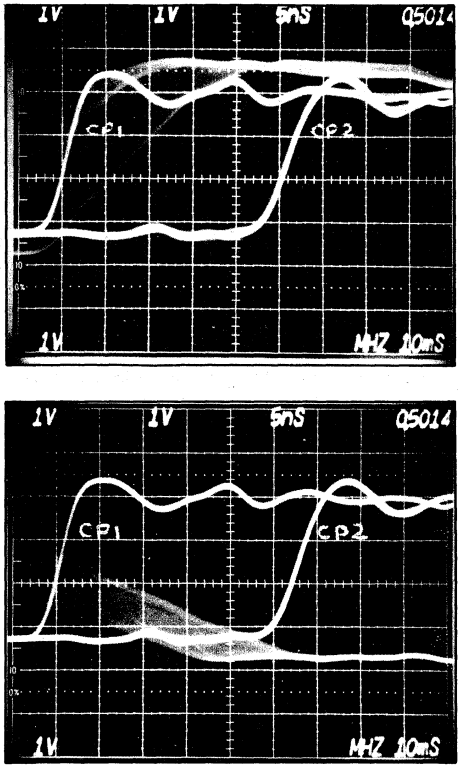

Figure 3. Test Waveforms

example, the output on the DUT may come out of the metastable region, but the 'AS04s may not switch before CP2 occurs. This causes an inappropriate reading. The typical propagation delay of the 'AS04s, **as configured in the test circuit**, is approximately 4 ns. This 4 ns delay should be considered when evaluating the test results. If inverters slower than the 'AS04s are used in the test circuit, a larger offset must be considered.

ALS/AS Test Results

Using the test circuit described in Figure 2, 'ALS74s, 'ALS273s and 'ALS374s were evaluated at several different Δt time periods. The input clock frequency used was 1 MHZ with an input data frequency of 500 kHz. The devices were allowed to run until an appropriate amount of errors were recorded. The number of errors were then divided by the total time the devices were allowed to run. This results in a MTBF for the selected Δt. The information was then recorded on semilog paper for analysis. It was found that all three device types exibited basically the same metastable characteristics within +3 ns of each other. This was expected since all three device types come from the same technology. The same experiment was performed using AS and LS devices. The average characteristics for all three device families are shown in Figure 4. The 4-ns offset generated by the test circuit has not been subtracted from the data.

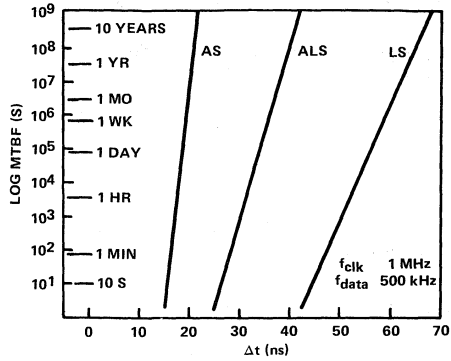

Figure 4. AS/ALS/LS Metastable Characteristics

Other Clock Frequencies

Clock frequencies other than 1 MHz will either increase or decrease the probability of the device entering the metastable state. The faster the frequency, the higher the probability of entering the metastable state. Likewise, the slower the frequency, the lower the probability of entering the metastable state. From the data taken in the above experiment, an equation can be derived for the metastable characteristics at other clock frequencies. Equation (1) relates input clock and data frequency, to metastable characteristics.

Metastable Equation

$$\frac{1}{\text{MTBF}} = f_{cp} \times f_{data} \times C1\, e^{(-C2\,\Delta t)} \qquad (1)$$

As stated earlier, the worst case situation for the test circuit shown in Figure 2, is when the data setup and hold time is always violated. Based on this assumption, the equation is reduced to the following.

$$\frac{1}{\text{MTBF}} = \frac{1}{2} f_{cp}^2 \times C1\, e^{(-C2\,\Delta t)} \qquad (2)$$

The constants C1 and C2 describe the metastable characteristics of the device. From the experimental data graphed in Figure 4, these constants can be solved for each device family. As an example, the constants are solved below for the ALS device family.

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C2 is defined by the slope of the line. Picking two data points off the graph yields the following.

$$C2 = \frac{\text{Log } 10^8 - \text{Log } 10^2}{40.2 - 28.2}(2.302) = \frac{6}{12}(2.302) = 1.151$$

By plugging C2 into equation 2, along with using one of the data points off the graph, C1 can be solved for.

$$\frac{1}{\text{MTBF}} = \frac{1}{2} f_{cp}^2 \times C1\, e^{(-1.151\,\Delta t)}$$

$$\frac{1}{10^8} = \frac{1}{2} (10^6)^2 \times C1\, e^{(-1.151 \times 40.2)}$$

$$C1 = 2.49$$

Inserting C1 and C2 into equation 2, yields the metastable equation for ALS.

$$\frac{1}{\text{MTBF}} = \frac{1}{2} f_{cp}^2 \times 2.49\, e^{(-1.151\,\Delta t)}$$

Given this worst-case equation, the system designer can determine the metastable characteristics for ALS when using other input clock frequencies.

The equations for AS and LS can be derived using the same procedure. They are as follows.

AS:

$$\frac{1}{\text{MTBF}} = \frac{1}{2} f_{cp}^2 \times 1.53 \times 10^7\, e^{(-2.92\,\Delta t)}$$

LS:

$$\frac{1}{\text{MTBF}} = \frac{1}{2} f_{cp}^2 \times 306\, e^{-0.783\,\Delta t)}$$

To get a feel for the effect of changing the input clock frequency, Figure 5 shows the change in the metastable characteristics from 1 MHz to 10 MHz.

METASTABLE CHARACTERISTICS OF PROGRAMMABLE LOGIC

The PAL16R4A and TIBPAL16R4-15 from the programmable logic family were also evaluated. They exhibited very similar characteristics to the ALS curve. This was expected because they utilize the same technology. One important consideration when evaluating programmable logic in the test circuit described, is positioning the jittery data a few nanoseconds before CP1. This compensates for the delay of the AND/OR array which is usually positioned in front of the flip-flop. Remember that the jittery data must be violating the setup and hold time at the input to the flip-flop, not just at the device input. Some experimentation is usually required to find the worst-case condition.

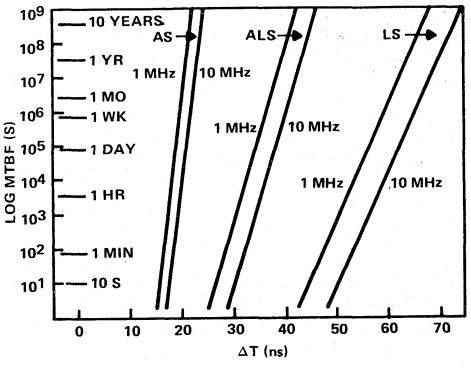

Figure 5. AS/ALS/LS Metastable Characteristics Variation with Frequency

As a general rule, a system designer can usually get a feel for the metastable characteristics of a device by simply looking at the setup and hold time specifications. Usually, the smaller the setup and hold time numbers, the better its metastable characteristics will be. However, in the case of programmable logic, the setup and hold time numbers are not reflective of metastable characteristics. This is because the setup and hold time numbers also reflect the propagation delay time of the AND/OR logic in front of the flip-flops.

SUMMARY

The metastable characteristics of a flip-flop used for data synchronization can greatly affect system reliability. Based on the information presented in this application report, the system designer can make a rational decision about what type of flip-flop to use, and what its metastable characteristics will be.

It is easy to see from the experimental data shown in Figure 4, that AS offers the best metastable characteristics. It has a much narrower setup and hold time window, and is quicker to recover once it gets into the metastable region. However, with adequate sampling time, ALS and LS will also perform well. The selection of what type of flip-flop to use must be based on the speed of the application. As a general rule, the faster the flip-flop, the better its metastable characteristics.

We at Texas Instruments believe that the graphs shown and equations derived, represent a reasonable assumption about the metastable characteristics for the device families discussed. However, we strongly recommend that when using flip-flops as data synchronizers, an adequate amount of guardband is allowed between the characteristics shown, and when the output of the flip-flop is actually sampled.

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Volume 2

Advanced Low-Power Schottky

Reliability Report

Quality & Reliability Assurance

PREFACE

Texas Instruments places major emphasis on the reliability of its semiconductor products beginning with design and continuing through wafer processing, assembly, test, and final packaging. This report provides the design engineer with an overview of the technology and reliability performance of Texas Instruments capabilities in the ALS family of plastic devices.

INTRODUCTION

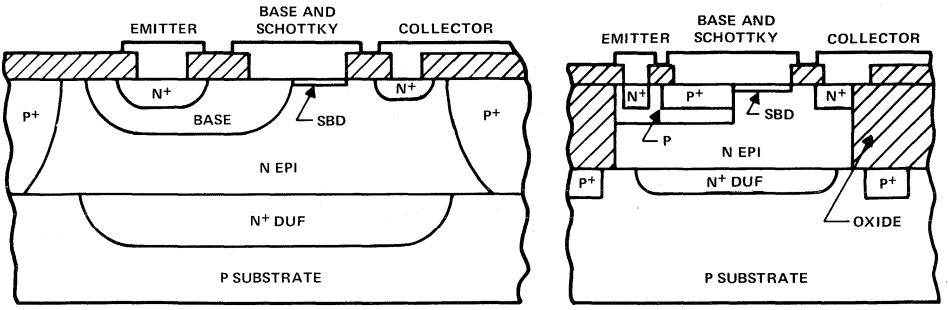
Series 54/74 transistor-transistor logic (TTL) has, since its introduction in 1965, become the most popular digital integrated circuit logic family ever offered and is probably the easiest to use medium-to-high performance logic available. Its popularity, coupled with high-volume production techniques, has vaulted TTL into a position where it is the most economical approach to the implementation of major portions of medium-to-high performance digital logic systems. Systems range from those making simple decisions to highly complex real time computer installations handling worldwide data processing.

The economic demands to constantly improve the efficiency of these systems are evident, and Series 54/74 is expanding rapidly to include the broadest selection of medium-scale integrated (MSI) and large-scale integrated (LSI) circuits of any logic family. In addition, the technology was, and still is, pursued vigorously to ensure that the TTL system designer has the needed performance at his disposal. With the invention of Schottky barrier diode clamping patented by Texas Instruments for TTL circuits, significant improvements in speed and performance were achieved. The announcement of Schottky (Series 54S/74S) catalog parts was made early in 1970.

Recent innovations in integrated circuit design have made it possible to go a step further, hence the development of the new "AS" (Advanced Schottky) and "ALS" (Advanced Low Power Schottky) families. AS provides considerably higher speeds at a reduced level of power consumption as compared with the S series. ALS is not only considerably faster than the existing LS device but also offers a substantial reduction in power consumption. It is also pin-for-pin compatible with the standard logic families.

OXIDE-ISOLATED BIPOLAR TECHNOLOGY

The major improvement in the speed-power product of the Advanced Low-Power Schottky family as compared to earlier TTL families is due to advances in bipolar processing technology. Figure 1 compares the Advanced Schottky Oxide-Isolated Process with the 'standard' junction isolation process used in the Schottky and Low Power Schottky families. The Oxide-Isolated Process greatly reduces the parasitic sidewall capacitance asssociated with the collector-substrate junction. As a result, transistors with very fast and well controlled switching speeds, and with f_T's in excess of several gigahertz can be produced.



STANDARD LS AND S PROCESS

- CONVENTIONAL MASKS
- JUNCTION ISOLATION
- STANDARD METAL SYSTEM

ADVANCED SCHOTTKY PROCESS

- COMPOSED MASKS
- ION IMPLANTED
- OXIDE ISOLATION
- STANDARD METAL SYSTEM

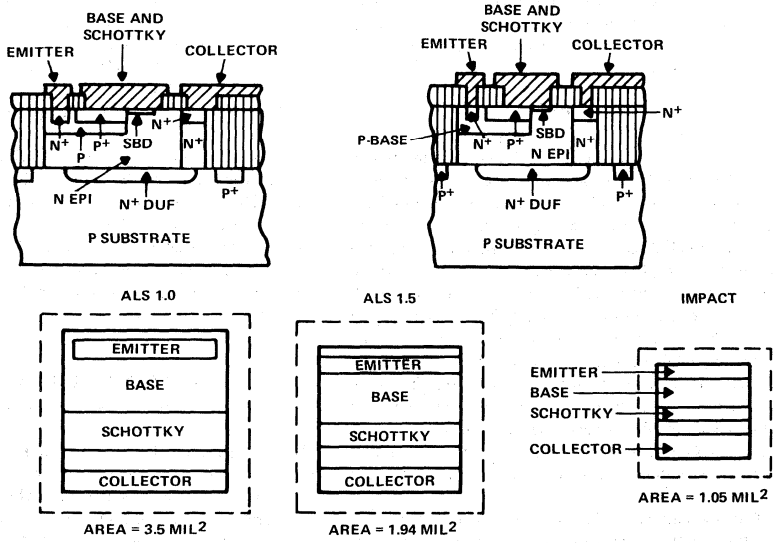
Figure 1. Transistor Cross Sections for Junction Isolated and Oxide-Isolated Bipolar Processes

In the oxide-isolated process, the various circuit components are separated by silicon dioxide rather than the junction isolation region used previously. Silicon dioxide is a dielectric material and there is no space-charge region formed at the interface. Therefore, both the base and emitter junctions can terminate in the oxide thus eliminating the sidewall capacitance of the base-collector junction and the emitter-base junction. In addition, the masks used in processing can overlap the device area into the oxide allowing standard lithographic processes to be used and easing the extremely close tolerances normally required for base and emitter masking.

Figure 2 shows how the Advanced Low-Power Schottky Process has evolved at Texas Instruments. The first generation of ALS devices was made using 4 μm minimum feature size design rules, composed masks and ion implantation(ALS 1.0). The next generation (ALS 1.5) was made using 2.5 μm minimum feature size design rules and including walled emitters as shown in Figure 2. The third generation (IMPACT), now in prototyping , uses two μm minimum feature size design rules. This evolution of the Advanced Low-Power Schottky Process has reduced the minimum area of a transistor from 3.5 mil^2 to 1.05 mil^2, permitting much more complex circuit design functions to be designed into the same die area.

The oxide-isolated process has been made possible by the use of composed masking, improvements in ion implantation techniques and improvements in the photolithography equipment and processes. Perfected ion implantation techniques now allow all junctions (with the possible exception of the buried-layer junctions) to be formed by ion implantation. The junction depths are shallower and doping profiles better controlled. This results in a narrower base region for bipolar transistors and much improved frequency response. The shallower junction depths permit thinner oxides for isolation with less growth along the surface directions during oxidation. The surface direction oxide growth is also reduced by using silicon nitride composed masks as shown in Figure 3.

Ion implantation also permits the space charge characteristics of the junction to be closely controlled so that acceptable breakdown voltages are obtained. However, the



	ALS 1.0	ALS 1.5	IMPACT
KEY FEATURES:	• 4 μm FEATURE SIZE • COMPOSED MASK • ION IMPLANT • OXIDE ISOLATION	• 2.5 μm FEATURE SIZE • LOW DUF SHEETS • WALLED EMITTER	• 2 μm FEATURE SIZE • COMPOSED MASK • WALLED EMITTERS
F/E ADVANCEMENTS	• HYPOX • LOW PRESSURE EPI	• PROJECTION PRINT • ARSENIC DUF	• 5X DSW PRINTERS • ARSENIC DUF
STATUS:	• IN PRODUCTION	• IN PRODUCTION	• IN PROTOTYPING

Figure 2. Device Area Reduction as a Result of Advanced Low-Power Schottky Process Development

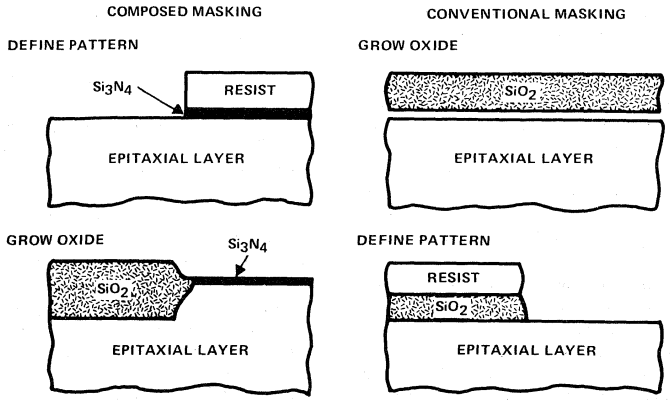


Figure 3. Composed Si_3N_4 Masking Compared to Conventional Masking

oxide isolated process allows smaller dimensions with shallower diffusions and oxides which enhance a devices susceptibility to electrostatic discharge (ESD) damage. Therefore, improved input and output circuits providing effective protection from ESD have been incorporated into the design for ALS devices.

RELIABILITY

Reliability is a measurement of how well an initially sound device will perform over time to its specified characteristics. Historically, semiconductor failures have primarily occurred during the early life phase of operation. After this initial phase, a low failure rate can be expected until the wearout phase is eventually reached. The largest contributor to infant mortality (early life failures) in TI bipolar devices was operator variability in the manufacturing process. For this reason, Texas Instruments has been aggressively adding automated equipment to critical stages of semiconductor production and package assembly.

Materials used in device fabrication also have an impact on the device reliability performance. Over the past four years, TI has evaluated over 100 encapsulating compounds and has selected those which provide the best product family performance.

Chip mounting materials also affect device integrity. A number of different adhesives have been evaluated by Texas Instruments for mechanical, chemical and electrical properties.It was found that many trade-offs existed in these products in terms of processibility and contamination levels. TI currently uses and will contiunue to use the product offering the best contribution to overall device reliability.

Many other areas of semiconductor fabrication and packaging are being researched. Die passivation, metallization, handling procedures, and leadframe construction and composition are a few of the areas under current investigation.

The reliability performance of Texas Instruments Advanced Low-Power Schottky (ALS) product is measured using the five major reliability tests listed below:

1. 125 °C operating life
2. 150 °C HTRB
3. 85 °C/85% RH with bias
4. Autoclave (121 °C/15 psig)
5. −65 °C/ + 150 °C temperature cycling

Numerous other tests are available and are used to supplement the information provided by the major reliability tests. These additional tests include thermal shock, high temperature storage, ESD sensitivity, thermal impedance, bond strength, lead bend and pull, solder heat, solderability, flammability, etc. The 1983 and 1984 reliability performance summary for typical non-burned-in ALS plastic devices is provided in the following tables.

OPERATING LIFE TESTS (Dynamic and Static)

125 °C Operating Life Test (Dynamic)

This high temperature operating life test is used to accelerate failure mechanisms which are time and temperature dependent allowing the simulation of long term device operation within a shorter period of time.(Tables 1 and 2)

High Temperature Reverse Bias-HTRB (Static)

This environmental test is designed to measure the failure rates and trends that can be expected in normal operation. It is usually carried out at elevated temperatures (125 °C or above) with reverse bias applied to the transistor junctions. The test determines the ability of the product to survive surface charge accumulation, charge injection, dielectric breakdown, and intermetallic growth. (Tables 1 and 2)

Table 1. ALS 1983 Reliability Summary
125°C Operating Life Test, 150°C HTRB Test

DEVICE	CONDITION	T_A °C	SAMPLES	TEST INTERVAL IN HOURS: FAILURES/DEVICES ON TEST 0	168	500	1000
'ALS08	STATIC	150	1	0/129	1/129	0/128	0/128
	DYNAMIC	125	1	0/129	0/129	0/129	0/129
'ALS74	STATIC	150	3	0/283	0/283	0/283	2/283
	DYNAMIC	125	3	0/283	0/283	1/283	0/282
'ALS876	STATIC	150	1	0/129	0/129	0/129	0/129
	DYNAMIC	125	1	0/88	0/88	0/88	0/88
Total			**10**	**0/1041**	**1/1041**	**1/1040**	**2/1039**

4.00 FITs (FAILURES/BILLION HOURS)
0.96 eV ACTIVATION ENERGY, AT 55°C AND 60% UPPER CONFIDENCE LEVEL

Table 2. ALS 1984 Reliability Summary
125°C Operating Life Test, 150°C HTRB Test

DEVICE	CONDITION	T_A °C	SAMPLES	TEST INTERVAL IN HOURS: FAILURES/DEVICES ON TEST 0	168	500	1000
'ALS00A	STATIC	150	2	0/258	0/258	0/258	0/258
	DYNAMIC	125	2	0/258	0/258	0/258	0/258
'ALS04A	DYNAMIC	125	1	0/129	0/129	0/129	0/129
'ALS10A	STATIC	150	1	0/129	0/129	0/129	0/129
'ALS28A	STATIC	150	1	0/129	0/129	0/129	0/129
'ALS74A	STATIC	150	1	0/129	0/129	0/129	0/129
'ALS74	STATIC	150	3	0/387	1/387	0/386	0/386
	DYNAMIC	125	3	0/387	0/387	0/387	0/387
'ALS810	STATIC	150	1	0/129	0/129	0/129	0/129
'ALS112	STATIC	150	1	0/129	0/129	0/129	0/129
'ALS112A	DYNAMIC	125	1	0/129	0/129	0/129	0/129
'ALS138	STATIC	150	2	0/258	0/258	1/258	1/257
	DYNAMIC	125	1	0/129	0/129	0/129	0/129
'ALS151	STATIC	150	1	0/129	0/129	0/129	0/129
	DYNAMIC	125	2	0/258	0/258	0/258	0/258
'ALS257	STATIC	150	1	0/129	0/129	1/129	2/128
	DYNAMIC	125	1	0/129	0/129	0/129	0/129
'ALS240A	STATIC	150	2	0/258	0/258	0/258	0/258
	DYNAMIC	125	2	0/258	0/258	0/258	0/258
'ALS299	STATIC	150	1	0/129	1/129	0/128	0/128
	DYNAMIC	125	1	0/129	0/129	0/129	0/129
'ALS645A	DYNAMIC	125	1	0/129	0/129	0/129	0/129
Totals			**32**	**0/4128**	**2/4128**	**2/4126**	**3/4124**

1.59 FITs (FAILURES/BILLION HOURS)
0.96 eV ACTIVATION ENERGY, AT 55°C AND 60% UPPER CONFIDENCE LEVEL

85 °C/85% RH WITH BIAS

In this environmental test the subject device is exposed to high humidity and temperature conditions (85% relative humidity and 85 °C) while having electrical bias applied to the circuit. Test duration is usually 1000 hours but may vary. This procedure is designed to measure the device's susceptibility to electrolysis and electrolytic corrosion. Failure mechanisms enhanced as a result of bias humidity include: corrosion of the aluminum metallization on the die; silver, tin, or gold migration from the leadframe; and parametric failures related to ionic conduction at the die/package interface. This biased temperature-humidity test is usually referred to as "85/85". (Tables 3 and 4)

Table 3. ALS 1983 Reliability Summary
85 °C/85% RH with Bias

		TEST INTERVAL IN HOURS: FAILURES/DEVICES ON TEST			
DEVICE	SAMPLES	0	168	500	1000
'ALS08	1	0/105	0/105	0/105	1/105
'ALS74	3	0/181	0/181	0/181	0/181
'ALS876	1	0/105	1/105	0/104	0/104
Total	**5**	**0/391**	**1/391**	**0/390**	**1/390**

0.5% FAILURES at 1000 HOURS

Table 4. ALS 1984 Reliability Summary
85 °C/85% RH with Bias

		TEST INTERVAL IN HOURS: FAILURES/DEVICES ON TEST			
DEVICE	SAMPLES	0	168	500	1000
'ALS00A	2	0/210	0/210	4/210	4/206
'ALS04B	1	0/129	0/129	0/129	0/129
'ALS10A	1	0/45	0/45	0/45	0/45
'ALS28A	1	0/105	0/105	0/105	0/105
'ALS74	3	0/315	1/315	2/314	3/312
'ALS74A	1	0/105	0/105	0/105	0/105
'ALS810	1	0/129	0/129	0/129	0/129
'ALS138	2	0/210	0/210	0/210	1/210
'ALS151	1	0/105	0/105	0/105	0/105
'ALS168B	1	0/105	0/105	0/105	0/105
'ALS257	1	0/105	0/105	0/105	1/105
'ALS240A	2	0/210	0/210	0/210	0/210
'ALS299	1	0/105	0/105	0/105	0/105
Total	**18**	**0/1878**	**1/1878**	**6/1877**	**9/1871**

0.9% FAILURES at 1000 HOURS

AUTOCLAVE

This environmental test of device reliability involves exposing the subject part to an atmosphere of high-temperature saturated steam under pressure (121 °C, 100% relative humidity at 15 psig). Unlike the bias humidity test, no electrical bias is applied to the device and the test duration is somewhat shorter. It indicates the susceptibility of the device to galvanic corrosion and therefore the electromotive forces of the elements involved are of great concern. The chemical instability of the encapsulating material and its tendency to form electrolytes add to the number of failures that result from this test. (Tables 5 and 6)

Table 5. ALS 1983 Reliability Summary
Autoclave (121 °C/15 psig)

		TEST INTERVAL IN HOURS: FAILURES/DEVICES ON TEST				
DEVICE	SAMPLES	0	96	144	192	240
'ALS08	1	0/52	0/52	0/52	0/52	0/52
'ALS74	3	0/126	0/126	0/126	0/126	0/126
'ALS876	1	0/52	0/52	0/52	0/52	0/52
Total	**5**	**0/230**	**0/230**	**0/230**	**0/230**	**0/230**

0.0% FAILURES at 240 HOURS

Table 6. ALS 1984 Reliability Summary
Autoclave (121 °C/15 psig)

		TEST INTERVAL IN HOURS: FAILURES/DEVICES ON TEST				
DEVICE	SAMPLES	0	96	144	192	240
'ALS00A	2	0/104	0/104	0/104	0/104	0/104
'ALS04B	1	0/77	0/77	0/77	0/77	0/77
'ALS28A	1	0/52	0/52	0/52	0/52	0/52
'ALS74	3	0/156	0/156	0/156	0/156	1/156
'ALS74A	1	0/52	0/52	0/52	0/52	0/52
'ALS810	1	0/71	0/71	0/71	0/71	0/71
'ALS112A	1	0/52	0/52	0/52	0/52	0/52
'ALS138	2	0/104	0/104	0/104	0/104	0/104
'ALS151	1	0/52	0/52	0/52	0/52	0/52
'ALS168B	1	0/52	0/52	0/52	1/52	0/51
'ALS257	1	0/52	0/52	0/52	0/52	0/52
'ALS240A	2	0/104	0/104	0/104	0/104	0/104
'ALS299	1	0/52	0/52	0/52	3/52	4/49
Total	**18**	**0/980**	**0/980**	**0/980**	**4/980**	**5/976**

0.9% FAILURES at 240 HOURS

−65 °C/+150 °C TEMPERATURE CYCLING

This reliability test is used to determine the compatibility of the materials used in device construction. The test requires cycling of the ambient temperature of the gas environment from a low point of typically −65 °C to a high temperature of 150 °C. These temperature extremes are not intended to simulate actual operation, but rather to exaggerate any faults that might exist. No bias is applied to the device. (Tables 7 and 8)

Table 7. ALS 1983 Reliability Summary
Temperature Cycling (−65 °C/+150 °C)

		TEST INTERVAL IN CYCLES: FAILURES/DEVICES ON TEST			
DEVICE	SAMPLES	0	100	500	1000
'ALS08	1	0/45	0/45	0/45	0/45
'ALS74	3	0/135	0/135	0/135	0/135
'ALS876	1	0/45	0/45	0/45	0/45
Total	**5**	**0/225**	**0/225**	**0/225**	**0/225**

0.0% FAILURES at 1000 CYCLES

Table 8. ALS 1984 Reliability Summary
Temperature Cycling (−65 °C/+150 °C)

		TEST INTERVAL IN CYCLES: FAILURES/DEVICES ON TEST			
DEVICE	SAMPLES	0	100	500	1000
'ALS00A	2	0/122	0/122	0/122	0/122
'ALS04A	1	0/45	0/45	0/45	0/45
'ALS04B	1	0/129	0/129	0/129	0/129
'ALS28A	1	0/77	0/77	0/77	0/77
'ALS74	3	0/199	0/199	0/199	0/199
'ALS74A	1	0/77	0/77	0/77	0/77
'ALS810	1	0/129	0/129	1/129	0/128
'ALS112A	1	0/45	0/45	0/45	0/45
'ALS138	2	0/122	0/122	0/122	0/122
'ALS151	1	0/77	0/77	0/77	0/77
'ALS161A	1	0/45	0/45	1/45	0/44
'ALS168B	1	0/77	0/77	0/77	0/77
'ALS257	1	0/45	0/45	0/45	0/45
'ALS240A	2	0/122	0/122	0/122	0/122
'ALS245A	3	0/231	0/231	0/231	1/231
'ALS299	1	0/45	0/45	0/45	0/45
'ALS574	2	0/122	0/122	0/122	0/122
'ALS645A	1	0/45	0/45	0/45	1/45
Total	**26**	**0/1754**	**0/1754**	**2/1754**	**2/1752**

0.2% FAILURES at 1000 CYCLES

GLOSSARY OF RELIABILITY TERMS

ACCELERATION FACTOR—The reaction rate of a process at one temperature or humidity condition compared with the rate at another (see appendix).

ACTIVATION ENERGY—The excess energy over the ground state which must be acquired by an atomic or molecular system in order for a specific process to occur.

AUTOMATED ASSEMBLY—Special equipment designed to reduce manufacturing costs and improve device reliability by eliminating operator variability.

BURN-IN—A procedure designed to reduce and stabilize the failure rate of a device population. By exposing the subject lot to high temperatures (typically 125 °C or higher) with electrical bias, early device failures (commonly known as infant mortality) can be detected and removed from the group.

CONFIDENCE LEVEL—A statistical expression for the degree of trust or assurance in a given statement or result. A confidence level is always associated with an assertion and indicates the probability that it is true.

ELECTROLYTE—A nonmetallic conductor in which current is carried by the movement of ions.

ELECTROLYSIS—The production of chemical changes by passing an electrical current through an electrolyte.

ENVIRONMENTAL TESTS—A general class of tests performed to enable estimations to be made of long term device stability and reliability. Devices under test are exposed to various combinations of extremely adverse conditions to aggravate potential faults in mechanical or electrical integrity and accelerate latent failures. Many common test procedures are defined in Military Standard 883.

FAILURE IN TIME (FIT)—A standard unit of measure for device failure rates in operating life and burn-in tests. One FIT represents one failure per billion (10^9) device hours or 0.0001%/1000 hr.

GALVANIC CORROSION—Corrosion related to the electromotive force potentials of two dissimilar elements.

HERMETIC DEVICE—A device sealed in a metal or ceramic package considered to be impervious to external moisture. These products have guaranteed leak rates of less than 10^{-5} cc/s of helium.

LEARNING CURVE—A principle which states, in a continuous situation, that the manufacturing efficiency and reliability of a product will improve with increased cumulative volume.

PLASTIC DEVICE—A device in a molded package composed of a plastic or plastic-like material. Unlike their hermetic counterparts, these products are not impervious to external moisture.

PRODUCT ENHANCEMENT PROGRAM—Special device preconditioning is offered by Texas Instruments to improve the reliability of semiconductor products. In the PEP 3 program, packaged devices are exposed to burn-in stress conditions and special testing designed to identify early failures and remove them from the lot being tested.

QUALITY—A product's degree of conformance to its specified parameters. It pertains to the probability of defective units existing in a given lot when received by the user.

RELIABILITY—A measurement of how well an initially sound device will perform over time to its specified characteristics. Overall system reliability is improved if early (infant mortality) failures are removed prior to system use.

UPPER CONFIDENCE LEVEL—Confidence levels represent the limits in the range of results that one might expect to see in a large number of samples from the same population. The upper confidence level (UCL) is the highest reject level expected at the confidence level expressed (often 60%).

APPENDIX

Reliability testing is often carried out at different conditions. In addition, it is not obvious how to relate test results at extreme times, temperatures,and humidities to real application conditions. Therefore, to enable the semiconductor user to more effectively interpret reliability data, two methods of equating results from dissimilar conditions have been developed by the semiconductor industry.

OPERATING LIFE TIME/TEMPERATURE ACCELERATION FACTOR (AF)[1]

$$AF = e^{\left[\frac{E}{K}\left(\frac{1}{T1} - \frac{1}{T2}\right)\right]}$$

Where

e = natural logarithm base of 2.71828
E = the activation energy for the semiconductor material (0.96 eV)
K = Boltzmann Constant (8.61423×10^{-5} eV/Kelvin)
T1 = lower temperature of the two conditions (in Kelvin)
T2 = higher temperature of the two conditions (in Kelvin)

For example, the AF between 125 °C and 55 °C = 393.8. In other words, device experience accumulated during one hour at 125 °C junction temperature approximates 393.8 hours (over 16 days) of normal operation at 55 °C. In this way, extremely long term failure rates in normal operation can be estimated with operating life tests lasting only a few thousand hours at elevated temperatures.

BIAS TEMPERATURE/HUMIDITY ACCELERATION FACTOR[2]

Acceleration factors (AF) which account for both temperature and humidity acceleration are more complicated and acceptance of these AF's within the semiconductor industry is mixed. Striny and Schelling evaluated several models for calculating the accelerating factors for aluminum metal corrosion between 85 °C and 85% R.H. and typical use conditions. Based on the fit of the data to the various models, they selected an Eyring model using an inverse humidity function. Using their equation and an activation energy of 0.706 eV, the AF for 85 °C/85% R.H. derated to 55 °C/50% R.H. would be 633. Although this overall acceleration factor is not commonly used, it does offer some guidance in analyzing bias humidity test results. Inasmuch as most real applications will usually not expose the device to these high temperature and humidity conditions, a 1000 hr. bias humidity (85/85) test can be interpreted as approximating the expected moisture related failures from 633,000 hrs (over 72 yrs) of operation at more moderate temperature humidity condition (55 °C/50% R.H.).

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[1]Zierdt, C.H. Jr., Bell Telephone Laboratories, " Source-Procurement Specification Techniques For High Reliability Transistors," presented at the 1967 Symposium on Reliability.

[2]Based on "Reliability Evaluation of Aluminum-metallized MOS Dynamic RAMs in Plastic Packages in High Humidity and Temperature Environment" by Kurt Striny and Arthur Schelling, Bell Labs, Allentown, PA.

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